Synthesis and Characterisation of Nanolayer Passivating Contacts for High Efficiency Solar Cells

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Abstract

Silicon solar panels currently suffer from defects at silicon-metal interfaces, which negatively impact their efficiency. To address this issue, passivating contact structures have been developed to reduce the harmful effects of interface defects. While SiO_x/poly-Si contacts have proved an effective electron contact, they are less effective as a hole contact, due to the lower conductivity to holes and high boron diffusivity through the SiO_x. The thin layers in the passivating contacts prohibit the use of standard techniques for understanding Si/dielectric interfaces. Thus, to improve hole-selective contacts, an alternative to SiO_x is required, combined with new techniques to extract the interface properties and improve the understanding of the contacts.

This thesis investigates the potential for SiN_x, AlO_x, and TiO_x nanolayers to form effective hole-selective contacts and introduces two techniques for analysing the interface properties of the novel dielectrics. The nanolayer fabrication, material properties, conductivity and passivation quality are investigated for single layers and in poly-Si contact stacks. The AlO_x and SiN_x formed contacts with resistivity as low as $\sim$100 m$\Omega \cdot$cm^2 via a low-temperature process and <80 m$\Omega \cdot$cm^2 with a highly doped poly-Si capping layer. An ultra-thin RCA2 SiO_x was found to significantly improve the passivation quality of the nanolayers with the lowest dark saturation currents of 94 fA/cm^2 and 140 fA/cm^2 achieved for a low-temperature RCA2+AlO_x and a hydrogenated RCA2+SiN_x/poly-Si, respectively. Adapted capacitance-voltage and conductance-voltage techniques are developed for characterising the interface properties of conductive films and were implemented on SiN_x, AlO_x, and TiO_x nanolayers. A high charge of -3×10^{12} q/cm^2 and -4.6×10^{12} q/cm^2 was measured on the AlO_x and TiO_x structures, respectively. Through simulations, it was shown that a high charge can significantly improve the passivation quality of the contacts and could lead to efficiency gains of $1\%_{abs}$, compared to a SiO_x poly-Si contact.

The first demonstration of low resistivity SiN_x and AlO_x poly-Si contacts have been shown, with the passivation of the RCA2+SiN_x poly-Si contact approaching SiO_x/poly-Si reference. With improved process uniformity these contacts could match or outperform SiO_x hole contacts. In combination with a highly selective electron contact, cell efficiencies >28% could be obtained, approaching the intrinsic limit for Si single junction cells. Further efficiency gains could be obtained when the contacts are incorporated into the bottom cell of a tandem structure. The techniques applied to these nanolayers provide a detailed understanding, enabling the optimisation of passivating contact structures. The techniques developed are transferable to a wide range of interlayers in solar devices, including perovskite cells and tandem architectures. In a broader context, the techniques could increase the understanding of interfaces in other electronic devices, such as connections to 2D materials used in nanoelectronics.

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For my Dad, Hamish, who would be proud to see his love of science rubbed off on me.

List of Acronyms and abbreviations

PV	Photovoltaics
TOPCon	Tunnel Oxide Passivated Contact
HJT	Heterojunction Technology
DFPC	Dopant Free Passivating Contact
PERC	Passivated Emitter Rear Cell
PECVD	Plasma Enhanced Chemical Vapour Deposition
ALD	Atomic Layer Deposition
RTO	Rapid Thermal Oxidation
RIE	Reactive Ion Etching
XPS	X-ray Photoemission Spectroscopy
ECV	Electro-Chemical Voltage
SPV	Surface Photovoltage
KP	Kelvin Probe
C-V	Capacitance-Voltage
G-V	Conductance-Voltage
J-V	Current Density-Voltage
T-JV	Temperature-dependent J-V
HF	Hydrofluoric acid
SRH	Shottkey Reed Hall
FEP	Field Effect Passivation
CBO	Conduction Band Offset
VBO	Valance Band Offset
SiO_x	Silicon Oxide
SiN_x	Silicon Nitride
AlO_x	Aluminium Oxide
TiO_x	Titanium Oxide
SiO_xN_y	Silicon Oxynitride

List of Symbols

T	Temperature [°C] or [K]
E_B	Binding Energy [eV]
E_k	Kinetic Energy [eV]
E_{CL}	Core Level Energy [eV]
E_V	Valance Band Onset Energy [eV]
ΔE_V	Valence Band Offset (VBO) [eV]
τ_{eff}	Effective Lifetime [μs]
τ_{bulk}	Silicon Bulk Lifetime [μs]
J_0	Dark Saturation Current [fA/cm^2]
t_{diel}	Dielectric thickness [nm]
ρ_{tot}	Total resistivity [Ω·cm^2]
ρ_c	Contact resistivity [Ω·cm^2]
ρ_{tun}	Tunnelling resistivity [Ω·cm^2]
ρ_{pin}	Pinhole resistivity [Ω·cm^2]
ρ_{waf}	Base wafer resistivity [Ω·cm]
$P_{tun,h}$	Tunnelling probability of holes
ϕ_B	Schottky Barrier Height [eV]
ϕ_F	Fermi Energy [eV]
ϵ	Permittivity
m_0	Free Electron Mass [kg]
m_h^*	Hole Effective Mass
n	Ideality Factor
$\hbar$	Plancks Constant [J·s]
k_B	Boltzmann's constant [J/K]
r_{pin}	pinhole radius [nm]
N_{pin}	pinhole density [cm^{-2}]
t_{waf}	wafer thickness [μm]
D_{it}	Interface defect state density [cm^{-2}]
Q_f	Dielectric fixed charge [q/cm^2]
C	Capacitance [nF]
G	Conductance [mS]
V	Voltage [V]

Preface

This thesis is an account of the work I have carried out as a postgraduate student at the Department of Materials, University of Oxford. I have not previously submitted any part of this thesis for a degree at this University or elsewhere. The work of other authors is duly acknowledged in the text, and appropriate references are given.

During the course of this thesis, I have written or contributed towards the following publications:

1. S. McNab, X. Niu, E. Khorani, A. Wratten, A. Morisset, N. E. Grant, *et al.*, “SiNx and AlOx nanolayers in hole selective passivating contacts for high efficiency silicon solar cells,” *IEEE Journal of Photovoltaics*, pp. 1–11, 2022. DOI: 10.1109/JPHOTOV.2022.3226706

2. S. McNab, M. Yu, I. Al-Dhahir, E. Khorani, T. Rahman, S. A. Boden, *et al.*, “Alternative dielectrics for hole selective passivating contacts and the influence of nanolayer built-in charge,” AIP Conference Proceedings, 2022, p. 020 013. DOI: 10.1063/5.0089282

3. T. Matsui, S. McNab, R. S. Bonilla, and H. Sai, “Full-Area Passivating Hole Contact in Silicon Solar Cells Enabled by a TiOx/Metal Bilayer,” *ACS Applied Energy Materials*, 2022. DOI: 10.1021/ACSAEM.2C02392

4. E. Khorani, S. McNab, T. E. Scheul, T. Rahman, R. S. Bonilla, S. A. Bowden, *et al.*, “Optoelectronic properties of ultrathin ALD silicon nitride and its potential as a hole-selective nanolayer for high efficiency solar cells,” *APL Materials*, vol. 8, no. 11, p. 111 106, 2020. DOI: 10.1063/5.0023336

5. I. Al-Dhahir, S. McNab, M. Yu, E. Shaw, P. Hamer, and R. S. Bonilla, “The influence of surface electric fields on the chemical passivation of si-sio2 interfaces after firing,” *AIP Conference Proceedings*, vol. 2487, p. 130 001, 1 2022. DOI: 10.1063/5.0089930

6. M. Yu, S. McNab, I. Al-Dhahir, C. E. Patrick, P. P. Altermatt, and R. S. Bonilla, “Extracting band-tail interface state densities from measurements and modelling of space charge layer resistance,” *Solar Energy Materials and Solar Cells*, vol. 231, p. 111 307, 2021. DOI: 10.1016/J.SOLMAT.2021.111307

7. I. Al-Dhahir, R. Kealy, S. Kelly, M. Yu, S. McNab, K. Collett, *et al.*, “Electrostatic tuning of ionic charge in sio2 dielectric thin films,” *ECS Journal of Solid State Science and Technology*, vol. 11, p. 063 010, 6 2022. DOI: 10.1149/2162-8777/AC7350.

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Contents

List of Acronyms and abbreviations iv

List of Symbols v

Preface vi

List of Figures xiii

List of Tables xx

1 Introduction 1
- 1.1 Climate Change . . . 1
- 1.2 Renewable Electricity Generation . . . 2
  - 1.2.1 Solar Electricity Generation . . . 3
- 1.3 Photovoltaic Cell Materials . . . 3
- 1.4 Scope for Improvements in Silicon Solar . . . 4
  - 1.4.1 Efficiency . . . 4
  - 1.4.2 Sustainability . . . 4
- 1.5 Passivating Contacts . . . 5
- 1.6 Aims and Objectives . . . 6
- 1.7 Structure of this thesis . . . 6

2 Literature Review 7
- 2.1 The Metal/Semiconductor (MS) Interface . . . 7
  - 2.1.1 Ideal Interfaces . . . 7
  - 2.1.2 Real Interfaces . . . 7
  - 2.1.3 Metal-Insulator-Semiconductor (MIS) Contact . . . 8
- 2.2 Recombination . . . 8
  - 2.2.1 Types of Recombination . . . 9
  - 2.2.2 Recombination Parameters . . . 10
- 2.3 Passivation . . . 12
  - 2.3.1 Bulk . . . 12
  - 2.3.2 Surface . . . 13
  - 2.3.3 Contacts . . . 16
- 2.4 Cell Contact Technologies . . . 17
- 2.5 Poly-Si Contacts using Silicon Oxide . . . 20

2.5.1 Silicon Oxide and Poly-silicon fabrication 20
2.5.2 Influence of the Post Deposition Anneal 21
2.5.3 Conduction Mechanisms in Poly-Si Contacts 22
2.5.4 Hydrogenation 23
2.5.5 Metallisation 24
2.6 Poly-Si Contacts using Alternative Dielectrics 24
2.6.1 Aluminium Oxide 25
2.6.2 Silicon Nitride 25
2.7 Dopant Free Passivating Contacts 25
2.7.1 Titanium Oxide in DFPC 26
2.8 Fixed Charge in Passivating Contacts 26
2.9 Hole Contacts 27
2.10 Characterising Passivating contacts 29
2.11 Contribution to the Scientific Field/justification for the work 30

3 Experimental Methods **31**
3.1 Specimen Fabrication 31
3.1.1 Wafers 31
3.1.2 Rapid Thermal Oxidation, RTO 31
3.1.3 Plasma Enhanced Chemical Vapour Deposition, PECVD 32
3.1.4 Atomic Layer Deposition, ALD 33
3.1.5 Metal Contact Deposition 34
3.1.6 Reactive Ion Etching, RIE 35
3.1.7 Corona Charging 35
3.1.8 Transportation and Storage 35
3.2 Ellipsometry 35
3.3 X-ray Photoelectron Spectroscopy, XPS 38
3.3.1 Nanolayer Thickness Determination using XPS 40
3.4 Current-Voltage, J-V 41
3.4.1 Theoretical fitting of J-V curves 41
3.4.2 Temperature-Dependent J-V, T-JV 42
3.5 Lifetime Measurements via Photo-Conductance Decay 43
3.6 Capacitance-Voltage, C-V 44
3.6.1 Conductance-Voltage, G-V 46
3.7 Kelvin Probe 46
3.7.1 Surface Photovoltage 48

4 Understanding Hole Selective Contacts Through Device Simulations **49**
4.1 Theoretical Calculations of Tunnelling Probability 51
4.2 Sentaurus TCAD Finite Element Simulation Set-Up 53
4.2.1 Resistivity Simulation 54
4.2.2 Passivation Simulation 55
4.3 Effect of Dielectric Thickness on Contact Resistivity 55
4.3.1 Comparison of Sentaurus TCAD and Theoretical calculations 56
4.4 Effect of Interface Charge on the Contact Resistivity 57

4.4.1 Effect of Charge on Contact Resistivity for Varied Dielectric Thickness . . . 57
4.4.2 Influence of Doping Profiles on the Contact Resistivity 58
4.4.3 Application to Realistic Structures 59
4.5 Effect of Interface Charge on Passivation Quality 59
4.5.1 Influence of Charge for Varying Levels of Chemical Passivation 59
4.5.2 Influence of Charge for Different Doping Profiles 60
4.5.3 Realistic Contact Structures 61
4.6 Effect of Interface Charge on the Contact Selectivity 63
4.7 Discussion 64
4.8 Summary 65

5 Fabrication and Physical Properties of Nanolayer Dielectrics 66
5.1 Nanolayer Growth and Thickness Determination 67
5.1.1 Silicon Oxide 67
5.1.2 Silicon Nitride 68
5.1.3 Aluminium Oxide 71
5.1.4 Titanium Oxide 73
5.2 Nanolayer Stability 74
5.3 Stoichiometry 75
5.4 Valence Band Offsets 79
5.4.1 Influence of Sputtering 79
5.4.2 Bare Silicon 79
5.4.3 Silicon Oxide 79
5.4.4 Silicon Nitride 82
5.4.5 Aluminium Oxide 85
5.4.6 Comparison of VBO for Dielectric Nanolayers 87
5.5 Discussion 88
5.6 Summary 90

6 Carrier Transport in Nanolayer Dielectric Contact Structures 91
6.1 Contact Resistivity of Dielectric Nanolayers in MIS Structures 91
6.1.1 Influence of Capping Metal and Wafer Doping 91
6.1.2 Resistivity Dependence on Dielectric Thickness 93
6.1.3 Resistivity of RCA2+Dielectric Nanolayer Stacks 94
6.2 Determination of Conduction Mechanisms through Temperature-Dependent J-V . . 96
6.2.1 Silicon Oxide 96
6.2.2 Silicon Nitride 97
6.2.3 Aluminium Oxide 98
6.2.4 Titanium Oxide 100
6.3 Discussion 100
6.4 Summary 102

7 Passivation at Silicon-Nanolayer Dielectric Interfaces 103
7.1 Development of Novel Characterisation Techniques 103
7.1.1 Conductance-Voltage, G-V 104

7.1.2 Capped C-V measurements . . . 105
7.2 Silicon Oxide Interface Nanolayers . . . 107
7.2.1 Lifetime Measurements . . . 107
7.2.2 SPV . . . 108
7.2.3 Capped C-V . . . 108
7.2.4 Summary . . . 110
7.3 Silicon Nitride Interface Nanolayers . . . 110
7.3.1 Lifetime . . . 110
7.3.2 SPV . . . 111
7.3.3 Capacitance and Conductance Measurements . . . 112
7.3.4 Summary . . . 112
7.4 Aluminium Oxide Interface Nanolayers . . . 114
7.4.1 Lifetime . . . 114
7.4.2 SPV . . . 115
7.4.3 Capacitance and Conductance Measurements . . . 116
7.4.4 Summary . . . 118
7.5 Titanium Oxide Interface Nanolayers . . . 119
7.5.1 Lifetime . . . 119
7.5.2 Plasma and Thermal ALD Titanium Oxide . . . 120
7.5.3 Effect of Post-Deposition Processing . . . 120
7.5.4 Effect of Silicon Orientation . . . 122
7.5.5 Effect of UV degradation . . . 123
7.5.6 Summary . . . 124
7.6 Discussion . . . 125
7.6.1 Comparison of Techniques . . . 125
7.6.2 Comparison of Nanolayer Dielectric Interfaces . . . 126
7.7 Summary . . . 128

8 Poly-Si on Oxide and Nitride Nanolayer Contacts 129
8.1 Resistivity of Poly-Si Contacts . . . 130
8.1.1 Effect of Anneal Temperature . . . 130
8.1.2 Comparison of Dielectrics . . . 131
8.2 Passivation of Poly-Si Structures . . . 133
8.3 Boron In-diffusion in Poly-Si structures . . . 134
8.4 Discussion . . . 135
8.5 Summary . . . 137

9 Summary and Further Work 138
9.1 Future work . . . 139

Bibliography 142

Appendix A: Derivation of Direct Tunnelling Current 169

Appendix B: Additional Methods 173

Appendix C: Simulations **175**

Appendix D: Fitting inputs **178**

Appendix E: Poly-Si **183**

Appendix F: XPS Peak fitting **185**

List of Figures

1.1 a) Change in atmospheric CO_2 concentration since 1800 b) Change in the Earths mean temperature compared to solar irradiance since 1880. Data from GISS NASA [9], GISTEMP[11], NOAA [9], [12] 2
1.2 a) TWh of energy produced per year for main renewable sources [18] b) Yearly availability of renewable energy sources compared to the annual global electricity demand. From Our world in data. Data from BP statistical review of world energy (Areas of the full circle are to scale). Adapted from [19] 2

2.1 a) ideal MS contact b) real MS contact c) real MIS contact 8
2.2 Types of recombination in semiconductors. a) Radiative, b) Shockley-Read-Hall, and c) Auger Recombination 9
2.3 Schematic band diagrams of a) Unpassivated silicon surface with defect states b) silicon surface with chemical passivation and c) silicon surface with chemical and field-effect passivation 13
2.4 Typical D_{it} and Q_f for common surface passivation layers [63]. 14
2.5 a) Schematic of a PERC cell and b) Band Diagram of the PERC hole contact 17
2.6 a) Schematics of cell featuring electron and hole selective poly-Si contacts. b) Band Diagrams of hole selective poly-Si contacts on a p or n-type silicon substrate. 18
2.7 a) Schematic of SHJ cell structure and b) Band Diagrams of hole selective SHJ contacts with an n or p-type silicon substrate. 18
2.8 a) Schematic of DFPC cell structure and b) Band Diagram of DFPC low WF oxide on n-Si base wafer c) Band diagram of high WF metal-oxide with SiO_x interlayer, on p-Si wafer. 19
2.9 J_0 and ρ_c for a selection of passivating contact technologies. The black lines show the optimum contact area, as a percentage. The efficiency simulation is based on an idealised front contact, full area back contack and no absorption losses. Reproduced from [108]. . . 20
2.10 Components of a poly Si based contact 21
2.11 TEM images of the cross-sectional structures around the SiO_x layers in as-deposited states, annealed at 850 °C, 900 °C, 950 °C, and 1000 °C for the samples with (a)–(e) 1.2 nm-thick SiO_x layers and (f)–(j) 1.5 nm-thick SiO_x layers. The Fast fourrier transport images in (a) and (b) show the crystallisation of the a-Si and were obtained from the red-boxed regions. Reproduced from [145]. 22
2.12 Current flow through a dielectric with a) tunnelling-dominated conduction and b) pinhole-dominated conduction. 23
2.13 Figure showing the lifetime curves at each stage of the poly-Si process [160]. 24
2.14 Dopant profiles in a) phosphorus and b) boron poly-Si contacts [129]. 28

3.1 Programmed temperature profile and gas flows for SiO_x growth using RTO 32
3.2 AlO_x ALD reaction process a) Si surface terminated with O-H groups. b) 2×pulse-purge cycles of TMA form an Al terminated surface c) 3×pulse-purge cycles of H_2O terminate the surface with Hydroxyl groups. d) The process repeats to grow an AlO_x layer. . . . 34
3.3 Schematic of the sample structures for electrical characterisation techniques. a) Single nanolayer structures b) Full poly-Si stack 34
3.4 Schematic of an Ellipsometry measurement. Linearly polarised light is reflected off the sample surface, the magnitude and phase change of the polarisation is measured at the detector. 36
3.5 Ellipsometry fit for a) SiO_x, b) SiN_x, c) AlO_x, d) TiO_x 37
3.6 Photo-emission of an electron due to an incident x-ray. [229] 38
3.7 Energy Bands at a silicon/dielectric interface, with annotations indicating the energy differences used in the Krauts method to determine the VBO. 39
3.8 MIS sample structure with the resistive components annotated. 41
3.9 Illumination and photoconductance intensity for measurement of effective lifetime in a) transient and b) QSS modes 44
3.10 The top figures show band diagrams of an MIS structure in a) accumulation, b) flat-band c) depletion. The distribution of charge in the semiconductor and insulator is shown below and the insets show the equivalent circuit diagram in each regime. 45
3.11 High-frequency CV curve of a 100 nm SiO_x on n-type Si, with fitting parameters. . . . 45
3.12 a) Schematic of KP measurement for a dielectric with a high negative charge on n-Si a) in the dark and b) under illumination. The charge distribution in the silicon and dielectric is indicated below. 47

4.1 Selectivity, Efficiency and optimal contact area fraction as a function of J_0 and ρ_c. Blue lines show the Selectivity, red lines show the maximum efficiency and black lines show the optimum area fraction. The efficiency values are for a full-area contact. Adapted from [255]. 50
4.2 Tunnelling probability of electrons and holes a) SiO_x b) AlO_x c) SiN_x, and d) TiO_x. Values used are found in Tables 4.1 and 4.2. 53
4.3 Schematics of simulated poly-Si structure for a) contact resistivity simulations, b) J_0 Simulation. 54
4.4 Doping profiles for a) varying dopant concentration in the poly-Si and b) varying peak dopant concentration in the wafer. The dielectric interface is at 0 μm. 55
4.5 Total resistivity of a poly-Si contact structure. Solid lines indicate the theoretical calculations and open shapes indicate the Sentaurus TCAD simulations. 56
4.6 The effect of interface charge on the resistivity of a poly-Si structure for different SiN_x thicknesses. 57
4.7 The resistivity of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for varying poly-Si doping concentration. Where $[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$. 58
4.8 The effect of charge on J_0 for different levels of chemical passivation. 60
4.9 The J_0 of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for a) varying poly-Si doping concentration ($[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$). 61
4.10 S_{n0} calculated for a) SiO_x [187] SiN_x [170] and c) AlO_x [176] using values of τ_{eff} or J_0 from literature. Dash lines indicate the value of S_{n0} extracted. 61

4.11 J_0 of SiO_x SiN_x and AlO_x poly-Si contacts as a function of dielectric charge. Values of S_{n0} obtained from Figure 4.10 . . . 62
4.12 The Selectivity, S_{10} of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for varying poly-Si doping concentration ($[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$) . . . 63

5.1 Ellipsometry thickness measurements of SiO_x a) as a function of oxidation time b) showing uniformity of a 10 s oxidation over a 4″ wafer after a 5 min 450 °C hotplate anneal. . . . 68
5.2 Ellipsometry measurements of thickness and RI for a) 5 s PECVD SiN_x on P1-10 silicon for increasing plasma power. The samples underwent a 450 °C post-deposition hot plate anneal and b) 5 s SiN_x with increasing ammonia flow rates using a PECVD power of 20 W. Lines are a guide to the eye. . . . 69
5.3 Ellipsometry measurements a) of SiN_x thickness for increasing deposition time as-deposited and b) comparing the RI to the SiN_x thickness. . . . 70
5.4 Ellipsometry thickness measurements showing uniformity over a 4″ P1-10 wafer for a) 3 s SiN_x and b) of RCA+3 s SiN_x, after a 5 min 400 °C anneal. . . . 71
5.5 Thickness measurements of AlO_x a) Measured using ellipsometry and XPS for increasing number of deposition cycles b) Ellipsometry measurements showing thickness uniformity of 5 cycles thermal ALD over a 4″ wafer after a 5 min 400 °C anneal. . . . 72
5.6 Uniformity measurements of the TiO_x over 4 cm sample. . . . 73
5.7 Evolution of dielectric film thickness overnight and after hotplate anneals. a) SiO_x b) SiN_x and c) AlO_x. . . . 75
5.8 Si:O ratio for bulk and thin SiO_x films . . . 76
5.9 a) Atomic concentrations of silicon, nitrogen and oxygen and b) Si:N ratio in SiN_x bulk and thin films. Ann denotes the hotplate anneal and Spl the sputtered bulk. In b) dark blue plots indicate measurements taken with the TSK XPS and light blue bars represent PhiV XPS data. . . . 77
5.10 Al:O ratio for bulk and thin AlO_x films. Dark blue indicates measurements taken with the TSK XPS and light blue represent the PhiV XPS data. Spl refers to the sputtered Bulk . . . 78
5.11 TSK XPS of bare P1-10 silicon wafer a) valence band onset b) Si 2p peak with fitting. . 80
5.12 TSK XPS peaks for SiO_x a) 10 nm SiO_x Si 2p peak, b) 10 nm SiO_x O 1s peak c) 3 nm SiO_x Si 2p peak, d) 3 nm SiO_x O 1s peak, e) 10 nm SiO_x valence band onset. . . . 81
5.13 TSK XPS peaks for SiN_x annealed at 450 °C on P1-10 Si a) Bulk SiN_x Si 2p peak, b) Bulk SiN_x N 1s peak c) 3 nm SiN_x Si 2p peak, d) 3 nm SiN_x N 1s peak, e) Bulk SiN_x valence band onset. . . . 83
5.14 Normallised XPS spectra of the Si2p peak for SiN_x, annealed SiN_x, annealed a RCA+3 s SiN_x and an SiO_x layers on P1-10 wafers. . . . 85
5.15 TSK XPS peaks for ALD AlO_x a) Thick AlO_x Al 2p peak, b) Thick AlO_x O 1s peak c) Thin AlO_x Si 2p peak, d) Thin AlO_x O 1s peak, e) Thin AlO_x Al2p peak, f) Thick AlO_x valence band onset. . . . 86
5.16 Valence band offsets of SiO_x, SiN_x and AlO_x to P1-10 Si. . . . 88

6.1 Resistivity of a SiO_x nanolayer determined from I-V measurements showing the influence of wafer doping and capping metal. Crosses show the resistivity of each measured metal contact. The inset shows a schematic of the sample structure. 92
6.2 J-V curves of a) SiO_x b) SiN_x and c) AlO_x on P1-5m wafers. Experimental data are depicted as points with lines for a guide to the eye. Shaded areas give theoretical fitting and the thicknesses indicated on the plot are the values determined from ellipsometry. . 93
6.3 Resistivity as a function of dielectric thickness for SiO_x, SiN_x and AlO_x. Solid lines indicate the theoretical fitting for each dielectric, assuming the transport mechanism is purely tunnelling 94
6.4 Resistivity of RCA2 stacks on P1-5m with gold contacts a) RCA2 single-layer, SiN_x single-layer and RCA2+3 s SiN_x stack b) RCA2+5 cycles AlO_x and RCA2+10 cycles AlO_x. Crosses show the resistivity of each measured metal contact. 95
6.5 Temperature-dependent J-V measurements with theoretical fitting a) 10 s RTO SiO_x and c) RCA2 chemical SiO_x. The total resistivity as a function of temperature for b) 10 s RTO SiO_x and d) RCA2 chemical SiO_x. Open symbols show the experimental data and solid lines are obtained from theoretical calculations. 97
6.6 Temperature-dependent J-V measurements with theoretical fitting for a) 5 s SiN_x and c) RCA2+3 s SiN_x. Total resistivity as a function of temperature for b) 5 s SiN_x and d) RCA2+3 s SiN_x. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations. 98
6.7 Temperature dependent J-V measurements with theoretical fitting for a) 5 cycles AlO_x and c) RCA2+5 cycle AlO_x. Total resistivity as a function of temperature b) 5 cycles AlO_x and d) RCA2+5 cycles AlO_x. e) and f) are the RCA2+5 cycles AlO_x measurements fitted with a purely tunnelling current. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations. 99
6.8 a) Temperature-dependent J-V of 5 nm TiO_x layer with Au contact b) TiO_x resistivity as a function of thickness. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations. 100

7.1 C-V curves for a) thermal 100 nm SiO_x layer on n-type Si b) a thin, leaky dielectric on p-type Si. 104
7.2 G-V curves for a) a highly resistive, thick dielectric b) thin, leaky dielectric c) Example of fitting the G-V curves to the $|Q_{abs}|$. 106
7.3 C-V measurement of 100 nm PECVD SiO_x with 350 °C hotplate anneal and Al contacts 107
7.4 Effective lifetime of a) 10 s RTO SiO_x and an RCA2 SiO_x on N30-60 with a hotplate anneal, and b) a 10 s RTO SiO_x with negative corona charging. Lines are a guide to the eye, with each line representing a separate sample 108
7.5 CPD of SiO_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map. 109
7.6 Estimated D_{it} and Q_f from SPV results. Red lines indicate the CPD values from Figure 7.5. Black lines show the CDP_{dark} values superimposed on the SPV plot. 109
7.7 Capped C-V measurements of RCA2 SiO_x layer for varying anneal temperature. Inset shows a schematic of the measured structure. 110

7.8 Effective Lifetime of SiN_x on N30-60 for a) increasing anneal temperature b) deposition of negative corona charge. Lines are a guide to the eye, with each line representing a separate sample. . . . 111
7.9 CPD of SiN_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map. . . . 112
7.10 Estimated D_{it} and Q_f from SPV for a 5 s SiN_x annealed at 350 °C. Red lines indicate the CPD values from Figure 7.9. Black lines show the CDP_{dark} values superimposed on the SPV graph . . . 113
7.11 G-V of SiN_x for increasing deposition time on P1-10 wafers and with Au contacts. . . . 113
7.12 Capped C-V measurements of SiN_x and RCA2+SiN_x layers for varying anneal temperature. 114
7.13 Lifetime of ALD AlO_x with a hotplate anneal. Lines are a guide to the eye, with each line representing a separate sample . . . 115
7.14 CPD of AlO_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map. . . . 116
7.15 Estimated D_{it} and Q_f from SPV measurement of 5 cycles AlO_x after 450 °C anneal. Black lines show the CDP_{dark} values superimposed on the SPV graph. . . . 117
7.16 G-V of AlO_x for increasing deposition cycles. The value of conductance used to represent the onset of excessively high conductance is reduced as the thickness increases. . . . 117
7.17 C-V measurements of AlO_x nanolayers using a PECVD SiO_x capping layer. Solid black lines give the theoretical fits. . . . 118
7.18 Effective Lifetime of plasma and thermal ALD TiO_x as-deposited and after various post-deposition processes. The samples underwent an anneal (Ann), a HPT or both. Measurements were carried out before (AIST) and after transportation (Sample 1 and 2). 119
7.19 CPD measurements of plasma and thermal ALD TiO_x in the dark and under illumination. 120
7.20 Estimated D_{it} and Q_f of tALD TiO_x from SPV. . . . 121
7.21 Dark and illuminated CPD measurements of thermal ALD TiO_x sample as-deposited, with an anneal, with HPT treatment and with an anneal and HPT treatment. . . . 121
7.22 G-V analysis of a TiO_x sample as deposited, with HPT treatment, with an anneal and with HPT+anneal . . . 122
7.23 G-V analysis of TiO_x deposited on (100) and (111) wafers . . . 123
7.24 Dark and illuminated CPD measurements of thermal TiO_x deposited on (100) silicon, (111) silicon and textured silicon. . . . 123
7.25 Dark and illuminated measurements of UV degraded of TiO_x with HPT treatment. The sample is initially degraded with 100 hr of UV, then it is recovered with a 2 hr anneal at 180 °C, before a second degradation. . . . 124
7.26 G-V analysis of TiO_x as deposited, after HPT and after 100 hr light soaking . . . 125
7.27 Comparison of a) τ_{eff} on N30-60 wafers, b) SPV on P1-10 wafers and c) capped CV measurements on P1-10 wafers and after 350 °C anneal for Si/dielectric interfaces . . . 127

8.1 Process flow for poly-Si contacts. . . . 129
8.2 Contact resistivity of Dielectric/poly-Si structures for poly-Si anneal temperature between 800–900 °C. . . . 130

8.3 Temperature dependent Contact resistivity of 3 s SiN_x/poly-Si structures for poly-Si anneal temperature between 800–900 °C. 131
8.4 a) Contact resistivity of Dielectric/poly-Si structures. The grey boxplots show ρ_c for UV-O_3 SiO_x and 3 s SiN_x from Batch 1. b) Temperature-dependent Contact resistivity of Dielectric/poly-Si structures 132
8.5 a) τ_{eff} and b) iV_{OC} of the dielectric/p^+poly-Si structures. Batch 2a samples were measured after the high-temperature anneal but were not hydrogenated. 133
8.6 PL images of 4" wafers with poly-Si structures after hydrogenation. a) UV-O_3 SiO_x, b) RCA+SiN_x and c) SiN_x 134
8.7 Active boron concentration as a function of depth for the dielectric/poly-Si structures. . 135
8.8 J_0 and ρ_c of the best contacts fabricated in this work and selected work from literature. Black dashed lines indicate the Selectivity. Results from this work are represented by shaded symbols and results from literature are shown as open symbols [156], [178], [187], [214], [318], [327]–[330]. 137

A1 Free electron wave approaching a potential barrier 169
A2 Qualitative solution to the potential barrier problem. 171
A3 Schematics of simulated structures. a) poly-Si structure for contact resistivity simulations, b) DFPC structure for contact resistivity simulations c) poly-Si structure for J_0 Simulation. 175
A4 Simulations of a) ρ_c and b) J_0 for a DFPC structure and a poly-Si structure with the parameters from Table 4.3. 176
A5 a) Doping profiles for varying peak in-diffusion, $[B]_{poly\text{-}Si} = 1.3\times10^{20}$ cm^{-3}. b) Resistivity c) J_0 and d) Selectivity of a 2 nm SiN_x/poly-Si contacts as a function of dielectric charge. 177
A6 CPD signal as a function charge for determination of the carrier density during KP measurements. The black line indicates a measurement in the dark, the yellow line is generated by a carrier generation of 1×10^{18} cm^{-3} at the silicon surface, the blue line shows the equivalent carrier density of 5×10^{13} cm^{-3} to match the generation profile, and the dashed blue line show the high carrier density required to obtain a negative SPV on a p-type substrate, as seen in the AlO_x nanolayers. 179
A7 Estimated D_{it} and Q_f from as deposited SPV. Black lines show the CDP_{dark} values superimposed on the SPV graph. 179
A8 Extraction of J_0 values from fitting of τ_{eff} curves for a) a)10 cycles AlO_x, b) RCA+10AlO_x c) RCA+5AlO_x with negative corona d) RCA2+10AlO_x with negative corona. 181
A9 Extraction of J_0 values from fitting of τ_{eff} curves for a) UV-O3 SiO_x/poly-Si b) RCA2+SiN_x/poly-Si. The automatic fitting of τ_{eff} for the RCA+SiNx gave an unrealistic value of J_0 so manual fitting of the τ_{eff} was carried out. The manual fitting shows good agreement for the τ_{eff}, S_{eff} and J_0. The J_0 value quoted is taken at 2×10^{15} cm^{-3}, the minimum point on the S_{eff} curve. 182
A10 Contact resistivity of Dielectric/poly-Si structures with and without an HF dip to remove native oxide from the poly-Si and with contact firing. 183
A11 G-V measurement of 3 s SiN_x poly-Si structure. A high conductance is seen in at all voltages due to the high density of holes at both the Si/dielectric and dielectric/poly-Si interfaces. 184
A12 XPS data for P1-5m a) Si2p peak b) VBO 185

A12 XPS data for SiO_x a) P1-5m Si2p peak b) P1-5m O1s peak c) 10 s RTO SiO_x Si2p peak d) 10 s RTO SiO_x O1s e) 100 nm SiO_x Si2p f) 100 nm SiO_x O1s peak g) 100 nm SiO_x VBO. 187
A12 TSK XPS data for SiN_x a) P1-5m Si2p peak b) P1-5m N1s peak c) P1-5m annealed Si2p peak d) P1-5m annealed N1s peak e) P1-10 5s SiN_x annealed Si2p peak f) P1-10 5s SiN_x annealed N1s peak g) Bulk SiN_x Si2p peak h) Bulk SiN_x N1s i) Bulk SiN_x VBO 189
A13 PhiV XPS data for a),b),c) bulk SiN_x and d),e),f) spluttered bulk SiN_x 190
A14 XPS data for a),b),c) bulk AlO_x and d),e),f) spluttered bulk AlO_x 191
A14 XPS data for thin AlO_x films on P1-10. a)-c) 30 cycles, d)-f) 20 cycles g)-i)10 cycles j)-l) RCA2+5 cycles 193
A15 XPS peaks for TiO_x a) pALD Ti2p peak b) tALD Ti2p peak c) pALD O1s peak d) tALD O1s peak e)pALD Si2p peak f) tALD Si2p peak 194

List of Tables

1.1 PV technologies . . . 4

2.1 A selection of the best surface passivation achieved on n and p-type Si. . . . 16

3.1 Wafer Groups . . . 31
3.2 Standard operating parameters for PECVD SiN_x, SiO_x and poly-Si . . . 33
3.3 Standard deposition parameters for ALD AlO_x . . . 33
3.4 Standard operating parameters for RIE of poly-Si . . . 35

4.1 Literature Values of band offset parameters and effective mass. . . . 52
4.2 Values used for simulations. . . . 52
4.3 Default Values for Sentaurus Simulations . . . 54

5.1 Summary of analysis techniques used in this chapter . . . 66
5.2 XPS Values for SiO_x VBO determination. . . . 82
5.3 XPS Values for SiN_x VBO determination . . . 84
5.4 XPS Values for AlO_x VBO determination on P1-10 wafers. . . . 87
5.5 XPS Values for Simulations and Theoretical Fitting . . . 90

7.1 Fitted Q_f and D_{it} from C-V of RCA2 SiO_x . . . 108
7.2 Fitted Q_f and D_{it} from C-V of SiN_x and RCA2+SiN_x stacks . . . 114
7.3 Fitted Q_f and D_{it} from C-V of AlO_x and RCA2+AlO_x stacks . . . 118

8.1 Fitted t_{diel}, ϕ_b and N_{pin} for poly-Si contact structures . . . 132

A1 Standard Modelling Parameters for SPV Fitting. . . . 178

Chapter 1

Introduction

1.1 Climate Change

Since the industrial revolution, fossil fuels have been used as a source of energy. Coal, oil and natural gas have been used to heat homes, power factories, and fuel cars, leading to huge advancements in science and technology in the 200 years since. However, fossil fuels are made up of hydrocarbons, which, when burnt, release CO_2 into the atmosphere. In addition, impurities and incomplete combustion emit other gases such as CO and CH_4. The burning of fossil fuels has released vast quantities of CO_2 into the atmosphere [9]. Figure 1.1(a) plots the increase in atmospheric CO_2 since 1880. CO_2 absorbs energy at the same wavelength as the infrared radiation emitted from the Earth's surface [10]. Therefore, the increase in CO_2 concentration causes an increase in heat absorbed by the atmosphere. This trapped heat accumulates over time, leading to what is known as the greenhouse effect. CO_2, and other gases with similar absorption peaks, are termed greenhouse gases. The greenhouse effect has caused a rise in the mean temperature of the Earth and is plotted in Figure 1.1(b). To emphasise the human-induced warming above the natural variation in the Earth's temperature, the total incident irradiance is added for comparison. The divergence of these two curves around 1980 shows the warming due to human behaviour, which coincides with the sharp increase in CO_2 concentration in Figure 1.1(a).

The 2015 Paris Climate Agreement set to limit global warming to 'well below 2 °C' [13]. To prevent a continued temperature rise, the trend in CO_2 concentration in Figure 1.1(a) must be reversed. Many governments have now set out targets to reach 'net zero', where the volume of CO_2 emitted is equal to that absorbed or captured. To achieve this, the emission of CO_2 must be drastically reduced by replacing electricity production using fossil fuels with low carbon alternatives, while simultaneously electrifying other sectors such as transportation and heating [14]. An additional means to achieve net-zero is through carbon capture and storage, however, the technology is currently immature so it is unlikely to provide a significant contribution by 2050 [15].

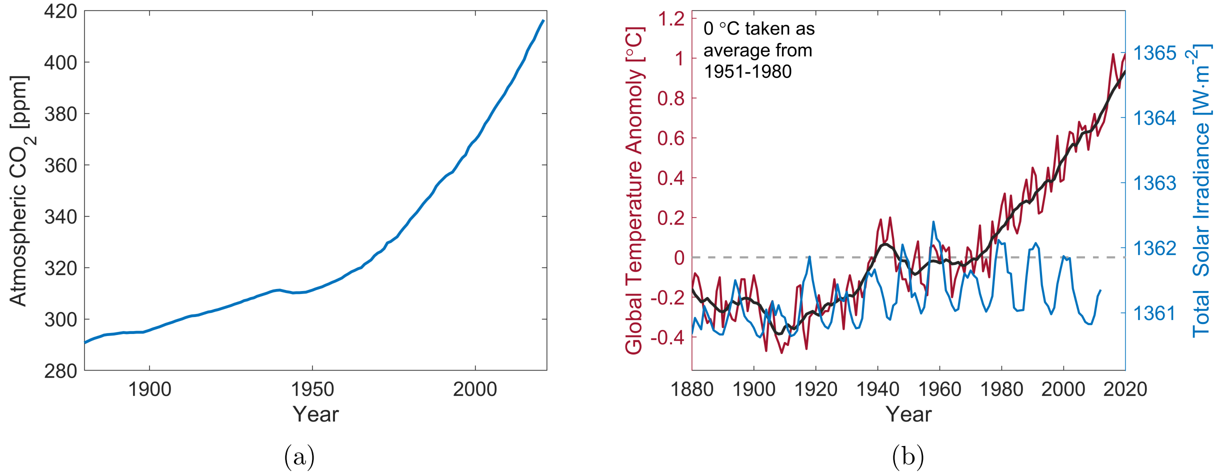


Figure 1.1: a) Change in atmospheric CO_2 concentration since 1800 b) Change in the Earths mean temperature compared to solar irradiance since 1880. Data from GISS NASA [9], GISTEMP[11], NOAA [9], [12]

1.2 Renewable Electricity Generation

To remove the greenhouse gas emissions from electricity production, there must be a transition to clean electricity generation [16]. In 2021, 61% of electricity production was generated by fossil fuels while hydroelectric, wind and solar power combined accounted for 25% [17]. Figure 1.2(a) shows the electricity production from all renewable sources. Currently, hydroelectric power dominates renewable production, however wind and solar are increasing capacity at a significantly higher rate. To replace fossil fuel electricity production entirely, solar energy must play a leading role. The reason for this is highlighted in Figure 1.2(b). The available capacity of solar far exceeds all other sources combined, with over 1000×more capacity than required to power the world.

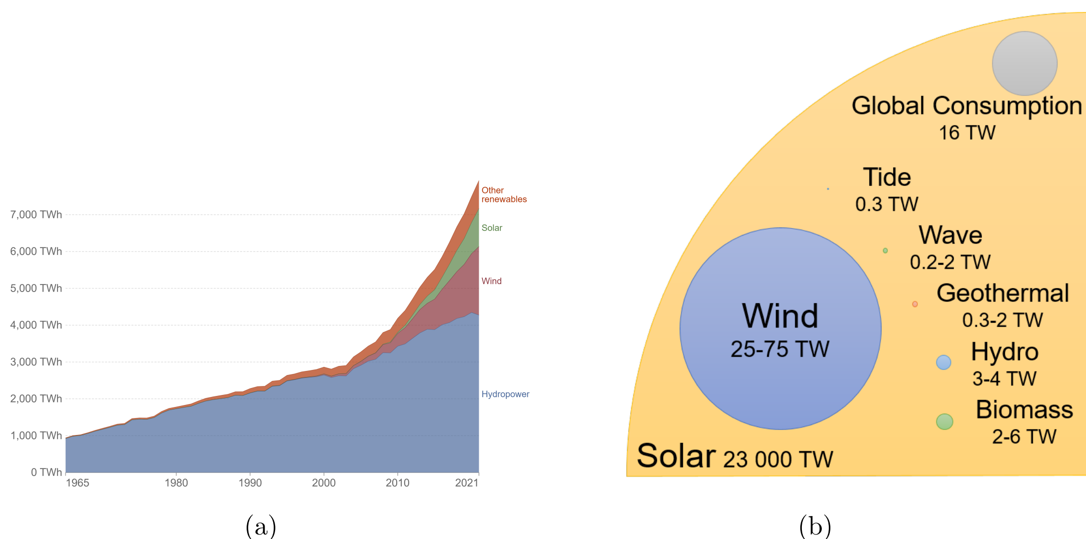


Figure 1.2: a) TWh of energy produced per year for main renewable sources [18] b) Yearly availability of renewable energy sources compared to the annual global electricity demand. From Our world in data. Data from BP statistical review of world energy (Areas of the full circle are to scale). Adapted from [19]

The power generated by solar panels will vary with the time of day and calendar month. Therefore, once a substantial proportion of the grid is supplied by solar energy, excess energy generation in the daytime and summer months must be stored for use when generation is lower. Batteries are one option for energy storage, but many batteries use precious materials which limit their capacities for grid storage. Some more novel solutions include off-river pumped hydro [20], electrolysis of hydrogen [21] or thermal storage [22].

1.2.1 Solar Electricity Generation

So far, there has been 1 TW of cumulative solar power capacity deployed worldwide [23]. In 2022 268 GW was installed, now exceeding wind installations [24]. Compared to 50 GW of installations in 2015, the increased pace of solar deployment is evident. A reason for this is the learning rate of cost of producing a solar photovoltaic (PV) module [25]. The levelised cost of energy (LCOE) of solar energy has dropped from 0.4 $/kWh in 2010 to 0.05 $/kWh in 2020 [26]. The decrease is due to improvements in cell efficiency and a streamlined manufacturing process as PV mass production took off. This compares to fossil fuels, which recently increased to around 0.25 $/kWh [26], making solar power economically favourable as well as being a clean energy source.

1.3 Photovoltaic Cell Materials

There are many materials that can act as the absorber in a PV cell. The key requirement is for it to have a band gap with an energy similar to the energy of the solar spectrum. The optimum band gap is a trade-off between a low band gap, which can absorb a large proportion of the solar spectrum but provides little potential energy, and a high band gap that can extract more energy from the high energy photons but is transparent to a large proportion of the incident light. This is known as the Shockley-Queisser Limit [27] and it has been found that the optimum band gap for the air mass (AM) 1.5 spectrum is 1.34 eV, which can achieve 33.16% efficiency [28].

Photovoltaic technologies can be split into five groups: silicon, thin film, organic, perovskite and III-Vs. Silicon has a fixed band gap of 1.12 eV, close to the optimum, while other material classes enable the band gap to be tuned. An ideal solar cell requires high efficiency, large-scale production at low costs, and stable efficiency for many years. Table 1.1 summarises the key features of each class of PV materials. Currently, only Si cells meet all criteria, and hence they dominate the market, accounting for >90% of industrial PV modules [29].

Table 1.1: PV technologies

Technology	Record Efficiency	Stability	Cost
Silicon	26.8 [30]	High (30+ years)	cheap
Thin Film (CdTe)	23.3 [31]	moderate	cheap
Organic	18.2 [30]	poor	cheap
Perovskites	25.7 [30]	months	cheap
III-Vs	29.1 [31]	high	expensive
Tandem structures	33.2[a] [32]	months[a]	cheap[a]
	38.8[b] [31]	high[b]	expensive (very)[b]

[a] Si/Perovskite, [b] III-Vs

1.4 Scope for Improvements in Silicon Solar

Higher-efficiency solar panels increase the power output per cell and per m^2, allowing more power to be generated from a finite area, e.g. residential roof space, and reducing the infrastructure costs such as mounting and electrical inverters. In addition, PV must be deployed in large volumes and at low cost, so efficiency gains must be realised via techniques and materials suitable for industrial production at competitive prices.

1.4.1 Efficiency

The theoretical maximum efficiency for single junction Si solar cells is 32.2% [28]. Though this is reduced to 29% once intrinsic recombination processes are considered [33]. To reach the theoretical efficiency, first, all photons incident on the cell must be absorbed in the silicon. The silicon surface is highly reflective, so an anti-reflection coating and textured surface are used to increase light trapping. A pyramidal structure and anti-reflection coating results in absorption of >98% of incident light [34]. The absorbed photon generates an excited electron-hole pair. The electron and hole are charge carriers and must be extracted to separate contacts. Defects can trap the charge carriers, preventing them from reaching the contact. Therefore defects must be minimised to maximise the cell efficiency.

The Shockley-Queisser limit can be surpassed by multi-junction tandem cells. Tandems stack two (or more) cells on top of each other to enable a higher proportion of the solar spectrum to be utilised. A high band gap material is used in the top cell and a lower energy band gap for the bottom cell. The top cell absorbs the high-energy photons, while lower-energy photons, which are transparent to the high band gap material, can be absorbed by the bottom cell.

1.4.2 Sustainability

Forecasters predict >70 TW of PV capacity is needed by 2050 to reach net-zero targets [35], [36]. In 2022, a cumulative capacity of 1 TW was reached. For 70 TW, the annual production of PV modules must increase from 250 GW/year to 2-3 TW/year. To achieve this, sufficient material abundance for solar panel production is vital. Silver and indium are currently used in solar cells, however, the global supply is insufficient for TW-scale production. Silver is used for the metal contacts and PV already accounts for ∼10% of the total annual silver production [37]. In addition,

the new, higher efficiency structures use a higher proportion of Ag [38]. While silver production could increase, it is generally accepted that alternatives to silver contacts must be adopted [38]. Indium is used in transparent conductive layers (TCLs). It is the higher efficiency cells which require TCLs and so far only 0.7 GW of power is produced however there is 40-50 GW of planned capacity which would use ∼10-20% of the annual indium supply [37]. Indium-free TCLs and silver free contacts are thus key areas of research for silicon PV [39], [40].

1.5 Passivating Contacts

As mentioned in Section 1.4.1, minimising the defects is crucial for maximising the efficiency of silicon photovoltaics. The silicon-metal interface has a high density of defect states that lead to electron-hole recombination at the contacts. The contacts are currently a major source of power loss in industrial solar cells [41]. To minimise contact recombination, the area of the Si-metal interface can be reduced, as is the case in a currently mainstream Passivated Emitter and Rear Cell (PERC) structure. In industrial PERC the metallisation fraction is only ∼ 3% [42], however, this still dominates recombination losses. Engineering constraints such as the minimum contact width and cell series resistance prevent the contact area from being further reduced.

To increase the efficiency of solar cells, the contact can be 'passivated', i.e. the highly defective Si-metal interface is removed. Additional layers are inserted between the silicon and the metal to provide the passivation. The layers must be conductive to avoid an increase in the series resistance (R_S). In an ideal cell, one contact is optimised for electron collection and the other is optimised for holes. There are three main categories of passivating contacts: Silicon heterojunction (SHJ), poly-Si based contacts (Tunnel Oxide Passivated Contacts (TOPCon) or Poly-Si on Oxide (POLO)), and dopant free passivating contacts (DFPC). SHJ contacts have achieved the highest efficiency obtaining the world record 26.8% cell with electron and hole selective SHJ contacts [30]. Poly-Si contacts are formed of a 1-2 nm SiO_x layer and a highly doped poly-Si capping layer. This structure has proved effective as an electron contact, reaching cell efficiencies of 26% [43]. The efficiency could be increased further if the poly-Si electron contact was combined with a highly passivating hole contact [44]. However, poly-Si hole contacts have been less effective, partly due to the lower conductivity of holes through the SiO_x passivation layer, and partly due to a non-optimal doping profile for boron, which reduces the passivation quality. A detailed comparison of electron and hole poly-Si contacts is given in Section 2.9. Substantial efforts to improve hole contacts are being made, with one approach focused on the replacement of silicon oxide with an alternative dielectric. The new material can have a higher hole conductivity and a more optimum dopant profile. The presence of a fixed negative charge could also increase the conductivity and improve the passivation.

Combining electron and hole poly-Si or SHJ contacts to create a double-sided cell has some limitations due to parasitic absorption in the poly-Si or a-Si at the front side of the structure. This can be avoided by creating an interdigitated back contact (IBC) structure, however, complex processing makes it costly for industry. An alternative solution is to use a DFPC as the front contact. DFPCs do not have a parasitic poly-Si or a-Si layer, and it is the primary advantage of this cell structure. So far, the contact resistivity and recombination at DFPC interfaces are higher than poly-Si or SHJ contacts, with a maximum efficiency of 23.8% [45] reported for DFPCs.

Understanding the interface between the silicon and dielectric in more detail can help improve

passivating contacts. The primary methods of analysis involve contact resistivity and lifetime measurements to determine the contact parameters, and the efficiency of full cells is then compared to an unpassivated reference. Obtaining more information on the passivation and transport mechanisms at the Si/dielectric interface can guide future research. This is particularly important for novel materials as the passivisation mechanisms at the Si interface are less well understood. However, the high conductivity of nanolayer dielectrics poses challenges for interface characterisation. New techniques must be developed to analyse the interfaces in passivating contact structures.

1.6 Aims and Objectives

This thesis aims to develop novel hole-selective contacts that improve on the current SiO_x poly-Si contacts. The overall aim is split into four parts:

1. Utilise advanced simulations to understand the effect of the band structures, dielectric charge, and doping profiles in passivating contact structures.
2. Develop fabrication processes that enable deposition of uniform, nanolayer AlO_x and SiN_x and determine the key physical properties of the nanolayers for passivating contacts.
3. Understand the carrier transport and passivation properties of nanolayer SiN_x, AlO_x and TiO_x to assess their potential in hole selective contacts. The properties of the dielectrics are measured individually and integrated into a poly-Si contact stack.
4. Develop techniques for characterising the interface properties of passivating contact structures. Using analysis of SPV, C-V and G-V measurements to enable extraction of D_{it} and Q_f values at the Si/Dielectric interface.

1.7 Structure of this thesis

This thesis is split into three sections. The first section contains the Literature Review and Experimental Methods. The Literature Review consists of the key semiconductor theory, on which the simulation and characterisation techniques are based, and a detailed review of the latest work on passivating contacts to provide context and motivation for the research carried out. The second section contains the main results chapters, Chapters 4 to 8, and the final section summarises the conclusions and future work, Chapter 9.

The results chapters cover each aspect of the nanolayers in passivating contacts. Chapter 4 contains TCAD simulations and theoretical calculations which set out the motivation for implementing SiN_x and AlO_x as replacements for SiO_x in hole selective contacts. Chapter 5 details the fabrication and material properties of the nanolayers and Chapter 6 measures the conductivity of the nanolayers. Chapter 7 first introduces two novel methods for analysing the Si/dielectric interface of conductive dielectrics, then applies the techniques to nanolayers. Finally, SiN_x and AlO_x poly-Si contacts are fabricated in Chapter 8.

Chapter 2

Literature Review

This review gives a broad overview of the key physical principles governing the contacts of silicon solar cells and then covers the state of the art passivating contact technologies.

2.1 The Metal/Semiconductor (MS) Interface

2.1.1 Ideal Interfaces

When a semiconductor and metal come into electrical contact charge may pass between the metal and semiconductor. At equilibrium, under no applied bias, the interface will have a neutral charge and the fermi level will be constant. Figure 2.1(a) illustrates the case of an n-type Si in contact with a metal that has a higher work function. Electrons flow from the Si to the metal so that the two sides of the junction reach equilibrium with no final net flow, and a constant Fermi level across the junction. Far from the interface, the metal work function (Φ_M) and the electron affinity (χ) of the semiconductor will retain the values of the isolated materials, therefore the balancing of charge must happen near the interface. The electrons flowing to the metal cause a depletion of electrons at the semiconductor surface, resulting in band bending (there is no band bending in the metal due to the high density of available states at each energy level). This is a Schottky barrier and the ideal Schottky barrier height (ϕ_b) is given as $\Phi_M - \chi$ for an n-Si substrate and $E_g - (\Phi_M - \chi)$ for a p-Si substrate. E_g denotes the band gap of the semiconductor.

2.1.2 Real Interfaces

At the surface of a semiconductor, the crystal lattice structure is interrupted, which introduces defect energy states in the band gap. Defect states are acceptor or donor like. Donor states have neutral charge when filled and a positive charge when empty. Acceptor states are neutral when empty and negative when occupied. The neutral level (ϕ_0) in the semiconductor band gap is the energy at which, on average, all the acceptor sites are filled, and all donor states are empty. When the Fermi level of the semiconductor is either above or below the neutral level, the surface becomes negatively or positively charged, respectively. The charge density of the surface states (Q_{it}) depends on the density of defect states, D_{it}, and is given by [46]:

$$Q_{it} = -qD_{it}(E_g - q\phi_0 - q\phi_b). \tag{2.1}$$

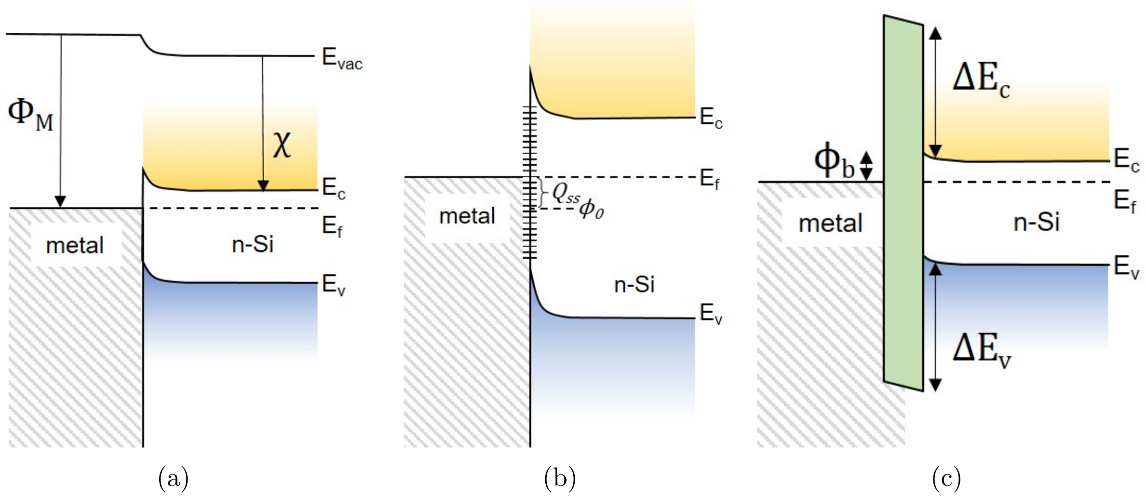


Figure 2.1: a) ideal MS contact b) real MS contact c) real MIS contact

Figure 2.1(b) shows these energy values on the band diagram. In the case of a metal-semiconductor (MS) interface, the defect states and their charge can influence the height of the Schottky barrier. When the defect density is high, the barrier height is dictated by the interface charge neutrality level and the Fermi level is pinned, irrespective of Φ_M. $D_{it} = 0$ represents the ideal case where the barrier height is the difference between Φ_M and χ. Most MS contacts fit an intermediate regime. In the case of silicon-metal contacts the D_{it} can be $4{\times}10^{13}$ cm^{-2}/eV and the charge neutrality level is ∼0.2 eV below the intrinsic energy level, giving a strong pinning force [46]. The presence of interface states increases ϕ_b compared to the ideal value. On bare p-type Si ϕ_b is 0.85 eV for an aluminium contact, while the higher work function of gold results in a smaller ϕ_b of 0.34 eV [47].

2.1.3 Metal-Insulator-Semiconductor (MIS) Contact

Real contacts often feature an insulator between the semiconductor and metal. This could be unintentional i.e. in the case of a native oxide forming, or a purposefully grown layer e.g. the thin tunnelling oxide inserted underneath the metal contacts in bipolar transistors [48]. The insulator passivates some of the defects at the interface, lowering ϕ_b. However, insulators are not classically conductive, due to a large energy barrier to the Si. Provided the insulator is sufficiently thin, a low resistivity contact can be maintained with the carrier transport across the junction dominated by direct quantum tunnelling. The direct tunnelling current through a metal-insulator-semiconductor (MIS) contact is derived in Appendix A.

2.2 Recombination

Recombination in a solar cell is one of the key loss mechanisms that can limit the efficiency. It is the process where an excited electron in the conduction band combines with a hole in the valence band. The energy gained by the electron when the photon was absorbed is lost as heat or light. As the charge carriers did not reach the external circuit, no power was generated. Therefore, to maximise the efficiency of solar cells, recombination must be minimised.

2.2.1 Types of Recombination

There are three main types of recombination that occur in semiconductors: Radiative, Auger and trap-assisted or Shockley-Read-Hall (SRH). Figure 2.2 depicts the mechanism for each. Radiative recombination is the direct recombination of an electron in the conduction band with a hole in the valence band, releasing a photon with an energy similar to the band gap. The recombination rate depends on the concentration of electrons and holes and thus depends on the excess carrier density (Δn), and the band structure of the semiconductor. The indirect band gap of silicon significantly reduces the probability of radiative recombination. The radiative recombination rate for silicon is $R = 1.1 \times 10^{-14} \cdot np$ [49], where n and p are the concentration of electrons and holes, respectively.

Auger recombination involves three carriers. As with radiative recombination, an electron and hole directly recombine, but instead of the energy being released as a photon, it is given to another carrier. This carrier is excited to a higher state in the conduction band and then relaxes back to the conduction band edge through thermalisation processes. Auger recombination requires either two electrons and a hole or two holes and an electron. The extra carrier involved means the recombination rate is dependent on the doping concentration or injection level in the semiconductor.

The radiative and Auger recombination rates are intrinsic material properties. The final recombination mechanism, SRH recombination, is an extrinsic recombination process dependent on the defect concentration in the semiconductor crystal. In SRH recombination, an electron (hole) gets trapped in a defect state in the band gap, then a hole (electron) arrives and combines with the trapped carrier. The defects responsible for SRH recombination can be present in the bulk, or at the semiconductor surfaces. Defect states close to the middle of the band gap are the strongest recombination centres and thus can be the most detrimental to PV devices [6]. Dopant atoms generate defect states very close to the band edges, so are weak recombination sites. Passivation of defects to reduce SRH recombination is discussed in Section 2.3.

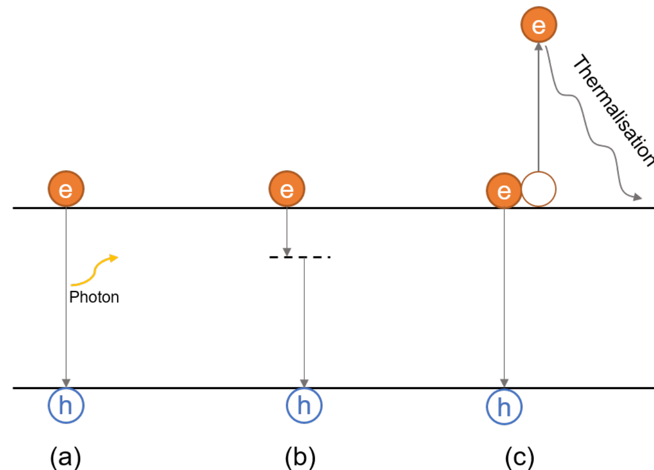


Figure 2.2: Types of recombination in semiconductors. a) Radiative, b) Shockley-Read-Hall, and c) Auger Recombination

2.2.2 Recombination Parameters

Characterising the recombination in PV devices is important for understanding and improving device performance. The most common method for measuring the recombination is using the photo-conductance decay method developed by Sinton Instruments [50]. The photo-conductance technique measures the effective minority carrier lifetime of a sample, τ_{eff}. The resulting data can be further analysed to give the surface recombination velocity, the dark saturation current, J_0, or the implied open circuit voltage, iV_{OC}. The following sections summarise these recombination parameters, which are described in detail by McIntosh and Black [51] and Bonilla et al. [52].

2.2.2.1 Lifetime

The effective lifetime gives the average time an electron will remain in the conduction band after excitation from a photon. A flash of light incident on the sample will generate carriers in the sample, and then the τ_{eff} is determined by [52]:

$$\tau_{eff} = \frac{n(t)}{G(t) - \frac{dn(t)}{dt}} \tag{2.2}$$

Where n is the carrier density, G is the generation rate and $\frac{dn}{dt}$ is the recombination rate. The effective lifetime has combined contributions from each of the recombination mechanisms previously stated. These can be combined into contributions from the bulk, τ_b and the surface, τ_s,

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}, \tag{2.3}$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{aug}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_s}. \tag{2.4}$$

When determining the surface recombination parameters, high-quality silicon wafers are used, with few impurities, thus the SRH contribution to τ_b can be neglected [53]. τ_{eff} is dependent on the thickness and bulk properties of the wafer. Thus, the surface recombination velocity (SRV) or dark saturation current (J_0) are preferred for comparing the surface passivation measured across different wafers. The determination of effective lifetime is more straightforward, so is used to compare samples on the same substrate.

2.2.2.2 Surface Recombination Velocity

The effective surface recombination velocity (SRV) directly relates to the recombination rate at the surface, U_s [51],

$$SRV = \frac{U_s}{\Delta n_d} = \frac{(n_s p_s - n_i^2)}{\Delta n_d} \int_{E_v}^{E_c} \frac{dE}{(n_s + n_i)/S_{p0} + (p_s + n_i)/S_{n0}}. \tag{2.5}$$

n and p are the density of electrons and holes. The subscript s refers to the values at the semiconductor surface, d refers to the edge of the space charge region and i is the intrinsic density.

The key parameters of S_{n0} and S_{p0} are determined by the defects at the interface,

$$S_{n0} = \nu_{th} D_{it}(E) \sigma_n(E), \tag{2.6}$$
$$S_{p0} = \nu_{th} D_{it}(E) \sigma_p(E). \tag{2.7}$$

where ν_{th} is the thermal voltage, D_{it} is the defect density and σ is the capture cross-section of either electrons (subscript n) or holes (subscript p). D_{it}(E) is not evenly distributed over the band gap energies. There is typically a minimum value near the mid-gap and increasing density towards the band edges. For σ(E), the defects near the mid-gap are the most active recombination centres so the capture cross section is larger, while defect states near the band tails are ineffective recombination centres. The capture cross-section of electrons is larger than that of holes, so SRV is typically larger when electrons are the minority carriers, as this limits the recombination.

The surface lifetime can be used to determine SRV experimentally. SRV combines τ_s with the wafer thickness, t_{waf}, and the diffusion length, D,

$$SRV = \sqrt{D\left(\frac{1}{\tau_s}\right)} \cdot \tan\left(\frac{t_{waf}}{2}\sqrt{\frac{1}{D}\left(\frac{1}{\tau_s}\right)}\right). \tag{2.8}$$

When SRV is sufficiently low tan(x)≈x, and S_{eff} can be approximated as:

$$SRV = \left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_b}\right) \cdot \frac{\mathrm{t}_{waf}}{2}. \tag{2.9}$$

The SRV indicates the recombination rate at the surface of the semiconductor. It removes the contribution of the wafer bulk to the recombination in the sample to give the contribution of surface recombination to the overall passivation of the wafer. A low SRV value indicates a highly passivated surface. This enables the quality of the surface passivation for two different wafers to be compared.

2.2.2.3 Dark Saturation Current

The dark saturation current, J_0, is another recombination parameter often used to assess the passivation quality of a semiconductor surface. It is equal to the dark current under reverse bias [54] and can be in the fA/cm^2 range for a highly passivated silicon surface. J_0 can be calculated from lifetime measurements [52] and is given by,

$$J_0 = \frac{d}{d\Delta n}\left(n_{i,eff}^2 \cdot \sqrt{D\left(\frac{1}{\tau_s}\right)} \cdot \tan\left(\frac{\mathrm{t}_{waf}}{2}\sqrt{\frac{1}{D}\left(\frac{1}{\tau_s}\right)}\right)\right) \tag{2.10}$$
$$J_0 = \frac{d}{d\Delta n}\left(n_{i,eff}^2 \cdot S_{eff}\right) \tag{2.11}$$

It can be split into contributions from the front and rear sides, or from passivated and contacted regions.

2.2.2.4 Implied Open Circuit Voltage

The final recombination parameter frequently used is the implied open circuit voltage, iV_{OC}. The implied open circuit voltage gives the maximum V_{OC} possible without any drop due to resistive losses or contacting [55]. This can be a useful quantity for estimating the cell parameters if the structure was implemented into a full device. Comparing the V_{OC} of a full cell to a measured iV_{OC} can indicate the quality of the contacts in the full cell. iV_{OC} is extracted from the injection-dependent photo-conductance measurements [56] via:

$$iV_{\mathrm{OC}} = \frac{kT}{q}\ln\left(\Delta n\left(\frac{N_A + \Delta n}{n_i^2}\right)\right) \tag{2.12}$$

The iV_{OC} is dependent on the injection level and is generally quoted for 1 Sun conditions. This requires Δn to be converted to the equivalent Suns, which depends on the generation of carriers in the wafer. Hence, the wafer thickness and the sample optical properties are important input parameters.

2.3 Passivation

2.3.1 Bulk

Impurities in the Si can provide recombination centres in the bulk. Metals such as iron, chromium and nickel are some of the most harmful impurities, particularly when found as discrete atoms in interstitial or substitutional lattice sites [57]. They have energy states near the mid-gap of silicon, making them highly recombinative. Iron concentrations of only 4×10^{12} cm^{-3} can reduce the bulk lifetime to a few hundred microseconds [57]. The first method to minimise recombination is to limit the concentration of these impurities during Si crystal growth. Conveniently, the solubility limit of most impurities is significantly greater in liquid Si compared to the solid. Therefore, as the Si crystal is drawn out of the crucible, the impurities are segregated into the liquid. As the ingot is cast, and the volume of Si melt is reduced, the remaining liquid Si will have a higher concentration of impurities. There is, therefore, an increase in impurities in the final portion of the ingot, before the remaining liquid is discarded.

Gettering is a process to ensure the remaining impurity atoms in the Si are located far from the active regions of the device [58]. In many PV devices, the highly doped regions formed by high-temperature diffusion act as the gettering step, with a dual purpose of forming the p-n junction. The solubility limit is higher in heavily doped regions and the high temperature means metal impurities have high diffusivity [58]. The metal impurities become concentrated in the highly doped regions, where recombination is dominated by Auger recombination [58].

Finally, hydrogen can be incorporated into the silicon wafer. Hydrogen has a very high diffusivity in silicon and it can bond to many defects, passivating the mid-gap states. There are many different methods to incorporate hydrogen into the cell such as through a hydrogen-rich capping layer and firing [59], a forming gas anneal [60], a remote hydrogen plasma [3] or a shielded hydrogen plasma [61], [62].

2.3.2 Surface

As mentioned in Section 2.1.2, the silicon surface has a high density of defect states. The defect states have energy levels in the silicon band gap, so act as SRH recombination centres in a solar cell. To remove these defects, a dielectric layer is added to the Si surface to satisfy the dangling bonds at the silicon surface. This is known as chemical passivation. The degree of chemical passivation at an interface is characterised by the concentration of defects near the middle of the band gap. The most commonly used dielectrics for the passivation of silicon are silicon oxide, silicon nitride and aluminium oxide. As with bulk passivation, hydrogen treatments can provide additional passivation of surface defect states. Depending on the material and deposition technique, hydrogen may be intrinsically present, or it can be added extrinsically after deposition.

To complement chemical passivation, field-effect passivation (FEP) can further reduce the recombination at the interface. Often, an intrinsic charge in the dielectric provides FEP. The dielectric charge induces an image charge in the silicon. This forms an accumulation of one type of carrier at the interface, and depletion of the other, resulting in bending of the energy bands in the silicon at the interface with the dielectric. An electron and hole are required for recombination, so limiting one of these carriers will reduce the recombination rate. Figure 2.3 shows the band bending and surface states for an unpassivated silicon surface, a surface with chemical passivation, and a surface with chemical and field-effect passivation. The silicon is n-type with a pinned fermi-level, causing upward band bending at the bare Si surface. In Figure 2.3(c) a dielectric with positive charge is present. The holes are repelled from the interface and recombination is reduced. Figure 2.4 shows the typical levels of chemical and field-effect passivation for a range of surface passivation layers.

The minority carrier density at the interface can also be reduced by a high dopant concentration in the Si, limiting recombination. However, a high doping concentration throughout the wafer will

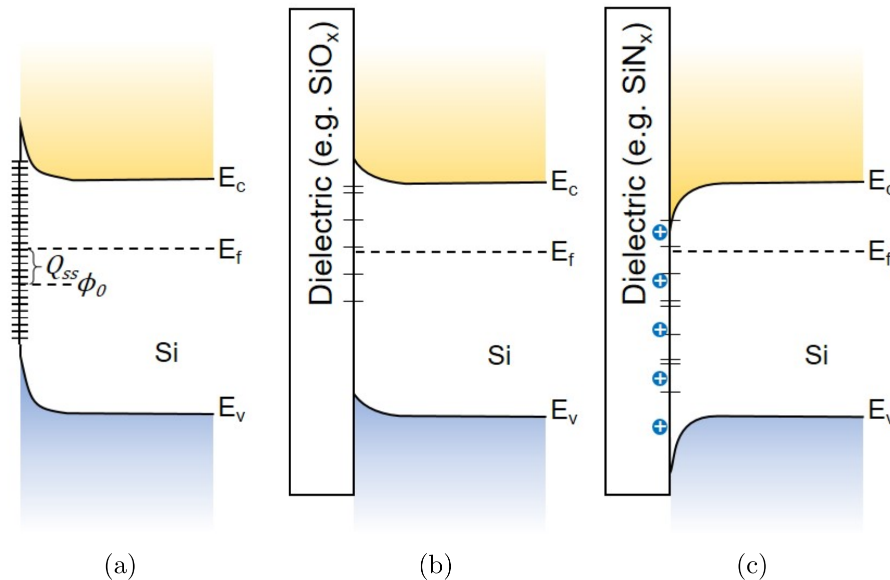


Figure 2.3: Schematic band diagrams of a) Unpassivated silicon surface with defect states b) silicon surface with chemical passivation and c) silicon surface with chemical and field-effect passivation

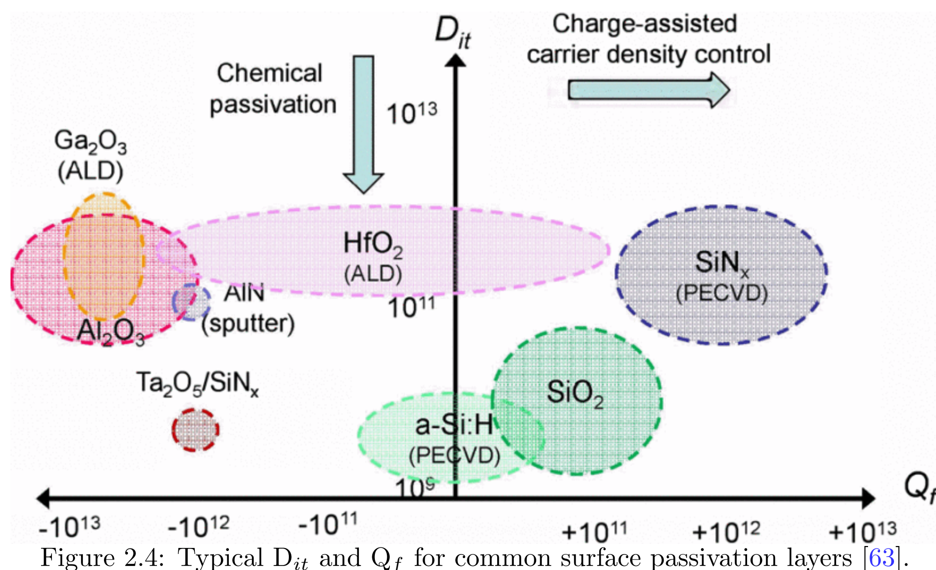


Figure 2.4: Typical D_{it} and Q_f for common surface passivation layers [63].

increase the Auger recombination. To overcome this, a diffusion can be carried out to increase doping only at the surface, while the rest of the wafer has a lower doping concentration. The doping profile also induces a built-in electric field near the silicon surface, further contributing to FEP.

The following sections give an overview of the literature on surface passivation using SiO_x, SiN_x AlO_x and TiO_x layers. The D_{it}, fixed charge density, Q_f, recombination parameters, and post-deposition treatments are discussed for each dielectric when implemented as a layer or stack for surface passivation. Amorphous silicon is another material used for surface passivation. It is not discussed in detail, but it can also provide excellent passivation, with SRV as low as 0.06 cm/s has been reported [64]. This stems from a very low D_{it}, as the fixed charge is negligible [63]. The disadvantages of a-Si are that post-deposition processes must be kept below <400 °C to avoid loss of surface passivation [65] and it has high absorption losses due to its direct band gap of 1.7 eV [66].

2.3.2.1 Silicon Oxide

Silicon oxide is the most extensively studied dielectric layer for surface passivation [52], [67]. It can either be grown into the silicon wafer via thermal [68], chemical [69], or anodic oxidation [70], or deposited via PECVD [71], [72] or ALD [73], [74]. As seen in Figure 2.4, SiO_x can achieve excellent chemical passivation, with D_{it} $\sim 10^{10}$ cm^{-2}/eV [75], [76]. To achieve this low D_{it}, a high-temperature step is required, to allow the bonds at the Si/SiO_x interface to rearrange, and additional hydrogenation [62], [77]. Table 2.1 shows the lowest SRV reported for SiO_x with optimised chemical passivation.

Figure 2.4 also shows that SiO_x has low intrinsic charge, $\sim +10^{11}$ cm^{-2}/eV [78]. To obtain the additional benefits of FEP to complement the excellent chemical passivation, external charge can be added to the SiO_x. Al Dhahir et al. [5] injected a high positive charge of 10^{13} q/cm^2 in thermal SiO_x via ion migration, while Hiller et al [79] used Al-doped ALD SiO_x to obtain a negative charge density of 5×10^{12} q/cm^2. SRVs of 0.17-0.44 cm/s have been reported for ion migration with additional hydrogenation [62], [80], [81]. FEP can also be achieved by adding a highly charged capping layer of SiN_x or AlO_x [52]. The SiO_x provides a low D_{it} at the Si surface and the capping

layer provides the high Q_f and often additional hydrogenation. These stacks are described in more detail in the SiN_x and AlO_x sections.

2.3.2.2 Silicon Nitride

Silicon nitride is typically deposited using Chemical Vapour Deposition (CVD) techniques such as Plasma enhanced CVD (PECVD) or Low-Pressure CVD (LPCVD), though it can also be deposited by atomic layer deposition (ALD). These techniques have many deposition parameters that, when altered, can have a significant influence on the D_{it} and Q_f at the Si/SiN_x interface. With most conditions SiN_x has a high intrinsic positive charge (1-7×10^{12} q/cm^2 [52]) and a moderate D_{it} (∼3×10^{11} cm^{-2}/eV [82]). It has a high concentration of hydrogen that can migrate during a firing step to passivate defects at the Si/SiN_x interface and in the silicon bulk.

The large, positive Q_f make SiN_x less suited for p-type passivation. However, through modification of the deposition processes, high levels of passivation have been achieved on p-type surfaces [82]–[86]. With optimisation of the SiN_x deposition for p-Si, Gatz et al. [85] achieved an SRV of 5.2 cm/s by fabricating a SiN_y/SiN_x double layer with a silicon-rich layer at the Si interface. Wang et al. [84] found that a post-deposition anneal at 450 °C generated a negative charge of 1.3×10^{12} q/cm^2 and low D_{it} of 3×10^{11} cm^{-2}/eV. Table 2.1 includes the lowest reported SRV for SiN_x layers. As mentioned in Section 2.3.2.1, SiO_x/SiN_x stacks can combine the properties of SiO_x and SiN_x [86]–[89]. Bonilla et.al. [87] achieved a very low SRV of 0.17 cm/s for a 100 nm thermal SiO_x + 70 nm SiN_x. The addition of an oxide layer is particularly advantageous for passivating p-type surfaces. The SiO_x provides a lower D_{it} interface and reduces the positive Q_f [86]. The benefits of silicon oxide and nitride have also been combined in SiO_xN_y layers. A double layer of SiO_xN_y/SiN_x proved effective on both n and p-type Si (SRV 1.35 and 2.85 cm/s, respectively) [90].

2.3.2.3 Aluminium Oxide

AlO_x is often deposited using ALD, a slow process (2 hours for a ∼20 nm layer), which makes it unattractive and costly for industrial application. However, the low D_{it} of $<10^{11}$ cm^{-2}/eV [91], [92] and a large, negative Q_f up to -10^{13} q/cm^2 [93]–[95], means it ideal for passivating p-type wafers. Therefore, despite the high costs, industry has started incorporating ALD passivation layers [96], [97]. The costs can be reduced by minimising the thickness and depositing in large batch processes.

An activation anneal between 300-500 °C is required to activate the beneficial negative charge and reduce D_{it} [91]–[93], [98]. Benick et al. [92] showed that the formation of the SiO_x interlayer during this anneal coincides with an increase in Q_f and a decrease in D_{it}. This, in combination with other works, show the $Si/SiO_x/AlO_x$ interface is key for the passivation mechanisms in AlO_x [99]. This is further corroborated by studies which show the negative charge to be largely independent of the AlO_x thickness [95], [100]. An SiO_x layer can be intentionally formed in SiO_x/AlO_x stacks to form a high-quality Si/SiO_x interface and minimise D_{it} at the Si surface [91], while the AlO_x layer provides negative charge and hydrogenation. The low SRV reported is included in Table 2.1.

2.3.2.4 Titanium Oxide

Titanium oxide is less commonly used as a surface passivation material compared to SiO_x, SiN_x and AlO_x. However, it has recently shown some promising results. It is deposited by either plasma

or thermal ALD [101]–[103], or APCVD [104], [105]. The charge is generally negative [102], [105], though a positive charge can be obtained with certain processing conditions [101]. The SRV is higher than the other dielectrics with 3.2 and 8.9 cm/s measured on n and p-type Si [102].

2.3.3 Contacts

Solar cells require contacts to extract the carriers and generate power in an external circuit. However, the silicon-metal interfaces have a high density of defect states of 4×10^{13} cm^{-2}/eV [107], which results in an SRV of over 10^5 cm/s and losses in the V_{OC} of cells. As with surface passivation, a combination of chemical and field-effect passivation can be utilised to minimise recombination at the silicon/metal interface. For contacts, the passivation must be achieved without a significant reduction in the conductivity across the interface. If the contact covers the full area of the cell, the resistivity must be below 100 $m\Omega\cdot cm^2$ [108] to prevent a detrimental increase in the series resistance of the cell. The thick dielectric layers used for surface passivation do not meet this requirement so alternative materials and processes are required. The different structures that have achieved the dual requirements of passivation and conduction are discussed in detail in the following sections.

Table 2.1: A selection of the best surface passivation achieved on n and p-type Si.

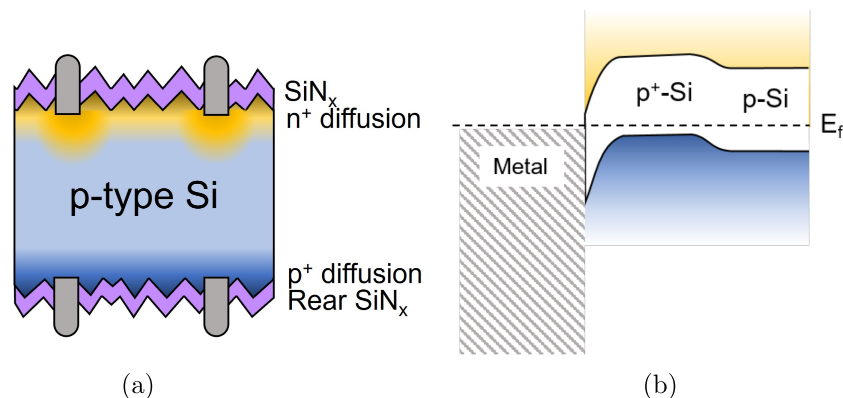
Dielectric	**Wafer** [type - Ω·cm]	**SRV** [cm/s]	**Reference**
SiO_x	n - 1.5	1.72	[77]
SiO_x	p - 1	7.01	[77]
SiN_x	n - 1	0.64	[106]
SiO_xN_y	p - 1	2.85	[90]
SiN_x	p - 0.85	1.6	[82]
AlO_x	n - 1	0.3	[91]
AlO_x	p - 1	0.3	[91]
TiO_x	n - 2.5	3.22	[102]
TiO_x	p - 2	8.91	[102]

2.4 Cell Contact Technologies

The contacting method that currently dominates industrial production is the Passivated Emitter Rear Cell (PERC). The cell surface is passivated with a thick dielectric stack (as described in 2.3.2) and local contacts are formed to minimise the area of the cell with high recombination. The PERC structure and the band diagram of the direct MS hole contact are shown in Figure 2.5. The contact area is dependent on the contact finger width and the contact spacing [8]. Screen printing is the main industrial technology due to its high processing speeds. Through optimisation of the screen printing process, contact fingers down to 30 μm can be produced [109], enabling PERC cells to reach efficiencies of 24.5% [110]. Despite the low contact area of 3% in optimised PERC cells, the very high $J_{0,c}$ of 800 fA/cm^2 [109] makes the metal contacts the largest source of recombination losses, limiting the efficiency of PERC cells [108]. To improve the efficiency of silicon PV cells, a number of different structures have been developed. The main groups of passivating contacts include: poly-Si based contacts, which are termed either Tunnel Oxide Passivated Contacts (TOPCon) or Poly-silicon on Oxide (POLO); Silicon Heterojunction (SHJ); and Dopant Free Passivating Contacts (DFPC).

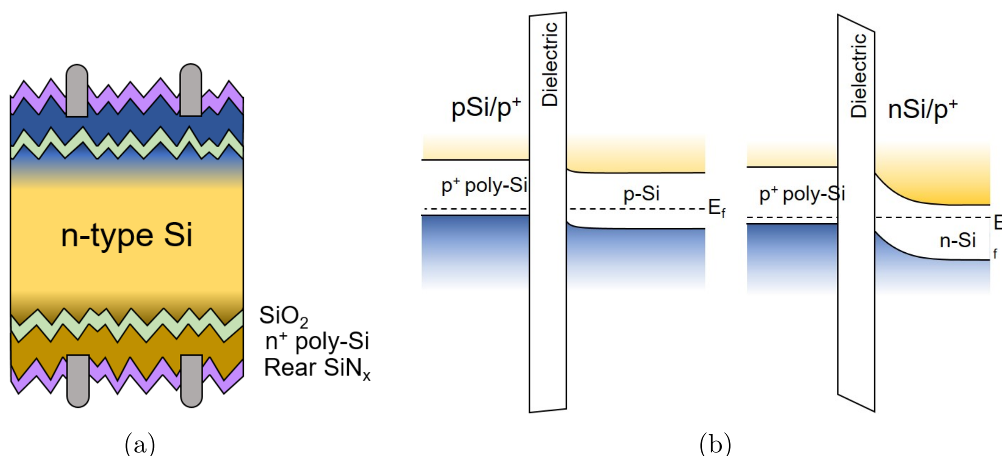
The poly-Si structures use a nanolayer dielectric to provide passivation, which is then capped with highly doped amorphous silicon. The structure is annealed at >800 °C to crystallise the amorphous Si and allow some diffusion of the dopants into the silicon. Figure 2.6 shows a schematic for a double-sided poly-Si cell and two possible band structures for a hole-selective poly-Si contact. Both electron and hole contacts can be fabricated with a poly-Si structure [111], and a base wafer of either polarity can be used. Industrial TOPCon cells have an n-type wafer with an electron-selective poly-Si contact and a boron emitter with local, unpassivated contacts. Cell efficiencies of 26% [43] have been achieved for this structure and the industrial market share is anticipated to surpass PERC in the coming decade [24]. Higher efficiencies have been achieved with both sides featuring poly-Si contacts [44], though the additional process complexity has so far limited industrial application.

Silicon heterojunction contacts use a thin intrinsic amorphous silicon layer to provide passivation with a highly doped amorphous Si layer on top. The lateral conduction provided by the doped layer is insufficient to prevent series resistance losses, so an additional transparent conductive oxide (TCO) layer is added. Figure 2.7 shows the cell structure and band diagrams of hole-selective SHJ contacts. A SHJ cell holds the record efficiency for a single-junction cell of 26.8% [30]. The



(a) (b)

Figure 2.5: a) Schematic of a PERC cell and b) Band Diagram of the PERC hole contact

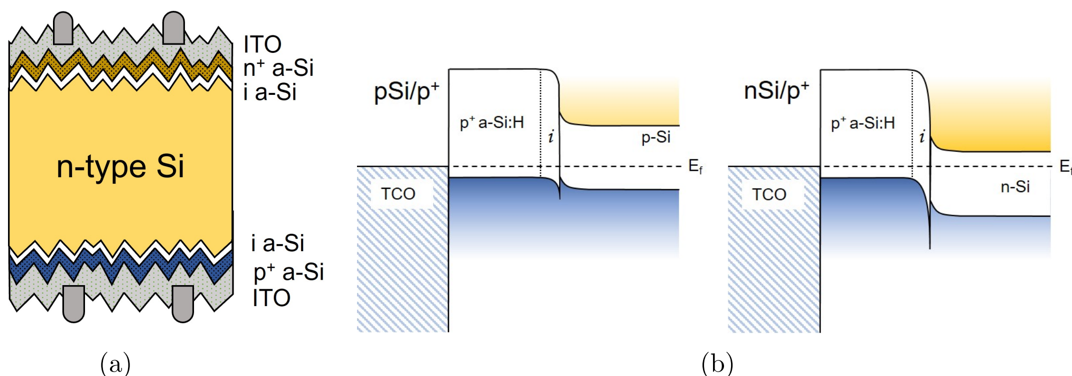


(a) (b)

Figure 2.6: a) Schematics of cell featuring electron and hole selective poly-Si contacts. b) Band Diagrams of hole selective poly-Si contacts on a p or n-type silicon substrate.

limitation of the SHJ design is parasitic absorption losses in the a-Si layers causing a reduction in short circuit current density (J_{SC}). High CAPEX costs have prevented wide-scale adoption in industry and the TCO layers are typically fabricated using indium tin oxide (ITO), which has potential sustainability issues (Section 1.4.2).

DFPCs look to reduce the absorption losses present in poly-Si and SHJ structures. Several transition metal oxides [112]–[114] and other novel materials [115], [116] have been investigated, due to their advantageous band offsets to silicon. The schematic of a DFPC in Figure 2.8(a) is similar to the SHJ structure with the a-Si replaced with the alternative materials. The band diagrams, however, are significantly different to the SHJ. Figure 2.8(b) and 2.8(c) show two possible band structures of DFPC hole contacts. In Figure 2.8(b) the valence band offset (VBO) is very small with a conduction band offset (CBO) of multiple eV. This allows high conductivity for the holes while the electrons are blocked. Alternatively, a material with the band gap entirely below the valence band (VB) of the silicon (such as MoO_x) can be used as a hole contact as shown in Figure 2.8(c). The conductivity is typically insufficient to provide lateral conduction to contact fingers so either a full metal contact or a TCO is required. DFPCs are often used to replace the front contact of a SHJ structure, to benefit from the lower absorption losses of the DFPC. So far the efficiency of



(a) (b)

Figure 2.7: a) Schematic of SHJ cell structure and b) Band Diagrams of hole selective SHJ contacts with an n or p-type silicon substrate.

DFPCs have reached 23.8% [45] for a hole contact and 23.1 [112] for an electron contact.

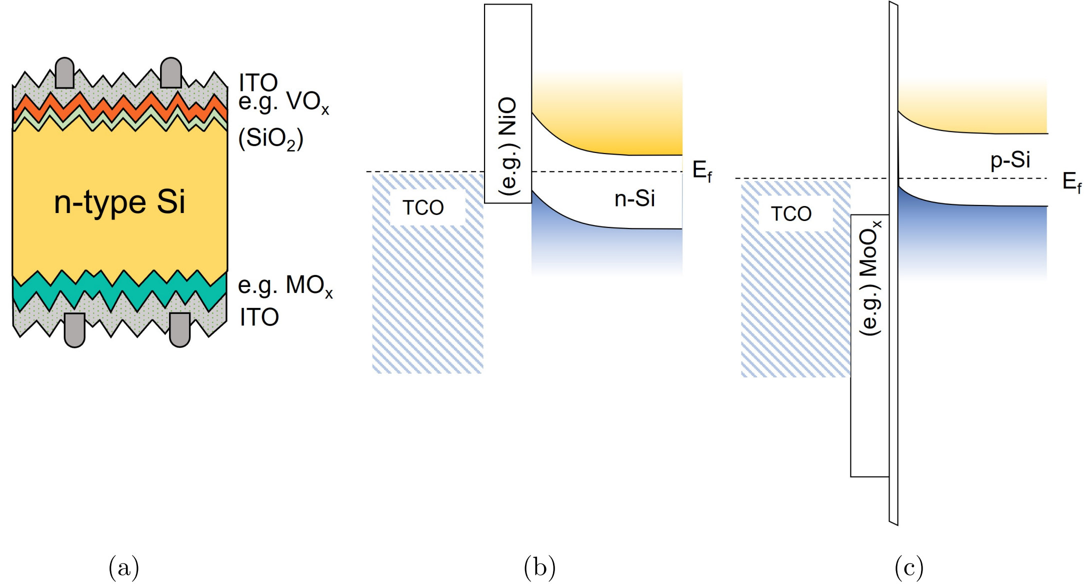


Figure 2.8: a) Schematic of DFPC cell structure and b) Band Diagram of DFPC low WF oxide on n-Si base wafer c) Band diagram of high WF metal-oxide with SiO_x interlayer, on p-Si wafer.

Finally, integrated back contacts, IBC, cells have both electron and hole contacts on the rear side of the cell. This has the key advantage that the front side is not metallised and therefore there are no shading losses. IBC cells can use any of the above contact technologies to optimise the contacts. Efficiencies of 26.1% [117] and 26.7% [31] have been reached with poly-Si and SHJ contacts respectively. The disadvantage of the IBC structure is the complex fabrication steps required to generate the patterning of the backside of the cell.

A comparison of the passivation and resistivity achieved for each of the contact technologies is summarised in Figure 2.9. An ideal contact will be in the bottom-left corner of the plot, with a low contact resistivity (ρ_c) and J_0. Poly-Si contacts show the highest potential efficiency, though this has not been realised experimentally. This may be due to difficulties optimising both the electron and hole contact in a full cell. DFPCs so far have the lowest idealised efficiency. The contacts typically show a trade-off between a low ρ or high passivation quality. The benefit of lower absorption losses in DFPCs is not seen in this plot as the idealised efficiency assumes perfect absorption.

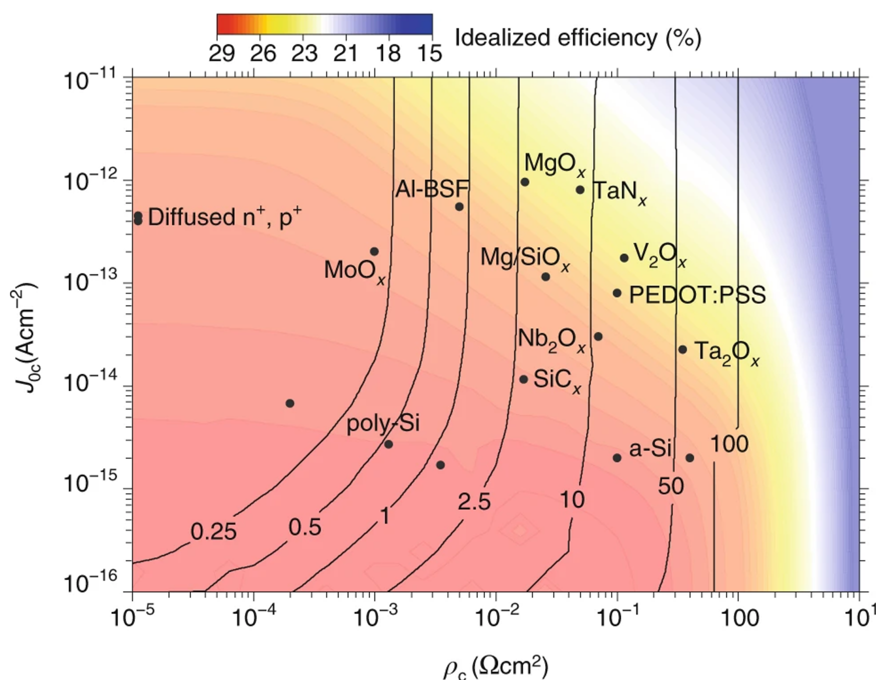


Figure 2.9: J_0 and ρ_c for a selection of passivating contact technologies. The black lines show the optimum contact area, as a percentage. The efficiency simulation is based on an idealised front contact, full area back contack and no absorption losses. Reproduced from [108].

2.5 Poly-Si Contacts using Silicon Oxide

As mentioned above, poly-Si contacts use a dielectric nanolayer and a highly doped poly-Si capping layer to provide high passivation and conductivity. Once integrated into a full cell, a SiN_x layer is added for anti-reflection and hydrogenation, and metal fingers provide conduction to the busbar. Figure 2.10 shows a cross-section of the poly-Si structure with the key properties and requirements of each component. The materials, deposition techniques and further processing will all influence the final device performance. These different features are described in detail in the following sections.

2.5.1 Silicon Oxide and Poly-silicon fabrication

There have been multiple methods of fabricating the oxide and the poly-silicon layers in TOPCon structures. The SiO_x layer needs to be thin, uniform and have good chemical passivation (after the high temperature anneal step). Many techniques have been attempted including wet chemical oxides [118]–[124], Thermal oxide [121], [124]–[127], PECVD SiO_x [125], ALD SiO_x, UV-O_3 oxidation [124], [128], and plasma oxidation [119], [129]. Direct comparison of the different oxide techniques is difficult between papers/institutions due to the additional processes that influence the final passivation. However, some studies directly compared the different oxidation techniques. There was often little difference between the different oxide layers [128], but a thermal oxide typically obtained the best passivation [119], [124], [130]. Gad et al [130] measured a D_{it} of $\sim 1\times10^{12}$ cm^{-2}/eV for an oxide grown via a rapid thermal oxidation and hydrogenation.

The highly doped poly-Si layer is formed by first depositing an a-Si layer using PECVD [120]–

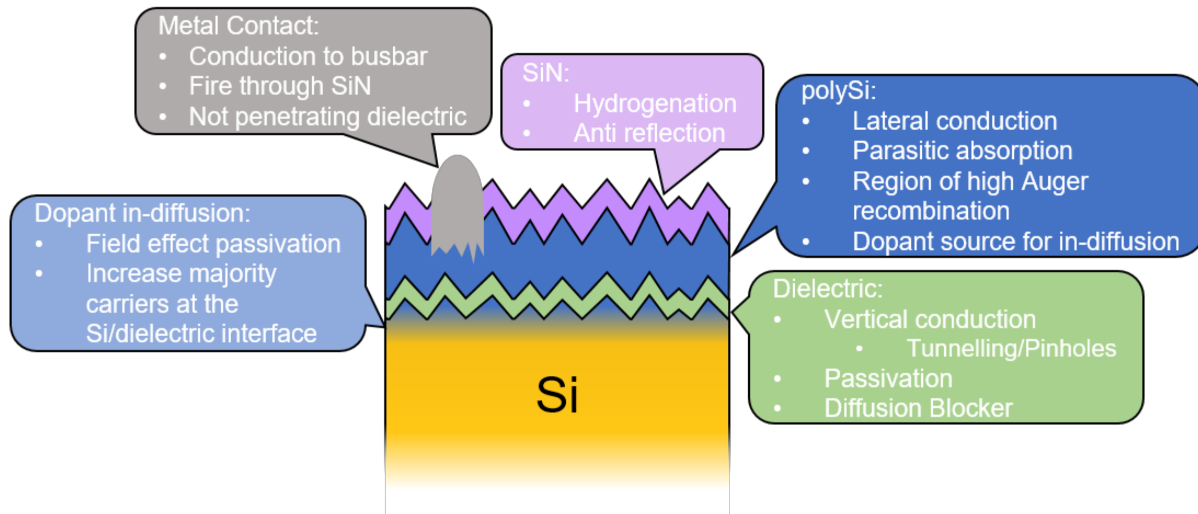


Figure 2.10: Components of a poly Si based contact

[122], LPCVD [120], [121], [127], [129] or PVD [121]. The a-Si is either doped in-situ or as a separate step [131], [132]. A high-temperature anneal is required to partially crystallise the a-Si and form the poly-Si structure. All deposition techniques, with either in-situ or ex-situ doping, have produced high-efficiency cells.

The poly-Si layer performs multiple vital functions in the contact structure. Its high conductivity provides a low resistivity current path to the metal contacts, it generates an in-diffusion of dopants into the Si wafer, and it acts as a buffer layer to prevent the metal contacts from damaging the SiO_x. One detrimental impact of the poly-Si layer is the increase in parasitic absorption in the cell, particularly if the poly-Si contact is on the front side or the cell is bifacial (i.e. allows light to be absorbed from both sides). To minimise the parasitic absorption, the thickness of the poly-Si layers has been reduced [24]. A 20 nm poly-Si causes <1 mA/cm^2 reduction in the J_{SC} [133]–[135]. The reduction in poly-Si thickness is limited by the screen printing technology, which requires a thick poly-Si to prevent spiking through the SiO_x. Adding dopants to the poly-Si can increase the band gap and reduce absorption in the capping layer. Carbon incorporation to form a SiC layer is the most widely studied [118], [136]–[139]. Doping with Nitrogen [140] and oxygen [141]–[143] have also been investigated. Promising results have shown improved transparency, but at the expense of a higher sheet resistance, therefore a TCO may be necessary to maintain a low fill factor (FF) [137], [143].

2.5.2 Influence of the Post Deposition Anneal

As well as crystallising the a-Si to form the poly-Si layer, the high-temperature anneal provides two other key functions. The high temperature allows restructuring of the Si-O bonds, and causes in-diffusion of dopants from the poly-Si into the wafer, providing both a high doping concentration at the silicon surface and a doping gradient across the interface. Studies have compared the dielectric interface after annealing at a range of temperatures [111], [144], [145]. It was found that there is a significant improvement in the passivation of the Si surface with anneals around 800−850 °C, likely due to the reordering of SiO_x bonds. The nature of the SiO_x layer dictates the performance at temperatures above 850 °C. Figure 2.11 images two thermal oxide layers at a range

of anneal temperatures. At 900−950 °C a 1.2 nm oxide ‘balled up’ and lost passivation, while a thicker, 1.5 nm oxide thinned but still maintained a complete layer [144], [145].

The diffusion of dopant atoms into the Si during the high-temperature anneal forms a high concentration of dopants immediately under the SiO_x layer. This increases the majority carrier density at the interface, which increases the conductivity across the SiO_x. It also reduces minority carriers at the direct Si/dielectric interface, reducing SRH recombination [146]. The doping gradient between the highly doped poly-Si and the Si base induces band bending in the Si. This generates an electric field across the interface and field-effect passivation to complement the chemical passivation achieved by the SiO_x. The doping profile is dependent on the temperature and time of the anneal and can impact the passivation properties achieved [129].

2.5.3 Conduction Mechanisms in Poly-Si Contacts

There are two main conduction mechanisms responsible for carrier transport through the dielectric nanolayers in poly-Si contacts. The first is quantum tunnelling as detailed in Appendix A. The current flows uniformly through the dielectric layer and is highly dependent on the oxide thickness and the band offsets. The other conduction mechanism is known as pinholes. Pinholes are nanoscale regions where the poly-Si penetrates the oxide layer. In these regions, there is a direct Si-Si contact that has very low resistivity so the current flow through the oxide becomes localised to the pinhole regions. The total resistivity when pinhole conduction is dominant is determined by the density of pinholes and the spreading resistance of each pinhole (due to the non-uniform current flow). Figure 2.12 depicts the current flow in a tunnelling and pinhole device.

Multiple studies have investigated the conduction mechanisms in poly-Si contacts. Temperature-dependent Current-Voltage (T-JV) [147]–[149], Electron Beam Induced Current (EBIC) [150], and Tetramethylammonium hydroxide (TMAH) etching [127], [150] have all been used to detect the presence of pinholes, along with Transmission Electron Microscopy (TEM) images that provide

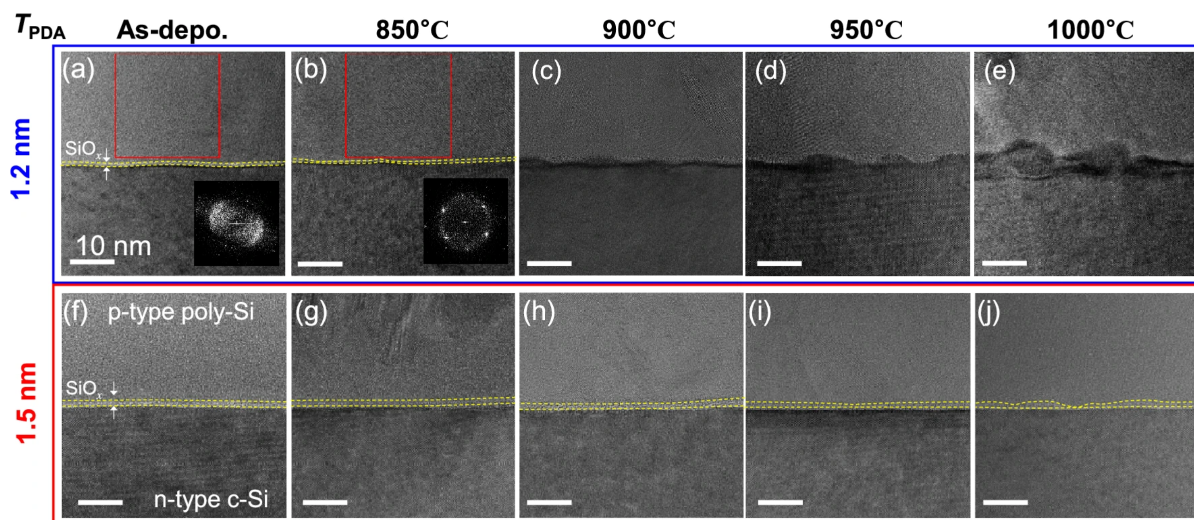
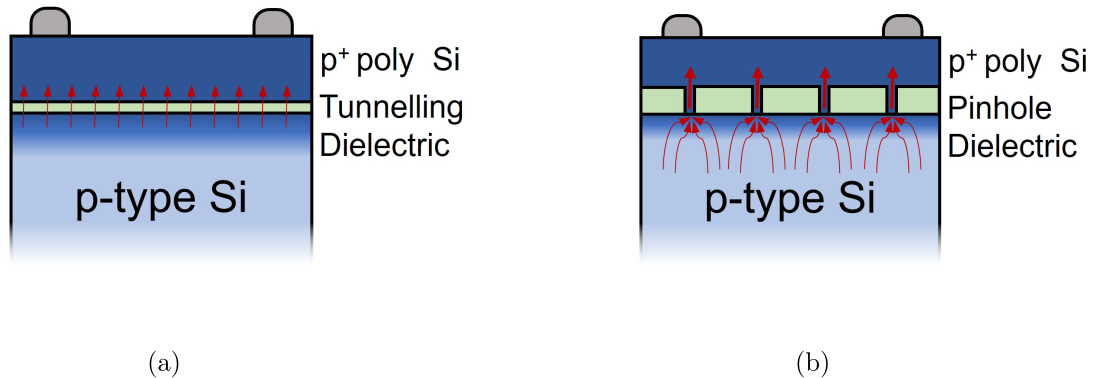


Figure 2.11: TEM images of the cross-sectional structures around the SiO_x layers in as-deposited states, annealed at 850 °C, 900 °C, 950 °C, and 1000 °C for the samples with (a)–(e) 1.2 nm-thick SiO_x layers and (f)–(j) 1.5 nm-thick SiO_x layers. The Fast fourrier transport images in (a) and (b) show the crystallisation of the a-Si and were obtained from the red-boxed regions. Reproduced from [145].



(a) (b)

Figure 2.12: Current flow through a dielectric with a) tunnelling-dominated conduction and b) pinhole-dominated conduction.

atomic resolution of the interface, but are limited by the extremely localised region. Conductive Atomic Force Microscopy (cAFM) [151]–[153], has also been used to determine the conduction mechanism. However, Morisset et. al. [154] somewhat invalidated these results by showing the localised current spots in a reference sample with no interfacial oxide present and the density of these hotspots still increased with higher T_{ann}. Despite this, most other techniques have produced corroborative results and some general rules can be drawn for fabricating contacts with either tunnelling or pinhole-dominated conduction.

The dominant conduction mechanism is determined by the oxide thickness and the annealing temperature. Thinner oxides annealed at <900 °C can achieve highly passivating, low resistivity contacts dominated by tunnelling. Annealing at higher T_{ann} can lead to oxide breakup, which will reduce the passivation quality. The exact temperature that this will occur will depend on the oxide growth method though is typically 850-950 °C. Thicker oxide layers ∼2.2 nm have a high resistivity from tunnelling alone, so at low T_{ann} the contacts are highly resistive. The thicker oxides can withstand a higher temperature before oxide breakdown. At 900-1050 °C pinholes form. Pinholes can reduce the passivation quality of the oxides [150], however, was found that careful control of the pinhole density can provide highly conductive contacts with good passivation of below 2 fA/cm^2 [155], [156].

2.5.4 Hydrogenation

After annealing the poly-Si, a hydrogenation step is carried out to provide additional passivation. Industrially, a thick SiN_x or AlO_x layer that contains a high concentration of hydrogen is used [59], [155]. During a subsequent firing step, this hydrogen is driven to the SiO_x/Si interface. The measured improvement in iV_{OC} can be 40-50 mV [157]–[161] reaching values of 720 mV for p$^+$ poly-Si [157] and 740 mV for n$^+$ poly-Si [158], [162]. In research scale devices, a remote hydrogen plasma [159] or a forming gas anneal, FGA [155], [158] may be used. Figure 2.13 shows the evolution in the passivation quality for each stage in the process.

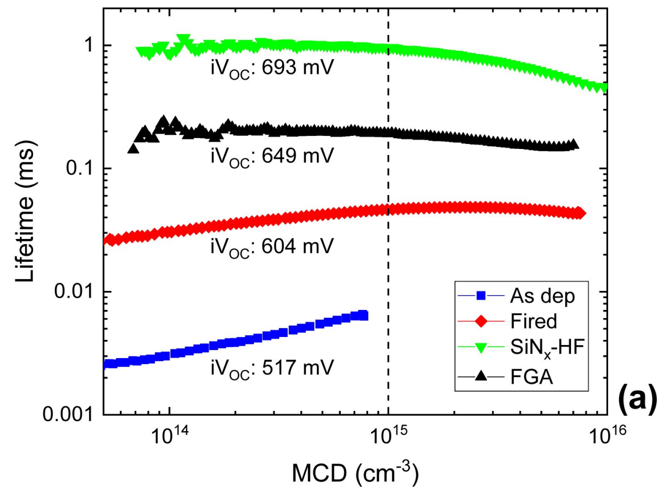


Figure 2.13: Figure showing the lifetime curves at each stage of the poly-Si process [160].

2.5.5 Metallisation

The metallisation of poly-Si contact structures is currently carried out through screen printing using silver pastes [156], [158], [163]. During firing, the metal paste penetrates the SiN_x layer to contact the highly doped poly-Si layer. Current screen printed metal pastes require a thick layer of poly-Si to prevent the metal penetrating the dielectric layer and reducing the passivation quality. This results in large absorption losses [164]. Reducing the poly-Si thickness results in a higher sheet resistance and an increase in J_0 [165]. The increase in J_0 could be due to the metal 'spiking' through the SiO_x layer [165], [166], however, even thick poly-Si layers show an increase in the J_0 under the metal contact. By measuring J_0 as a function of metallisation fraction for a p^+ poly-Si contact, Ok et al. [163] found $J_{0,met}$ to be 170 fA/cm^2, while the unmetallised surface had a J_0 of just 5.5 fA/cm^2. Padhamnath et al. [165] improved on these values with a $J_{0,met}$ of just 24 fA/cm^2 for a 150 nm poly-Si layer. The increase in J_0 during metallisation is significant, however, this is a substantial improvement compared to a standard boron emitter with $J_{0,met}$ >1000 fA/cm^2 [167].

The silver usage in industrial TOPCon is a current limitation for increasing the production to Terra Watt scale. Alternative contacts using copper [39] or aluminium [168] as an alternative screen printing method, or a combination of laser ablation and electroplating [40], [169] are being investigated to reduce silver consumption. The alternative metallisation techniques produce contacts with low ρ_c, though there are issues with the stability when using less Nobel metals.

2.6 Poly-Si Contacts using Alternative Dielectrics

Recent work has reported alternative dielectric materials as passivating layers in poly-Si structures. Reichel et al [170] carried out a wide-ranging study investigating many ALD oxide and nitrides in poly-Si contacts for both electrons and holes. This work found the thermal SiO_x outperformed all ALD dielectrics for both electron and hole contacts. However, the fabrication of these contacts is a highly versitile process so more research is required to better understand these layers, in particular, how they differ from silcon oxide. In addition to the work of Reichel, other authors have implemented aluminium oxide and silicon nitride in poly-Si contacts. This is reviewed in more

detail in the next sections.

2.6.1 Aluminium Oxide

Aluminium oxide attracted attention as a beneficial interfacial layer in the early 2010s. An ultra-thin layer of ALD AlO_x was inserted under the Al contacts for the n^+ phosphorus emitter [171]–[174] or at the boron BSF [173], [175]. It was shown to provide passivation, increasing iV_{OC} by 12-15 mV [171], [174]. Using ALD to deposit the AlO_x nanolayers allows very precise control of thickness. The optimum thickness varied widely between studies from 0.24 nm [171] to 2.2 nm [174]. The transport mechanism through the AlO_x layer was generally presumed to be dominated by tunnelling.

In more recent years, AlO_x has been studied as an alternative to SiO_x in poly-Si hole selective contacts [170], [176]–[179]. It has a low valence band offset of 2.9 to 3.75 eV [180]–[184], which corresponds to a higher tunnelling probability for holes than SiO_x. It is well known that thick AlO_x layers have a high density of negative fixed charge, which could improve the properties of a hole selective contact. The fixed charge in nanolayer AlO_x has been characterised [177], [185] and found to be 3-5$\times10^{12}$ q/cm^2 in layers <1 nm, though it is not known if the charge remains after poly-Si deposition and annealing. Kaur et al [178] achieved high levels of passivation with J_0 of 15 fA/cm^2 in AlO_x/poly-Si structures. The thickness control, high probability of hole tunnelling, and high negative charge make AlO_x a promising candidate in hole-selective poly-Si contacts.

2.6.2 Silicon Nitride

Silicon nitride based passivating contacts have primarily been investigated as electron selective contacts. The potential benefits of SiN_x include higher tunnelling probabilities [186], improved blocking of dopant atoms through the nanolayer [129], [187], and, for electron contacts, a positive charge to further enhance the FEP. Yan et al. [187], [188] added thick SiN layers (>10nm) to both electron and hole SiO_x/poly-Si contacts. The SiN_x was beneficial to the electron contacts, but a high contact resistivity was detrimental hole contacts.

In addition, SiO_xN_y layers have been studied to combine the superior chemical passivation of SiO_x with the advantages of SiN_x [129], [189], [190]. Feldmann showed that a nitrided silicon oxide nanolayer was effective at blocking boron diffusion, however the passivation quality was reduced compared to that of pure SiO_x. So far, SiN has achieved promising results for both passivation and contact resistivity in electron contacts. There are beneficial aspects for hole contacts, including beneficial boron diffusion profiles, though poor chemical passivation and high resistivity currently limits these contacts.

2.7 Dopant Free Passivating Contacts

Dopant free passivating contacts were introduced in Section 2.4 and have the advantage of lower absorption losses compared to SHJ or poly-Si technologies. Many materials have been investigated [112], with transition metal oxides often found to have the desired band offsets [112], [120]. The very low or negative band offset allows layers of tens of nanometres as tunnelling is not the dominant conduction mechanism. However, the lack of an in-diffused region under the contact, removes the highly doped region that can help fabricate low-resistivity contacts. As such, there are relatively

few DFPC stacks with ρ_c <100 mΩ·cm^2. AlO_x+CuO_x, SiO_2+VO_x and MoO_x have some of the lowest reported ρ_c of 33 mΩ·cm^2 [191], 35.5 mΩ·cm^2 [192] and 60 mΩ·cm^2 [193] respectively. This is sufficiently low to allow a full area passivating contact, though the sheet resistance is too high for transport to contact fingers, thus, either a full area metal contact [192], [194]–[197] or a TCO layer [194] is required to complete the contact. As there is no in-diffusion in DFPCs, high passivation must be achieved from a combination of chemical passivation including hydrogenation, and FEP from intrinsic charge in the contact materials. The addition of a SiO_x [103], [192], [195], [197], [198] or a-Si(i) nanolayer [194], [199] is often used to improve the chemical passivation as the Si surface. TiO_x single layers have achieved high levels of surface passivation (Section 2.3.2). This, combined with a beneficial band structure, has led to its study in DFPCs.

2.7.1 Titanium Oxide in DFPC

ALD TiO_x nanolayers have been deployed in DFPC as a full area passivating contact layer. The very low CBO of ~0.1 eV [196] has led to multiple studies investigating TiO_x electron contacts [101], [194]–[196], [198], [200]–[203]. Matsui et al. [194] found the TiO_x had a positive charge when deposited with plasma ALD, enhancing the passivation and charge collecting in electron contacts. An efficiency of 22.1% was reported by Yang et al. [195] for a cell with a full area, electron selective TiO_x rear contact and a boron emitter. Recent work has investigated TiO_x as a hole selective contact [194]. The VBO of 2 eV limits the thickness for a conductive layer via direct tunnelling, but an additional transport mechanism is proposed through a trap site near the Si valence band edge [194]. Additionally, thermal ALD forms a negative charge in the TiO_x, aiding hole collection and adding beneficial FEP to the contacts [194]. The negative charge in TiO_x is critical for both transport and passivation qualities. To optimise the hole selective contacts a deeper understanding of the role of the fixed charge in the passivation and transport properties is required.

2.8 Fixed Charge in Passivating Contacts

Developing passivating contact structures with an intrinsic fixed charge has gathered interest in recent years [79], [170], [177], [179], [185], [204]–[207]. In poly-Si contacts, the doping profile across the dielectric/Si interface increases the concentration of the majority carrier at the interface and repels the minority carrier, inducing band bending. A Si/dielectric interface charge has the same effects on the free carriers, and it was proposed that this could complement the doping in-diffusion to improve the passivation and transport properties of the poly-Si contacts [177]. AlO_x and SiN_x have been implemented into poly-Si contact structures to investigate potential benefits obtained from their intrinsic charge [170], [177], [179], [207]. The negative charge in AlO_x promotes an increased hole concentration at the Si surface, and thus improves passivation in hole-selective contacts. Conversely, the positive charge in SiN_x promotes an increased electron concentration at the Si surface, improving electron contacts. Difficulties arise when attempting to quantify the benefits of a highly charged dielectric. The dielectric dictates the chemical passivation, majority carrier transport, and diffusion of dopants in a poly-Si contact. Therefore, the specific influence of a dielectric charge in these structures is difficult to isolate.

Increasing the concentration of majority carriers at the silicon surface is particularly important in DFPCs as there is no highly doped region or FEP induced by a doping gradient. The high

work-function of the metal oxides combined with a high WF metal can generate the accumulation of holes required for effective hole contacts. Previous research often reports the surface potential in semiconductors [103], [197], [199], [200], [208] as it relates to the strength of the electric field at the surface and thus the carrier population and band bending characteristics of the interface. Fixed charge in the metal oxide may also contribute to the increase in holes, however, the respective contributions of the high WF and any fixed charge to the surface potential are not determined. Recently, the fixed charge in ALD AlO_x has been utilised in DFPC structures as an alternative interlayer instead of SiO_x or a-Si [191], [209], [210]. The structure with the addition of AlO_x has an increase in V_{OC} of 20 mV compared with a direct Si/Metal Oxide contact [191]. Further work could be done to characterise the Si/DFPC interface to develop a better understanding of the passivation mechanisms and guide future research into improving DFPCs.

Simulations provide a means of isolating the effect of the dielectric charge. Kløw et al [175] showed that high charges could increase the FF of Si/AlO_x/Al contact. This effect is likely a result of reduced series resistance in the contact. Ke et al. [211] simulated AlO_x poly-Si contacts. The efficiency of a cell featuring an AlO_x contact with and without an in-diffusion is simulated for varied D_{it} and Q_f. As expected, a larger charge and lower D_{it} gives a higher efficiency. The effect is stronger when there is no in-diffusion, highlighting the potential benefit of high fixed charge in DFPC structures. Further investigation into the contact parameters would provide a more detailed view on the specific influence of the charge.

There is evidence that a high dielectric charge can improve the contact properties, offering a route to improve upon the SiO_x and a-Si contacts which are the current mainstream technology. Although novel passivating contact structures have been fabricated, the beneficial effect of a dielectric charge has not been quantified. This is due to the complex nature of the passivating contact structures, in which the dielectric layers have many roles to fulfil, preventing the effect of charge to be isolated. While attempts have been made to characterise charge experimentally, the beneficial effect has not been quantified. This is due to the complex nature of the passivating contact structures, which have many concurrent requirements that prevent the effect of dielectric charge from being isolated. Simulations provide a means to isolate the charge and understand the effects on the contact properties. They show dielectric fixed charge can improve the contact properties, offering a route to improve upon the SiO_x and a-Si contacts which are the current mainstream technology. This could be particularly useful for hole-selective contacts as they currently have lower efficiencies.

2.9 Hole Contacts

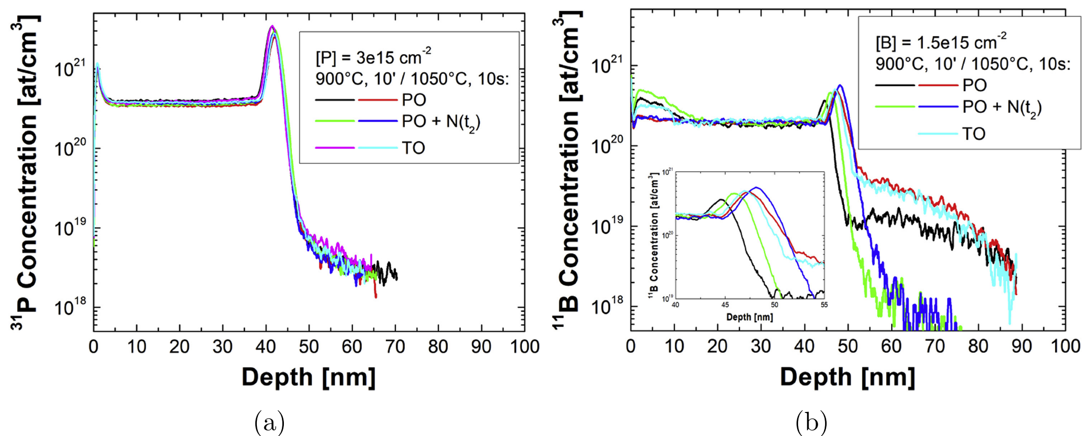
High-efficiency solar cells require two highly selective passivating contacts, one for electron collection and one for hole collection. So far electron contacts have been more effective than hole contacts in both poly-Si [55], [111], [122], [141], [155], [212], [213] and SHJ structures [214]. In addition, a large range of processing conditions have achieved excellent electron-selective poly-Si contacts, however, the optimum hole contacts have a much narrower processing window [111]. This makes it difficult to maintain high efficiencies when hole collection limits the overall device performance.

There are three main reasons why SiO_x poly-Si contacts have been less successful as hole-selective contacts, compared to the electron-selective counterparts. The first is due to the band structure at

the Si/SiO_x interface. SiO_x has a large valence band offset of 4.5 eV compared to the conduction band offset of 3.2 eV [186]. This has a significant effect on the tunnelling probability of carriers through the SiO_x, making it difficult to achieve a low resistivity contact. Either the SiO_x layer needs to be thinner (<1 nm [139]) or pinholes must be formed. Both these measures could lead to poorer passivation of the Si interface [215]. Thermal oxides are currently the most effective for hole contacts [155], [216]. This may be due to a higher thickness, which enables a high T_{ann} to form pinholes without the oxide breaking up. Mack et al. [156] have reported an extremely low J_0 of 1 fA/cm^2 after a 30 min, 900 °C anneal. The oxidation technique and oxide thickness were not disclosed.

The second reason for SiO_x to form less effective hole contacts is the diffusion profile that forms after the high-temperature anneal that crystallises and dopes a-Si into the required poly-Si layer. Phosphorus is blocked by the SiO_x layer, causing a build-up at the SiO_x/poly-Si interface and limiting diffusion into the wafer [129]. This results in a steep diffusion profile that generates a large FEP passivation component. Boron is not blocked in the same manner, resulting in deeper diffusion profiles with a flatter gradient [129], [216]. This reduces the beneficial FEP due to the concentration gradient and increases the Auger recombination due to a larger volume of the Si near the surface with a high concentration of dopants. The high temperatures required to form pinholes can further exacerbate this effect. Figure 2.14 shows the difference in the dopant profile of boron and phosphorus poly-Si contacts. There has been some work on altering the boron diffusion profile by first depositing intrinsic a-Si layers [217], [218] or by growing a nitrided silicon oxide layer [129]. Both methods have shown promise in slowing the boron diffusion to achieve a steeper doping profile. This is seen in Figure 2.14(b) which includes the ECV profiles of a nitrided oxide. Interestingly, the highest passivation achieved in SiO_x/poly-Si hole contact structures has been when the p-type poly-Si is deposited on an n-type wafer [149], [155], [156], [216], [219]. This may be due to additional FEP generated from the sharp change from p^+ to n-type silicon (Figure 2.6(b)) [145].

The final reason that the passivation of hole selective contacts is poorer than electron contacts is due to the intrinsic properties of electrons and holes. Electrons have a higher mobility, which results in a larger capture cross-section. At a p-type surface, electrons are the minority carriers, therefore their capture cross-section dominates recombination. The difficulties presented in this



(a) (b)

Figure 2.14: Dopant profiles in a) phosphorus and b) boron poly-Si contacts [129].

section highlight the need for more research to improve the quality of hole selective passivating contacts, in particular investigating alternative materials to SiO_x.

2.10 Characterising Passivating contacts

The methods for characterising poly-Si and SHJ contacts have primarily focused on contact resistivity and lifetime measurements for determining the transport and passivation properties. The contact resistivity is often measured using the TLM or Cox Stracks techniques to extract the contribution from the contact. Worryingly, there are a number of cases where these techniques have been applied incorrectly, leading to significant errors in the resistivity measurements reported [179], [187], [220], [221]. The most significant error results from allowing lateral conduction in the poly-Si layer. In TLM this will mean a large proportion of the current will bypass the dielectric layer entirely and in Cox Stracks the contact area will increase due to spreading in the poly-Si. Additional analysis of the conduction mechanisms has used T-JV to calculate the pinhole density [149]. This has provided crucial evidence for understanding the effect of the high-temperature anneal in SiO_x contacts, discussed in Section 2.5.3. The transport mechanisms in SiN_x and AlO_x poly-Si contacts or in many DFPCs have not yet been studied.

When studying the passivation in SiO_x/poly-Si contacts and SHJ, the interface charge is very low so the surface passivation achieved can be assumed to be purely chemical passivation. However, alternative dielectrics for poly-Si contacts and many novel materials for DFPC have substantial concentrations of fixed charge. This means the passivation will be a combination of field effect and chemical passivation. To determine the relative contributions of each, an accurate determination of D_{it} and Q_f is required. The typical methods to determine the D_{it} and Q_f in dielectric films were originally developed for substantially thicker films. The high conductivity of the nanolayer films makes a detailed analysis of the interface properties in passivating contact structures difficult. There have been some attempts to characterise the charge using corona-biased Kelvin Probe [170], [176]. The Kelvin probe is not directly contacted to the dielectric nanolayer, so the high conductivity is not a problem. However, using corona charge to bias the sample leads to issues as the charge can leak through the nanolayer dielectric, neutralising the corona charge. This leads to an overestimation of the charge in the film. Gad et al. [119], [130] used applied biased SPV to characterise SiO_x nanolayers. The applied charge is more stable than corona and it was used to determine the D_{it} distribution across the band gap energy. The contributions from Q_f and D_{it} cannot be fully isolated using SPV, so it is assumed that Gad set the SiO_x fixed charged to a low, constant value. Hollemann et. al. [222] uses a thicker oxide in the poly-Si structure to allow C-V analysis of the Si/dielectric interface, however this has limitations. The 10 nm thermal SiO_x layer is highly unlikely to have the same properties as the 2 nm ozone SiO_x and a different doping profile is generated for the two oxides. Adopting this technique for alternative dielectrics such as SiN_x or AlO_x leads to further issues as the high level of charge in these films is likely to vary in the first few nanometres of film growth. Thus, there are substantial difficulties in accurately extracting the interface properties from nanolayer dielectric structures.

2.11 Contribution to the Scientific Field/justification for the work

This thesis aims to contribute to two current limitations in the field of passivating contacts. The first is the development of improved passivating hole contacts compared to the standard SiO_x poly-Si contacts. This would enable further improvement in the efficiency of silicon PV cells when combined with the already well-developed electron-selective contacts. To achieve this, SiN_x, AlO_x and TiO_x are studied as potential nanolayers in hole-selective contacts. SiN_x and AlO_x have favourable band alignments for high hole conductivity, while AlO_x and TiO_x can also have advantageous negative charge. Additionally, it has been shown that SiN_x can block the boron diffusion, which could result in an improved doping profile.

The second contribution from this thesis is the development of techniques for advanced characterisation of the nanolayer dielectrics and their interface with Si. These will enable a wider-reaching scientific approach to optimising poly-Si contacts and furthermore, the techniques can be applied to other contact structures such as DFPCs on silicon devices or contacts on perovskite and other emerging PV technologies.

Chapter 3

Experimental Methods

3.1 Specimen Fabrication

3.1.1 Wafers

The types of silicon wafers used in this thesis are detailed in Table 3.1. P1-10, P10-20m, and P1-5m are from University Wafer, N30-60 is from MEMC, while EPFL and AIST wafers are provided by collaborators for specific experiments. The properties of the silicon wafers are of crucial importance for many of the experimental techniques used in this thesis. The key properties are the dopant type (n or p), resistivity, bulk lifetime, thickness, and surface texture. Some characterisation techniques are not possible with certain wafers, and the wafer properties are necessary for the analysis of results. Specific considerations are given in the relevant sections of this and future chapters. All wafers are cleaned before use using the standard RCA cleaning procedure, detailed in Appendix B, to remove organic and inorganic contaminants from the surface of the samples.

3.1.2 Rapid Thermal Oxidation, RTO

Nanolayer silicon oxide can be grown using a variety of methods. Rapid thermal oxidation (RTO) is used as the SiO_x thickness can be controlled. The RTO is carried out in a Jipelec Jetfirst rapid thermal anneal furnace. The temperature profile and furnace conditions for oxidation are detailed

Table 3.1: Wafer Groups

Wafer	**Dopant**	**Growth**	**Resistivity [Ω·cm]**	**Thickness [µm]**	**Main Use**
N30-60	P	Cz	30-60	700	Lifetime
P1-10	B	Cz	1-10	500	SPV, CV, GV
P10-20m	B	Cz	10-20 m	500	IV
P1-5m	B	Cz	1-5 m	500	IV
EPFL	B	FZ	1	200	Poly-Si
AIST	P	FZ	3	280	TiO_x [a]
AIST (111)	P	FZ	2	280	TiO_x

[a] planar and textured

in Figure 3.1. The chamber is initially purged with N_2 for 1 min, then the chamber is heated in two steps to the oxidation temperature (700-900 °C) at a reduced flow rate of 200 sccm N_2. Once at the set temperature N_2 flow is stopped and O_2 is introduced at a rate of 200 sccm into the chamber to grow the nanolayer SiO_x with the oxide growth process lasting between $5-60$ s. During cooling, the oxygen flow is stopped and 200 sccm N_2 is restarted.

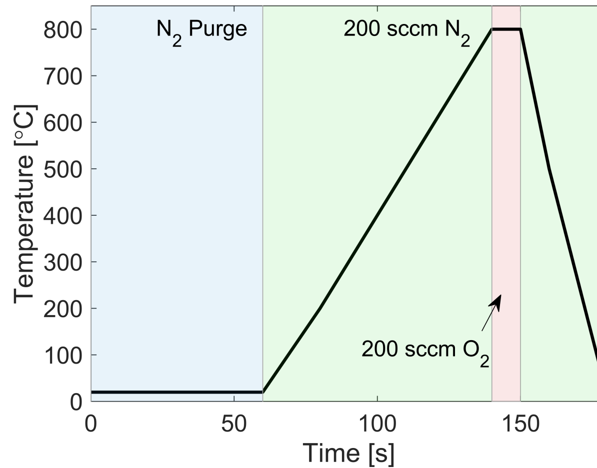


Figure 3.1: Programmed temperature profile and gas flows for SiO_x growth using RTO

3.1.3 Plasma Enhanced Chemical Vapour Deposition, PECVD

Plasma-enhanced chemical vapour deposition (PECVD) is a common technique in the semiconductor industry to deposit various materials. Before deposition, a dummy wafer is placed in the chamber and 75 nm of the required material is deposited. Then an RCA-cleaned sample is positioned on the dummy wafer and the PECVD chamber is evacuated to a pressure of <1 mTorr. A heated stage controls the sample temperature. For SiN_x deposition, silane and ammonia gases are injected into a deposition chamber and subjected to a plasma. The reactive species generated by the plasma cause the gases to react and bond to the silicon substrate The hydrogen present in the precursor gases results in a SiN_x:H film. The deposition is one-sided with typical deposition rates of 1 nm/s

An Oxford Instruments PlasmaLab 80+ system is used to grow silicon nitride and silicon oxide layers. The a-Si is deposited by collaborators at EPFL in an Oxford Instruments PlasmaPro 100, ICP CVD system. To avoid blistering of the poly-Si layer, a 10 s deposition of intrinsic a-Si is deposited before the boron-doped layer [157]. SiO_x is used to form an insulating layer for capacitance-voltage measurements in Chapter 7. The deposition is carried out in ten, 10 s bursts. The multiple short depositions cause different nucleation sites to form at each initiation of the plasma. This ensures a pinhole-free SiO_x layer with low conductivity. The standard deposition conditions are detailed in Table 3.2.

Table 3.2: Standard operating parameters for PECVD SiN_x, SiO_x and poly-Si

Parameter	SiN_x	SiO_x	a-SiC_x:B
Temperature	350 °C	350 °C	200 °C
Pressure	650 mTorr	800 mTorr	520 mTorr
Plasma Power	20 W	20 W	160 W
Silane flow rate	400 sccm	200 sccm	95 sccm
Ammonia flow rate	40 sccm	-	-
N_2O_2 flow rate	-	680 sccm	-
$B(CH_3)_3$ flow rate	-	-	75 sccm
CH_4 flow rate	-	-	15 sccm
H_2 flow rate	-	-	119.6 sccm

3.1.4 Atomic Layer Deposition, ALD

Atomic layer deposition (ALD) is used to deposit aluminium Oxide and titanium oxide nanolayers on silicon substrates. Contrary to PECVD, each precursor gas is injected independently in short pulse and purge cycles. This saturates the surface with the first precursor gas, before removing any surplus precursor. The second precursor is then injected and can react to the new surface condition. The purge removes excess precursors and any bi-products of the deposition. One full AlO_x cycle consists of 3× TMA pulse/purge cycles followed by 2× H_2O pulse purge cycles. The reaction mechanism is shown in Figure 3.2. The growth rates (0.1 nm/cycle) are slower than PECVD deposition, which allows greater control of the nanolayer thickness. The AlO_x depositions are carried out using an Anric thermal ALD with the conditions shown in Table 3.3. The TiO_x depositions are carried out by collaborators at AIST using both plasma and thermal ALD on an Oxford Instruments FlexAl system. The TiO_x deposition conditions are found in Table 3.3.

Table 3.3: Standard deposition parameters for ALD AlO_x

Parameter	tALD AlO_x	tALD TiO_x	pALD TiO_x
Chamber Temperature [°C]	150	260	200
Pressure [mTorr]	200	80	80
TMA Pulse	3x3 s	-	-
TMA Purge time	11 s	-	-
H_2O Pulse [s]	2×2	5×1.2	-
H_2O Purge time [s]	13	30	-
TTIP pulse [s]	-	1.2	1.2
TTIP purge [s]	-	9	9
O_2 plasma [s]	-	-	6 (330 W)
O_2 purge [s]	-	-	3

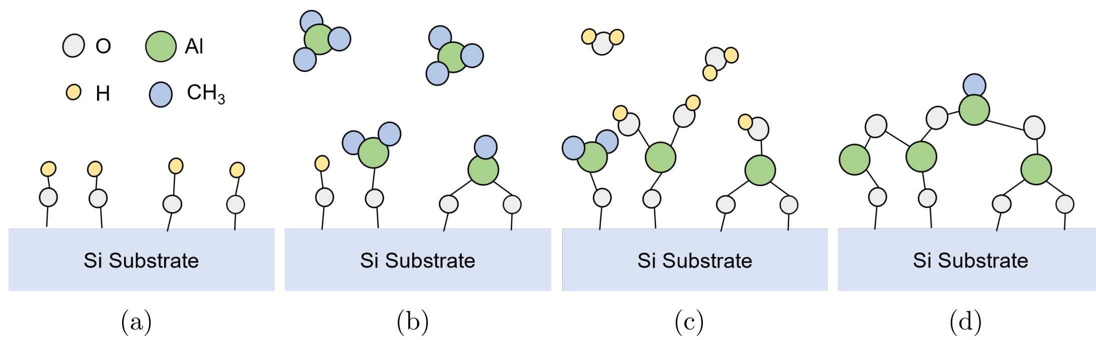


Figure 3.2: AlO_x ALD reaction process a) Si surface terminated with O-H groups. b) 2×pulse-purge cycles of TMA form an Al terminated surface c) 3×pulse-purge cycles of H_2O terminate the surface with Hydroxyl groups. d) The process repeats to grow an AlO_x layer.

3.1.5 Metal Contact Deposition

Thermal evaporation is used to create metal contacts for electrical characterisation of the dielectric structures. The source metal (99.999% Al or 99.99% Au) is placed in a tungsten filament. Under high vacuum (10^{-6} Torr), a high current heats the filament and melts then evaporates the metal source. The deposition rate is monitored using a quartz sensor. The sensor vibrates at a resonant frequency that changes as a material is deposited on the surface. The density and impedance of the source material are used to calibrate the sensor. Thicknesses of 80-150 nm are targeted. The front side contains the interface of interest, which is generally the silicon/dielectric nanolayer. Using a mask, approximately 1 mm diameter circular contacts are evaporated on the front side. The contact area is measured using an optical microscope. For the rear contact, a diamond scribe is used to expose a fresh Si surface and then a full area evaporation takes place. The front side contact is deposited first to minimise contamination on the measured dielectric. Figure 3.3 shows a schematic of the final device structures.

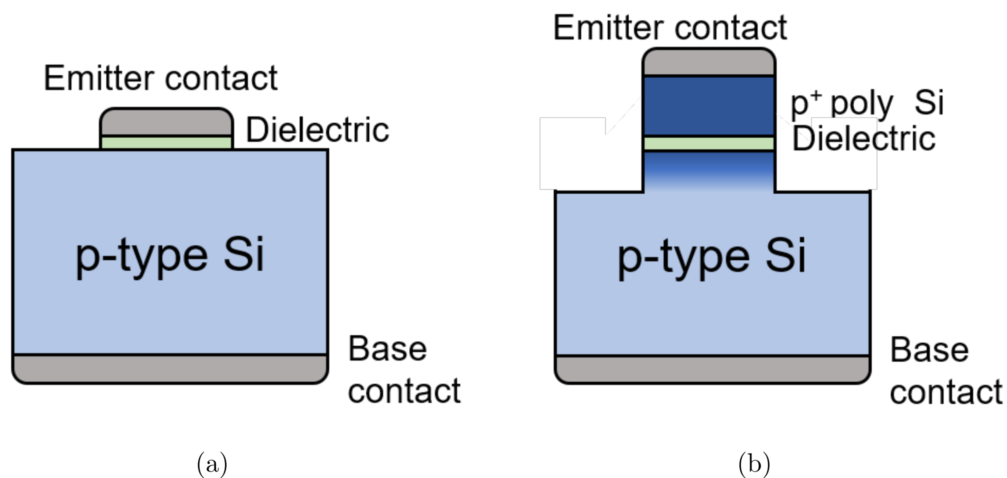


Figure 3.3: Schematic of the sample structures for electrical characterisation techniques. a) Single nanolayer structures b) Full poly-Si stack

3.1.6 Reactive Ion Etching, RIE

Reactive ion etching is used to selectively etch Si while leaving a metal contact undamaged. This isolates the contact stack in poly-Si samples to prevent lateral conduction in the p^+poly-Si or the in-diffused region. This is crucial for obtaining accurate contact resistivity in poly-Si contact structures. The parameters used for selective etching of Si over Al are shown in Table 3.4. The resulting structure is shown in Figure 3.3(b). The ECV measurements in Section 8.3 confirm the total etch depth of ~0.5 µm is sufficient to avoid an influence from the diffusion.

Table 3.4: Standard operating parameters for RIE of poly-Si

Parameter	Value
Temperature	20 °C
Time	5 min
Pressure	600 mTorr
Power	100 W
SF_6	15 sccm
CH_3	40 sccm

3.1.7 Corona Charging

Corona charging is used to deposit a temporary charge on the surface of a silicon/dielectric stack. An ISEG High Voltage power supply is used to apply a -30 kV voltage between the needle tip and the ground plate situated 20 cm away. The high voltage ionises particles in the air. The charge density deposited on the sample is given by [223],

$$Q = \frac{I \cdot t}{q \cdot 2d^2} \tag{3.1}$$

Where I is the current, t is the deposition time and d is the tip-to-sample distance. The charge uniformity across a sample width of 3–4 cm is <1%. The current measured for -30 kV is 23 μA.

3.1.8 Transportation and Storage

Various experiments carried out in this thesis required transportation between institutions. The nanolayers could be sensitive to degradation during this time so efforts were made to minimise this. Samples in Oxford were stored in a vacuum chamber which is back-filled and purged with nitrogen. Samples for poly-Si deposition at EPFL were vacuum-packed with desiccating silica beads. The TiO_x samples from AIST were packaged in a nitrogen atmosphere.

3.2 Ellipsometry

Ellipsometery measures the optical properties of nanolayer films and is commonly used to determine the thickness of dielectrics and dielectric stacks. A linearly polarised light beam is incident on the sample and the reflected beam is collected in the detector. The change in the polarisation of the light beam is detected in the plane of incidence, R_P, and perpendicular to the plane of incidence,

R_S. A schematic of the ellipsometry measurement is shown in Figure 3.4. The polarisation of the beam is indicated by the green lines at the source and detector. The ratio of R_P/R_S is expressed in terms of the magnitude (Ψ) and phase difference (Δ) in the p and s polarisation of the detected beam [224]:

$$\frac{R_P}{R_S} = tan(\Psi) \cdot e^{i \cdot \Delta}. \tag{3.2}$$

The Fresnel equations calculate the proportion of transmission, t, and reflectance, r, for p and s polarisation at each interface [224]:

$$t_s = \frac{2n_1 \cdot \cos\theta_1}{n_1 \cdot \cos\theta_1 + n_2 \cdot \cos\theta_2}, \qquad t_p = \frac{2n_1 \cdot \cos\theta_1}{n_1 \cdot \cos\theta_2 + n_2 \cdot \cos\theta_1}, \tag{3.3}$$

$$r_s = \frac{n_1 \cdot \cos\theta_1 - n_2 \cdot \cos\theta_2}{n_1 \cdot \cos\theta_1 + n_2 \cdot \cos\theta_2}, \qquad r_p = \frac{n_1 \cdot \cos\theta_2 - n_2 \cdot \cos\theta_1}{n_1 \cdot \cos\theta_2 + n_2 \cdot \cos\theta_r}. \tag{3.4}$$

Where θ_1 is the angle from the surface normal to the incident beam, θ_2 is the angle from the normal direction into the sample and the transmitted beam, and n_1 and n_2 are the refractive indexes in the two materials. The Fresnel equations are combined with Snell's law of refraction:

$$n_1 \cdot \sin\theta_1 = n_2 \cdot \sin\theta_2. \tag{3.5}$$

The magnitude and polarisation of each beam path are calculated as the light is reflected or refracted off each interface in the modelled structure. This can be combined to calculate the total reflected light, R_P and R_S. The sample structure is inputted into the model and a regression analysis compares the experimental data to the model results to determine the thickness and refractive index of the nanolayer films.

A Filmsense FS-1 multi-wavelength ellipsometer is used to measure the thickness of the fabricated nanolayers. It contains four LED light sources for multiple wavelength fitting for improved accuracy. Each sample is measured in at least 5 locations to assess sample uniformity. Silicon oxide is measured using the Palik model [225], Aluminium oxide using the McGraw-Hill model [226], and TiO_x using the Devore model [227]. These models have set values for the real and imaginary components of the refractive index. Silicon nitride is fitted using a Cauchy model, which allows the

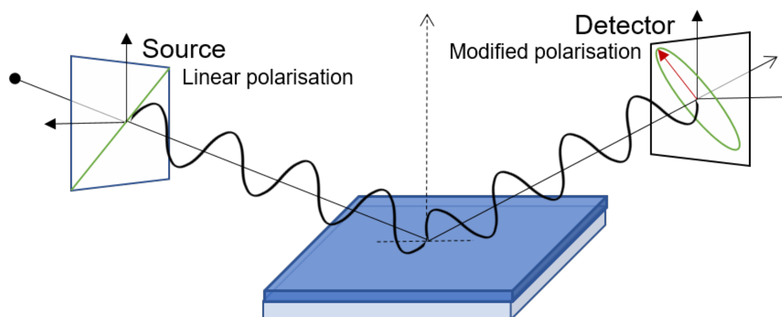
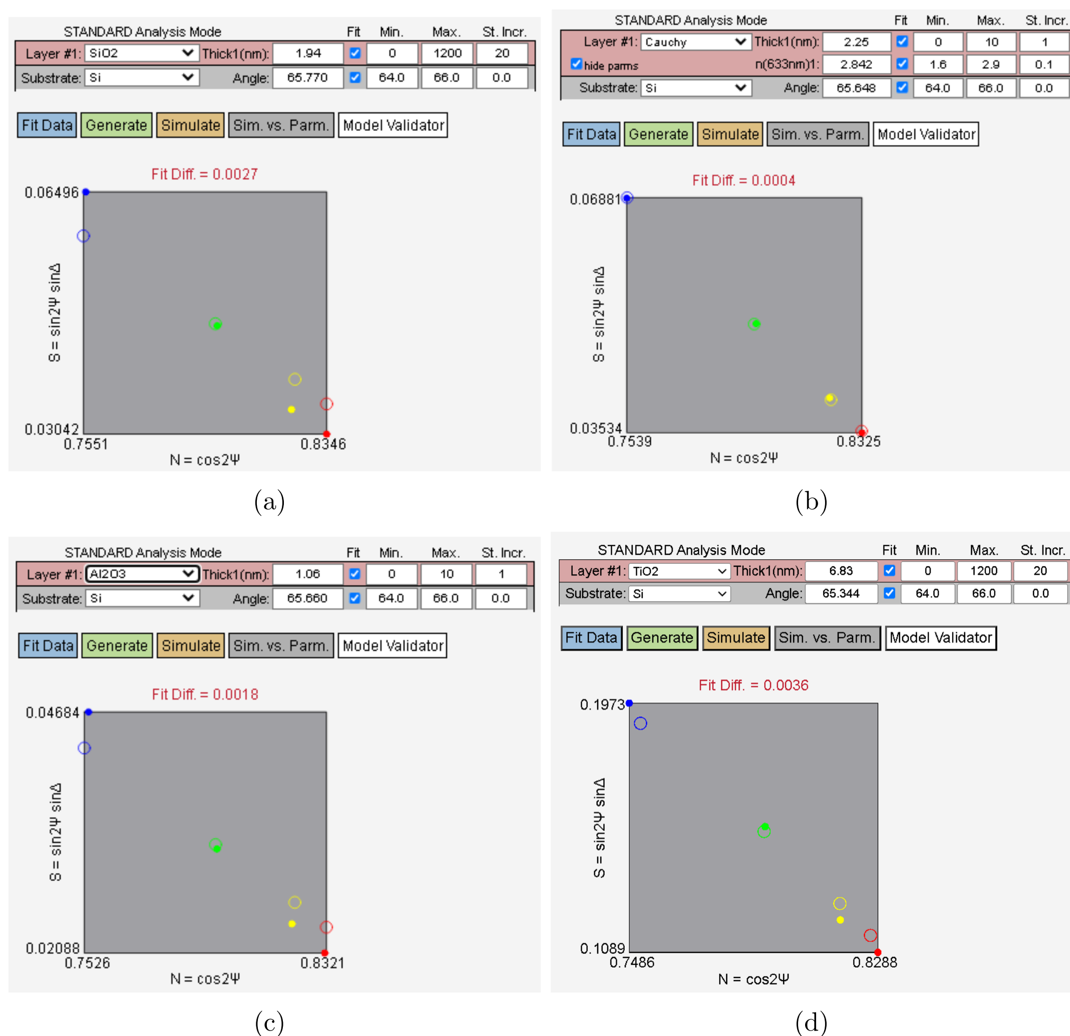


Figure 3.4: Schematic of an Ellipsometry measurement. Linearly polarised light is reflected off the sample surface, the magnitude and phase change of the polarisation is measured at the detector.

refractive index to vary. The Cauchy model is typically used for SiN_x as the deposition conditions have a strong influence on the composition of the film and the resulting refractive index. Figure 3.5 gives example fits for each of the dielectrics used.

For measuring the thickness of films <25 nm, the change in polarisation is significantly more sensitive than the change in the intensity of the beam. This enables ellipsometry to remain accurate at thicknesses below 1 nm, although at low thicknesses the refractive index and thickness become correlated. For models using fixed values for n and k, this is not a problem, however, it could lead to errors in the SiN_x when using a Cauchy model. The measurement is unaffected by specks of dust on the sample as the scattering of the beam reduces the intensity of the light but not the polarisation of the detected beam. However, a uniform layer of contamination such as an organic residue will affect the measurement.



(a) (b)

(c) (d)

Figure 3.5: Ellipsometry fit for a) SiO_x, b) SiN_x, c) AlO_x, d) TiO_x

3.3 X-ray Photoelectron Spectroscopy, XPS

X-ray Photoelectron Spectroscopy (XPS) is a surface-sensitive technique that provides a chemical analysis of the sample. A monochromatic x-ray beam is absorbed by electrons in the sample and photo-electrons are emitted from the sample at kinetic energy E_k. Figure 3.6 shows the process. The binding energy E_B is determined from the difference between the incident photon energy and the kinetic energy of the ejected electron [228],

$$E_B = h\nu - E_k. \tag{3.6}$$

Where ν is the frequency of the x-ray. Electrons in the core levels of each element have specific binding energies and therefore the XPS spectra can give composition analysis of the sample up to the absorption depth (typically ∼10 nm for a laboratory system). The binding energy is sensitive to the bonding state of the element, so different oxidation states can be distinguished, e.g. metallic silicon, Si^0, and silicon bonded to oxygen or nitrogen, $Si^{1,2,3,4+}$. Comparison of the signal intensity for the different elements and bonding states enables the determination of the stoichiometry of the nanolayers.

XPS measurements were performed using two XPS systems, a Thermo Scientific K-Alpha (TSK) and a Phi Versaprobe III (PhiV). The TSK uses a monochromatic A1 Kα X-ray (1.487 keV) source with a 400 μm beam diameter, a beam angle of 54°, and an electron take-off angle of 90°. A pass energy of 20 eV is used for the core peaks, while a higher pass energy of 50 eV is used for the valance band onset due to the small signal at this binding energy. The PhiV uses a monochromatic A1 Kα X-ray (1.487 keV) source with a 100 μm beam diameter, a beam angle of 90°, and an electron take-off angle of 45°. A pass energy of 20 eV is used for all scans. Sputtering is used to etch the surface to remove any undesired surface layers. Sputtering is carried out over a 3×3 mm area using Ar ion-milling at a potential of 1 kV. Measurements are carried out in the Thermo

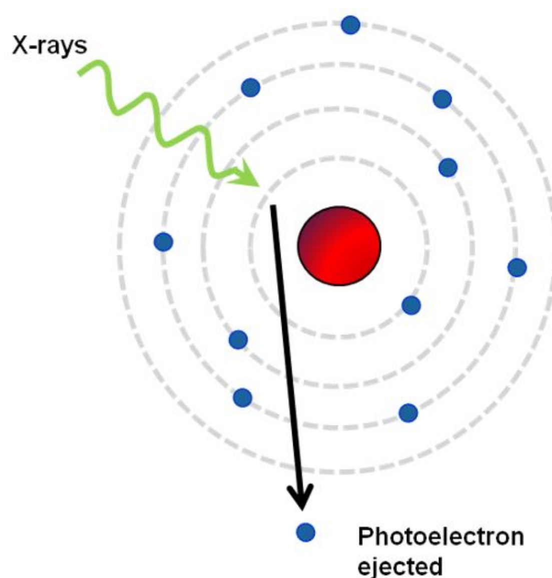


Figure 3.6: Photo-emission of an electron due to an incident x-ray. [229]

Scientific XPS, unless stated otherwise.

In both systems, an energy step size of 0.05 eV is used to give a precise value of the peak position. The carbon 1s peak at 284.7 eV is used to calibrate the samples from any surface charge generated at the sample surface due to the x-ray beam. This step is not strictly necessary for the determination of energy barriers since the calculations require the difference between two energies. The primary use for XPS measurements is to determine the difference in valence band between the dielectric nanolayer and the silicon absorber, here termed the valance band offset (VBO). For this, Kraut's Method [230] is used, which compares the energy of the core levels (E_{CL}) and valence levels (E_V) in the bulk and thin films to determine the valence band offset (ΔE_V). ΔE_V is given by [230]:

$$\Delta E_V = (E_{CL}^{Si} - E_{CL}^{diel})_{Si/diel} - (E_{CL}^{Si} - E_V^{Si})_{Si} + (E_{CL}^{diel} - E_V^{diel})_{diel}. \tag{3.7}$$

Where the subscripts Si, $diel$ and $Si/diel$ indicate the bulk Si, bulk dielectric and thin film samples, respectively. The thin film (<3 nm) enables simultaneous signal detection from the dielectric and underlying silicon to determine the energy difference of the core levels (the first term in Equation 3.7). The thick dielectric and bare silicon samples determine the energy difference from the core levels to the valence band onset in each material. The energy levels for each term in Equation 3.7 are labelled on the energy diagram in Figure 3.7. Band bending at the surface of the films will affect the valence band and core levels equally. Therefore, any charge present will not affect the VBO determination.

The energies of the core levels are found by fitting the XPS peaks with a Lorentzian asymmetric line shape and either linear or Shirley background shape, depending on the binding energy of the core peak. Oxygen, nitrogen and Al peaks used a linear background and a Shirley background is used for the Si2p and Ti2p peaks. The Shirley background is used when the background signal is changing rapidly at the energy of the core peak. The valence band onset is the initial increase of

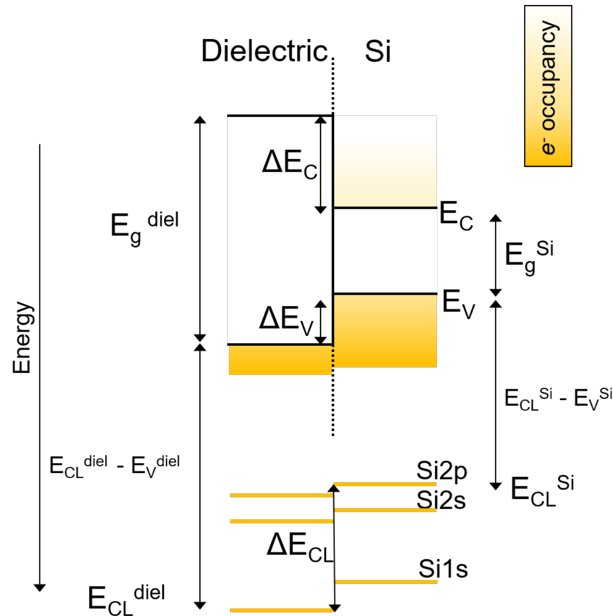


Figure 3.7: Energy Bands at a silicon/dielectric interface, with annotations indicating the energy differences used in the Krauts method to determine the VBO.

XPS signal at binding energies close to 0 eV. The energy of the valence band onset is determined by the intercept of a linear extrapolation of the leading edge to the background signal. The background is determined by linear extrapolation from -5 to -2 eV.

XPS gives quantitative information on the elemental composition of the samples, which can be used to determine the stoichiometry and thickness of the nanolayers. The intensity of the signal from each core level depends on the atomic concentration in the probed volume and the relative sensitivity factor (RSF) of the peak. To obtain highly accurate values of RSF, the system should be calibrated to standard reference samples. This was not deemed necessary for the analysis desired for this thesis. The values of RSF were found in reference tables. The CasaXPS reference library was used for the Thermo Scientific XPS [231], while the X-ray photoelectron handbook by Moulder [232] was used for the Phi XPS. Separate reference tables are required due to the different geometry of the TSK and PhiV systems. The reference tables were chosen as they gave close agreement for the stoichiometry of the bulk films. Errors in the RSF will lead to variation in the absolute values of stoichiometry and thicknesses determined. Comparisons can be made to measurements performed in the same system, however, caution must be taken when comparing measurements taken in different systems as was the case here. The deposition of bulk SiN_x and AlO_x films should be consistent, so a comparison of the stoichiometry obtained gives an indication of the disparity between the two systems. The RSF values are for homogeneous samples, so the stoichiometry of the thin films will not be as accurate.

3.3.1 Nanolayer Thickness Determination using XPS

The thickness of the nanolayer films is calculated from XPS spectra by comparing the relative intensities of core-level peaks from the Si substrate and the thin film. The maximum probing depth in XPS is ~10 nm so this technique is highly surface sensitive, even to films <1 nm. The nanolayer thickness is given by [233]:

$$t_{\mathrm{diel}} = \lambda_0 \cos\theta \cdot \ln\left(1 + \frac{I_o/s_o}{I_s/s_s}\right). \tag{3.8}$$

Where λ_0 is the electron attenuation length, θ is the emission angle, I is the intensity of the core peak, and s is the sensitivity factor. The subscript o refers to the thin dielectric film, termed the overlayer and subscript s refers to the Si substrate. This equation assumes the photo-electrons generated in the substrate and the overlayer have the same attenuation length in the overlayer. This breaks down when the core peak in the substrate has a significantly different energy from the core peak in the overlayer. The Thickogram method [234] used here, takes the different core energies into account. Several assumptions are required to estimate λ_0 in the dielectric films. A tilting stage can remove the need for these assumptions, however, this was not available. The attenuation lengths were calculated using the NIST electron attenuation length calculator [235]. The electron kinetic energy, stoichiometry, overlayer density and the geometry of the set-up are all required input parameters. The attenuation lengths of SiO_x, SiN_x, AlO_x and TiO_x are 3.5, 3.1, 2.8, and 2.5 respectively [235]. In Chapter 5 the technique is used to determine the thickness of SiO_x, SiN_x, AlO_x and TiO_x nanolayers and compared to the values measured with ellipsometry.

3.4 Current-Voltage, J-V

The resistivity of the structures is determined from current-voltage (J-V) measurements near 0 V. The total resistivity, ρ_{tot} is expressed as [236]:

$$\rho_{tot} = \rho_c + R_{spread} \cdot A_c + R_0 \cdot A_c. \tag{3.9}$$

Where R_{spread} is the spreading resistance in the silicon wafer and A_c is the contact area. The resistivity of interest is the front contact resistivity (ρ_c), which includes the dielectric nanolayer, the metal contact and any additional layers such as a poly-Si layer. R_0 contains all other resistivity components, namely the rear contact and the wire connections. To determine the contact resistivity, ρ_c must be isolated from ρ_{tot}. The two most common methods to do this are transfer line measurements, TLM, and the Cox Strack method, CSM [236]. Both techniques use multiple measurements to isolate ρ_c. For the majority of the resistivity measurements in this work neither of these methods were suitable due to large variations in the contact resistivity between identical contacts, as well as limitations of the techniques for low resistivity contacts [220]. As such, vertical J-V measurements of the structures shown in Figure 3.8 are made between ±0.1 V using a Keithley 2635B source meter. The total resistivity is calculated as:

$$\rho_{tot} = \left[\frac{\delta V}{\delta J}\right]_{V=0}. \tag{3.10}$$

A bare Si sample with a deposited metal contact was used as a control, this confirms that ρ_c in the structures is generally sufficiently high that ρ_{tot} is dominated by ρ_c. For the fired poly-Si contacts, this is not the case. The contact resistance is found by removing the theoretical spreading resistance of the Si wafer, $\rho_c = \rho_{tot} - R_{spread} \cdot A_c$. The contribution from R_0 is assumed to be small and is omitted from further analysis.

3.4.1 Theoretical fitting of J-V curves

The experimental J-V curves were fitted to theoretical models of the current. Figure 3.8 shows the sample structure with annotations of each contribution to the equivalent circuit. The contact resistivity is comprised of contributions from ρ_{tun} and ρ_{pin} in parallel. The total current (J_{tot}) is

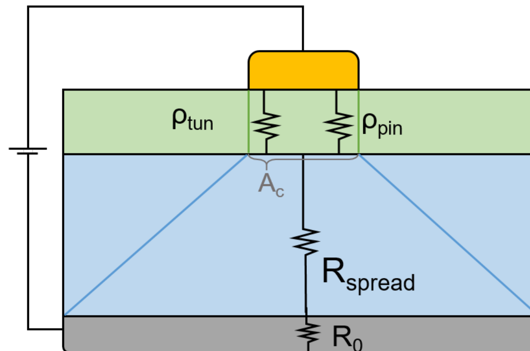


Figure 3.8: MIS sample structure with the resistive components annotated.

given by:

$$\frac{1}{J_{tot}} = \frac{1}{J_c} + \frac{1}{J_{spread}}, \tag{3.11}$$

$$J_c = J_{tun} + J_{pin}. \tag{3.12}$$

The theoretical tunnelling current is derived in Appendix A and is expressed as:

$$\mathrm{J}_{tun} = A^*T^2 \cdot P_t \cdot \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right]. \tag{3.13}$$

Where, P_t is the tunnelling probability, T is the temperature, ϕ_b is the Shottky barrier height, η is the idealist factor, V is the applied voltage and k is Boltzmann's constant. The spreading current, J_{spread}, is determined from R_{spread} which is given by a semi-empirical formula [237] as follows:

$$J_{spread} = V/R_{spread} \cdot A_c \tag{3.14}$$

$$R_{spread} = \frac{\rho_{waf}}{2\pi r_c} arctan\left(\frac{2t_{waf}}{r_c}\right) \tag{3.15}$$

Where r_c is the radius of the contact, ρ_{waf} is the wafer resistivity and t_{waf} is the wafer thickness. The pinhole contribution to the current takes a similar form,

$$J_{pin} = V/\rho_{pin} \tag{3.16}$$

$$\rho_{pin} = \frac{1}{N_{pin}} \cdot \frac{\rho_{waf}}{2\pi r_{pin}} arctan\left(\frac{2t_{waf}}{r_{pin}}\right). \tag{3.17}$$

Here, the contact radius is replaced by the the pinhole radius, r_{pin} and a prefactor is added to include the pinhole density, N_{pin}.

The resistivity extracted from the J-V curve can also be fitted from the equations above. This is used to fit the resistivity as a function of dielectric thickness or temperature, which provides the input parameters for fitting the J-V curves. The total resistivity is fitted from Equation 3.10 where contact resistivity includes both tunnelling and pinhole contributions,

$$\frac{1}{\rho_c} = \frac{1}{\rho_{tun}} + \frac{1}{\rho_{pin}} \tag{3.18}$$

The tunnelling resistivity is the inverse gradient of the J_{tun} (Equation 3.13) at V=0,

$$\rho_{tun} = \frac{nk_B}{qA^*T \cdot P_{tun}} \cdot \exp\left(\frac{q\phi_b}{k_B T}\right). \tag{3.19}$$

3.4.2 Temperature-Dependent J-V, T-JV

Low-temperature J-V measurements are used to separate the pinhole and tunnelling components of the contact resistivity. A CTI-Cryogenics 8200 helium compressor attached to a CTI-Cryogenics cold head is used to obtain a measurement temperature range from 100-300 K. A T-type thermocouple

was secured onto a dummy wafer to measure the temperature at the front surface of a silicon wafer on the sample stage. The thermocouple temperature differed slightly from that of the silicon diode sensor incorporated into the cold head, particularly at temperatures below 200 K. This is likely due to a temperature gradient between the the diode sensor and the silicon wafer surface.

3.5 Lifetime Measurements via Photo-Conductance Decay

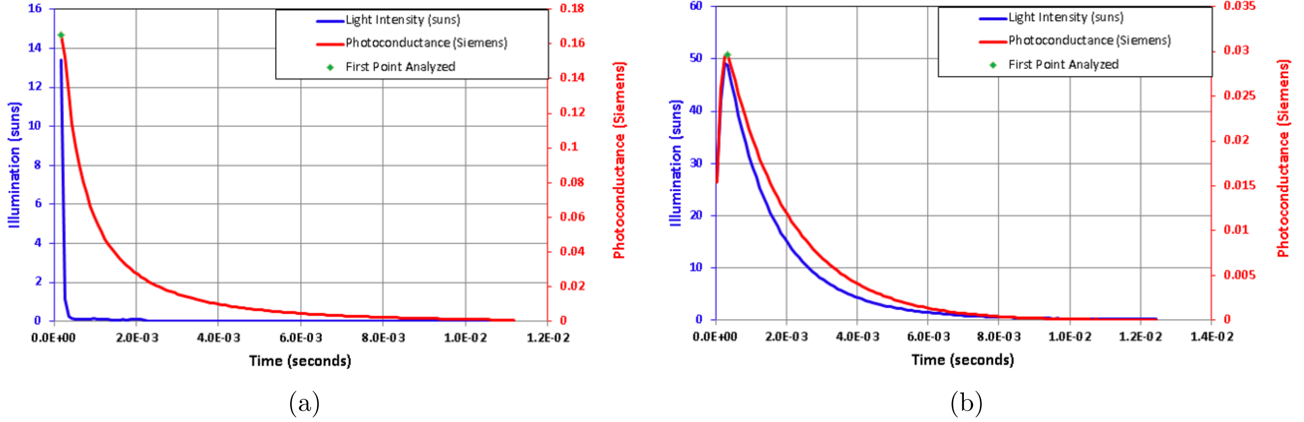
The effective lifetime is determined from photo-conductance decay measurements. The physical principles are introduced in Section 2.2.2. A WCT120 Sinton Lifetime Tester is used to measure the effective lifetime of samples in this work. Unless stated, lifetime samples have identical processing on the front and rear sides to allow easier extraction of the surface and bulk properties. The Sinton tester uses a flash of light to generate minority carriers in the sample and an induction coil to measure the induced conductivity. This is measured as a function of time to determine the number of generated carriers and the time they remain excited in the sample before recombining. The effective lifetime (τ_{eff}) is [52]:

$$\tau_{eff} = \frac{n(t)}{G(t) - \frac{dn(t)}{dt}}. \tag{3.20}$$

Where G is the generation rate, and n is the density of carriers.

There are two methods to extract the lifetime using the Sinton tester. The transient method uses a short flash and the photoconductance decay in the sample is measured after the light is switched off. The generation rate, G, is therefore 0 during the measurement. Quasi Steady State (QSS) mode has a significantly longer flash and the photoconductance is measured while the sample is illuminated. If the lifetime of the sample is $\ll$ the flash length, then the QSS is reached where the generation rate is equal to the recombination rate so $d\text{n(t)}/d\text{t} \approx 0$. A comparison of the two generation and photoconductance profiles is shown in Figure 3.9. In QSS mode, the generation rate in the sample is determined from a calibrated reference cell. The absorption of photons in the sample will depend on the thickness of the wafer and the optical properties of the sample surface. To convert the generation in the reference cell to the sample, an optical factor is used. For the polished planar samples used in this work, the optical constant was set to 0.7.

The minority carrier lifetime of a sample varies as a function of minority carrier density, due to the different recombination processes described in Section 2.2. Effective lifetimes measured in this work are quoted at 10^{15} cm^{-3}. The lifetime as a function of minority carrier density can be fitted to determine the dominant recombination mechanisms [238]. As stated in Section 2.2.2, J_0, SRV and iV_{OC} provide a better comparison between different substrate wafers. These parameters are extracted from lifetime curves using the Equations described in Section 2.2.2. The analysis used software available at[239], which uses the Kimmerle [240] and Mackel [241] models for extracting J_0.



(a) (b)

Figure 3.9: Illumination and photoconductance intensity for measurement of effective lifetime in a) transient and b) QSS modes

3.6 Capacitance-Voltage, C-V

Capacitance-voltage (C-V) measurements are used to extract the density of interface states, D_{it}, and the dielectric fixed charge, Q_f, of a semiconductor/dielectric interface. Figure 3.3(a) shows the sample structure for these measurements. A D.C. bias is applied to the metal (V_g) with a superimposed A.C. voltage d. V_g is varied to alter charge dynamics at the Si surface. In high-frequency C-V measurements, the Si/dielectric interface is in one of three regimes: accumulation, flat-band, or depletion. The band diagrams for each regime are depicted in Figure 3.10 for the example of an n-Si wafer. The contributions to the capacitance in each regime are shown by the equivalent circuit diagrams in Figure 3.10. Figure 3.11 shows an example C-V curve for a 100 nm SiO_x.

In accumulation (Figure 3.10(a)), the gate bias induces high concentration of majority carriers at the silicon surface. The silicon surface has a high conductivity and the MIS device behaves as a parallel plate capacitor [242]. The capacitance of the dielectric is expressed as:

$$C_{diel} = \frac{\varepsilon_0 \cdot \varepsilon_{r,diel} \cdot A_c}{t_{diel}} = C_{acc}. \tag{3.21}$$

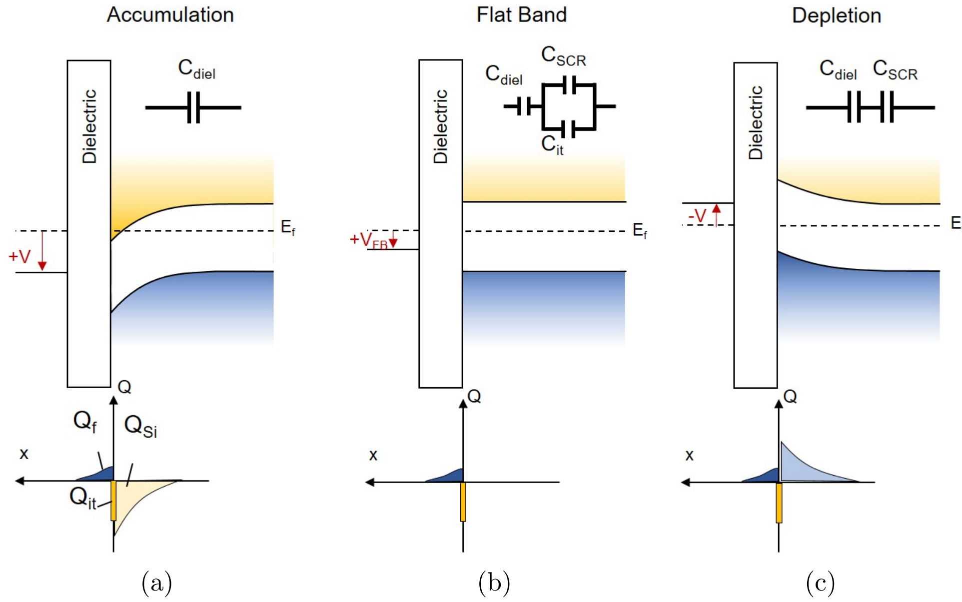
Where ε_r is the relative permittivity of the dielectric and ε_0 is the permittivity of free space.

In depletion, the V_g repels the majority carrier from the Si/dielectric interface (Figure 3.10(c)). The low majority carrier concentration at the silicon surface results in the bands bending near the Si surface. This is known as the space charge region and has an associated capacitance, C_{SCR}. C_{SCR} is given by [242],

$$C_{SCR} = \frac{\varepsilon_{r,Si} \cdot \varepsilon_0 \cdot A_c}{W_d}, \tag{3.22}$$

$$W_d = \sqrt{\frac{4 \cdot \varepsilon_{r,Si} \varepsilon_0 \cdot \phi_F}{q \cdot N_d}}. \tag{3.23}$$

Where ε_{Si} the relative permittivity of silicon, W_d is the width of the space charged region, ϕ_F is



(a) (b) (c)

Figure 3.10: The top figures show band diagrams of an MIS structure in a) accumulation, b) flat-band c) depletion. The distribution of charge in the semiconductor and insulator is shown below and the insets show the equivalent circuit diagram in each regime.

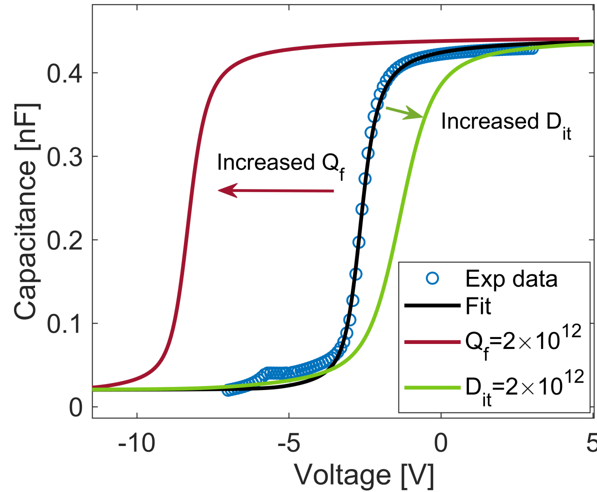


Figure 3.11: High-frequency CV curve of a 100 nm SiO_x on n-type Si, with fitting parameters.

the Fermi energy of the Si and N_d is the dopant concentration. The C_{SCR} is in series with C_{diel} so the capacitance in the depletion region, C_{dep} is given by,

$$\frac{1}{C_{dep}} = \frac{1}{C_{diel}} + \frac{1}{C_{SCR}}. \tag{3.24}$$

In high-frequency measurements, the switching speed is too high to enable the minority carriers to generate a region of high conductivity in the Si. When the frequency is lowered, the minority carriers can accumulate and generate an inversion layer in the silicon. In n-type Si, an inversion

layer is a high density of holes at the Si surface, forming a region of p-type Si. The inversion layer has a high conductivity and so the MIS behaves as a parallel plate capacitor. The capacitance in inversion is $C_{inv} = C_{diel} = C_{acc}$. A high-frequency is used for the measurements in this thesis so an inversion layer is not formed.

The transition from depletion to accumulation is dependent on the properties of the Si/Dielectric interface. The flat band condition is when there is no charge in the SCR (Figure 3.10(b)). The applied voltage required to reach this condition is the flat band voltage (V_{FB}) and occurs when the charges in the MIS contact are balanced. V_{FB} is given by [243],

$$V_{FB} = \frac{\Phi_{MS}}{q} + \frac{qC_{it}(t_{diel} - x_c)}{\varepsilon_{r,diel}} - \frac{Q_f(t_{diel} - x_c)}{\varepsilon_{r,diel}}. \quad (3.25)$$

Where Φ_{MS} is the metal-semiconductor work function difference, Q_f is the fixed charge density in the dielectric, x_c is the assumed charge centroid in the dielectric, and C_{it} is the interface state capacitance. x_c is assumed to be near the Si/dielectric interface, so the influence of Q_f on V_{FB} is larger when the dielectric thickness increases. C_{it} is directly proportional to the density of defect states at the silicon/dielectric interface. It is in parallel to the C_{SCR} and has the largest contribution to the measured capacitance near the flat band voltage (V_{FB}) shown in Figure 3.10(b). A high D_{it} and therefore C_{it} results in a slower transition between the depletion and accumulation regimes in the C-V curve, indicated by the green line in Figure 3.11.

To perform measurements, the MIS structure (Figure 3.3(a)) is fabricated, with 1 mm circular contacts. An Agilent E4980A precision LCR meter is used to sweep the voltage from the depletion region to accumulation to find the V_{FB}. Once the V_{FB} is determined, a detailed measurement is taken with a 20 s initialisation delay and a 1 s step delay. The A.C. signal is set to 0.05 V and the frequency is varied between 1-1000 kHz. The density of interface states as a function of the band gap energy is modelled as a constant value at the mid gap and an exponentially increasing density towards the band edges as has been done in other work [6]. The defects near the midgap, $D_{it,mg}$, are the most effective recombination centres, therefore $D_{it,mg}$ has the strongest influence on the chemical passivation of the interface [6].

3.6.1 Conductance-Voltage, G-V

G-V is measured simultaneously to C-V so the instrument acquisition parameters are the same as above. The G-V characteristics depend on the Si-dielectric interface properties and can be used to obtain Q_f and D_{it}, as per the methodology by Nicollian and Goetzerber [244]. For the thin dielectrics measured in this work, the contribution of interface states is marginal compared to the charge flow through the film and therefore this method does not apply. An adapted method to determine Q_f for the highly conductive dielectrics is developed and is discussed in Chapter 7.

3.7 Kelvin Probe

The Kelvin probe (KP) measures the potential at the surface of a sample. It uses a gold tip and backing voltage to find the contact potential difference (CPD) between the tip and the sample. Figure 3.12 shows a schematic of the measurement. A gold tip is vibrated above the sample resulting

in a sinusoidal variation in the capacitance between the sample and tip (C_K). Using $Q = VC$, $I = dQ/dt$ and $V = IR$, the variation in the voltage can be determined [245],

$$Q_s = (CPD + V_b) \cdot C_K, \tag{3.26}$$

$$I_K(t) = (CPD + V_b) \cdot C_K \cdot d/d(t), \tag{3.27}$$

$$V_{ptp} = (CPD + V_b) R_f \cdot G C_0 \cdot e \cdot \omega sin(\omega t). \tag{3.28}$$

Where R_f is the I/V converter feedback resistance and G is the pre-amplifier gain. V_b is measured at ±5 V, to ensure the signal is large compared to background noise. A linear interpolation is used to find the V_b where V_{ptp} will be zero [245]. At this point V_b = -CPD. The gradient of $V_{ptp}(V_b)$ is dictated by the ratio between the maximum and minimum distance of the probe to the sample. A low probe-sample distance is desired to obtain a high gradient and a more accurate calculation of V_b but there is a risk of the probe crashing into the sample. A gradient of ~300 is used, which is in the range of a few tens of micrometres.

The CPD is determined by metal-sample WF difference, the potential in the semiconductor SCR, the voltage across the dielectric (V_{diel}) and the voltage in the air gap between the sample surface and probe (V_{air}). CPD is given by [78],

$$CPD = -\left(\frac{\Phi_{ms}}{q} + \phi_s + V_{diel} + V_{air} \right) \tag{3.29}$$

Where ϕ_s is the potential across the SCR in the silicon, indicated in Figure 3.12(a). It is assumed the experimental setup is without electrical interference, and therefore the contribution of charge from the air is negligible. V_{diel} is generated due to a distribution of fixed charge in the dielectric

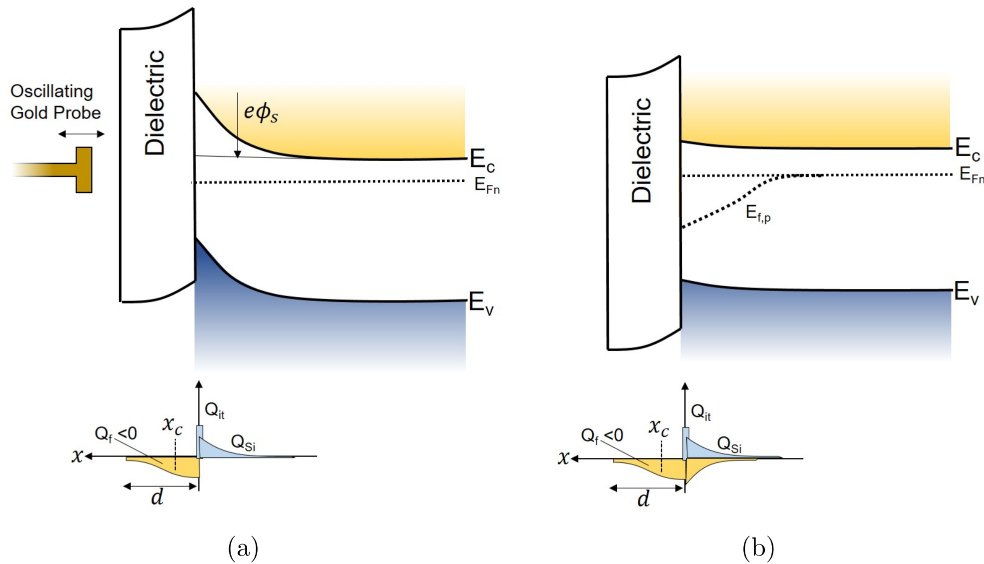


Figure 3.12: a) Schematic of KP measurement for a dielectric with a high negative charge on n-Si a) in the dark and b) under illumination. The charge distribution in the silicon and dielectric is indicated below.

[78],

$$V_{diel} = \frac{1}{\varepsilon_{r,diel}\varepsilon_0} \int_0^d x\rho_{diel}(x)dx. \tag{3.30}$$

As with CV measurements, it is not possible to know the exact distribution of charge in the dielectric, so a charge centroid is assumed,

$$V_{diel} = \frac{x_c Q_f}{\varepsilon_{r,diel}\varepsilon_0}. \tag{3.31}$$

Where x_c is the distance from the silicon surface. When inserted into the Equation 3.29,

$$\text{CPD} = -\left(\frac{\Phi_{ms}}{q} + \phi_s + \frac{x_c Q_f}{\varepsilon_{r,diel}\varepsilon_0}\right), \tag{3.32}$$

It can be seen from Equation 3.32, CPD is most sensitive to charge located on the surface of the dielectric, far from the Si/Dielectric interface. This is in contrast to CV measurements, which are more sensitive to charge at the Si/Dielectric interface. ϕ_s is found using an iterative process to find the condition of charge neutrality in the Si/dielectric structure the following condition is met,

$$Q_f + Q_{SCR} + Q_{it} = 0. \tag{3.33}$$

Where Q_{it} is the charge arising from interface states. The number of charged interface states is dependent on the relative number of acceptor and donor interface states, as discussed in Section 2.1.2. Q_{it} depends on the position of the Fermi level at the silicon surface, and hence the need for iterative calculations.

3.7.1 Surface Photovoltage

Under illumination the concentration of minority carriers at the surface increases and so the population of carriers becomes balanced, leading to a decrease in band bending and hence reducing the ϕ_s term from Equation 3.29. This is shown in Figure 3.12(b). The reduction in ϕ_s is found using the methodology set out in [246] by determining the steady state carrier concentration in the silicon generated when the sample is under illumination. Using ray tracing, the generation profile is determined for the 10 mW/ cm^2 intensity of the KP set-up. The resulting injection density is dependent on the lifetime of carriers in the sample and sample geometry. Δn is varied to provide a good fit of CPD against Q_f. An example of this is included in Appendix D.

The surface photovoltage (SPV) is defined as SPV=$CPD_{dark} - CPD_{light}$. For both KP and SPV measurements, an SKP5050 scanning Kelvin probe instrument from KP Technologies is used to generate a map of 6×6 to 10×10 points (corresponding to a scan area of 1-4 cm^2) in the dark, then under the 10 mW/ cm^2 illumination. At each point, the CPD is averaged over 5 measurements with a measurement delay of 200 µs. The CPD value for a range of D_{it} and Q_f values is calculated for both dark and light measurements using software available at [247]. The measured values of CPD_{dark}, CPD_{light}, and SPV are compared to the theoretical CPD values.

Chapter 4

Understanding Hole Selective Contacts Through Device Simulations

In sections 2.6 and 2.9 the potential benefits of alternative dielectrics to SiO_x for hole selective passivating contacts were discussed. The key considerations are: the valence band offsets, the fixed charge in the dielectric, and the doping profile in the Si after the post-deposition anneal of poly-Si. Simulations allow each of these considerations to be varied independently and their effect on the resistivity and passivation quality of the contact can be studied. Simulations isolate each parameter to develop an improved understanding of the contact structures to complement experimental work on the novel thin films. Several simulation packages have been used for the investigation of poly-Si structures including Sentaurus TCAD [139], [146], [248], [249], AFORS-HET [153], [250]–[252], Quokka [253], and Marco-POLO [215], [254].

Simulations were first used to illustrate the efficiency enhancement achieved by passivating the contact area. Glunz [253] compared iV_{OC} achieved for a given dark saturation current (J_0) and the contact area fraction, A_f. If J_0 under the contacts is 40 fA/cm^2, a full-area contact can reach an iV_{OC} of 700 mV. Reducing the contact area, and passivating the remaining area with a high-quality thick dielectric, results in a further increase in iV_{OC}. However, there is a trade-off between the passivation quality and current transport in the cell. A smaller contact area requires a lower contact resistivity (ρ_c) to avoid a high series resistance in the cell. Achieving high passivation and low contact resistivity simultaneously is a significant complexity for developing passivating contacts.

Brendel et al. [255] sought to define the quality of a passivating contact using a single metric. They coined the term 'Selectivity', defined as:

$$S = \frac{\mathrm{v}_{th}}{\rho_c \mathrm{J}_0}, \tag{4.1}$$

$$S_{10} = \log\left(\frac{\mathrm{v}_{th}}{\rho_c \mathrm{J}_0}\right). \tag{4.2}$$

The Selectivity is given by the ratio of majority to minority carrier resistivity across the interface. The majority carrier resistivity is simply the contact resistivity, ρ_c, and the minority resistivity is obtained from the dark saturation current and the thermal voltage, v_{th}. It is quoted as the $\log_{10}$ of this ratio, and termed S_{10} (Equation 4.2). Figure 4.1 shows how the Selectivity relates to

the maximum potential efficiency of the cell. It is clear that Selectivity offers a useful indication of the quality of a contact, however, in certain regimes either J_0 or ρ_c will have a much stronger influence on the efficiency. For example, in the top left corner of Figure 4.1, the contact resistivity is low and the contact dark saturation current is high. Reducing the contact resistivity further will increase the value of Selectivity, but have no influence on the efficiency of a cell. At a single value of Selectivity, there can be a substantial difference in the maximum efficiency.

The physics of the contacts has also been studied. The tunnelling current through nanolayer dielectrics in metal/insulator/silicon (MIS) or silicon/insulator/silicon (SIS) structures has been studied for several decades [107], [256]–[258], most notably to determine leakage currents in MOSFETs and for bipolar transistors. The models developed can now be applied to passivating contact structures, with additional conduction mechanisms such as pinholes also included in the models. Steinkemper [248] showed that for an electron selective tunnelling contact a SiO_x layer thicker than 1.5 nm results in a drop in the fill factor. Hole selective contacts have a lower thickness tolerance of around 1.2 nm [139], [259]. For thicker SiO_x layers, pinholes are required to form low resistivity contacts. A 2 nm SiO_x layer requires a pinhole density of 10^6 cm^{-2} for a contact resistivity <100 mΩ·cm^2 [215]. Meanwhile, calculations of J_0 show that if $D_{pin}>10^6$, the highly defective Si/metal contact created at pinholes contributes to an increase in the J_0 of the contact [215]. This agrees closely with the work of others [153], [252], [260]. The balance between a sufficiently high pinhole density required to form a low resistivity contact and a sufficiently low pinhole density required for a highly passivating contact contributes to a narrow processing window required to achieve low resistivity and highly passivated pinhole contacts [111].

The concentration and spacial variation of dopants (the doping profile) near the Si surface also has an important impact on the contact parameters. The in-diffusion of dopants from the

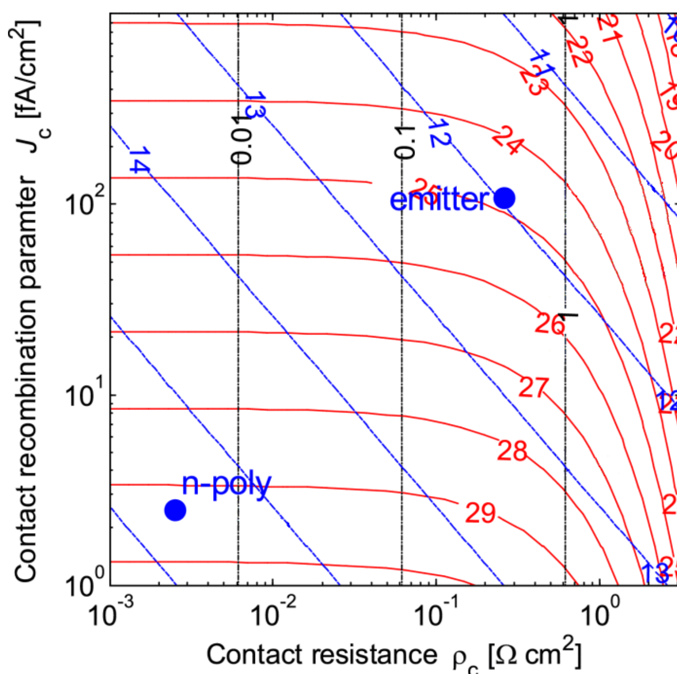


Figure 4.1: Selectivity, Efficiency and optimal contact area fraction as a function of J_0 and ρ_c. Blue lines show the Selectivity, red lines show the maximum efficiency and black lines show the optimum area fraction. The efficiency values are for a full-area contact. Adapted from [255].

poly-Si, through the dielectric, and into the Si wafer after the high temperature anneal can lower the resistivity of a tunnelling contact [139], [248]. The passivation quality of tunnelling and pinhole contacts is influenced by the shape of the dopant profile. Wei et al. [261] compared the iV_{OC} and the in-diffusion depth while varying the density of the interface states. They show that as the D_{it} increases, the optimum diffusion depth increases. Additionally, a sample dominated by pinhole conduction also requires a higher poly-Si doping concentration to reach the maximum iV_{OC}. The higher doping limits the recombination at the pinhole areas which are not passivated. Conveniently, as there is no oxide layer to block diffusion at the pinholes, in-diffusion is often enhanced under the pinholes, forming the desirable higher doping concentration [249]. There is not a single 'ideal' doping profile for passivating contacts, as the most effective doping profile for a given contact is dependent on the other properties of the contact.

There have been fewer studies on the effect of dielectric charge in poly-Si contacts, presumably due to the low intrinsic charge in SiO_x. However, with recent investigations into alternative dielectrics such as SiN_x, AlO_x, and TiO_x, the charge intrinsic to such dielectric nanolayers becomes crucial. Surface passivation from thick dielectric layers, including the chemical and field-effect passivation, has been extensively modelled using theoretical calculations [52], [262] and Sentaurus TCAD [263]. The understanding developed for the thick dielectrics can now be implemented into passivating contact structures where charge also flows across the dielectric.

The band structures in DFPCs are crucial for achieving low ρ_c as no beneficial doping is present. Messmer et al. [264] studied high WF metal oxide contacts. For hole contacts, a highly negative conduction band offset (CBO) between the a-Si and the metal oxide is required to allow holes transport (as shown in Figure 2.8(b)), or trap states must be present to allow conduction. Attafi et al. [265] added defects in the metal oxide and simulated the trap-assisted tunnelling. This showed an increase in fill factor with the addition of the defect states. Simulations have not yet been utilised to investigate the effect on contact resistivity and passivation quality when a fixed charge is present in DFPC structures.

In this chapter, a combination of theoretical calculations and Sentaurus TCAD simulations are used to understand how the band offsets, the interface charge in the dielectric, and the doping profile will alter the contact properties. The theoretical calculation of tunnelling probability and tunnelling current are used to determine the contact resistivity for each dielectric, then Sentaurus is used to validate the calculations. The simulations of ρ and J_0 are used to obtain target values and limits for the thickness and intrinsic charge in the contact structures, as well as to improve the understanding of the impact of the doping profile in poly-Si structures.

4.1 Theoretical Calculations of Tunnelling Probability

Tunnelling is an important phenomenon in many passivating contact structures. The key equations to study the tunnelling of carriers though a MIS contact structure were derived in Appendix A and it was shown that the tunnelling probability through a dielectric material is highly dependent on the nanolayer thickness (t_{diel}), the effective mass, and the energy barrier that the carriers need to surmount, i.e. the band offset between the dielectric and silicon. Figure 4.2 compares the probability of electron and hole tunnelling for SiO_x, SiN_x, AlO_x, and TiO_x. Table 4.1 gives the range of reported values for the band offsets and effective masses for each dielectric represented by

the shaded areas of Figure 4.2. In some cases, the range is large, which results in a wide spread of potential tunnelling probabilities. The large range can be due to (i) variation between modelled values and experimental values (ii) sensitive experimental techniques that are difficult to perform consistently (iii) different deposition techniques and (iv) different post-processing. The solid lines indicate the values used for the simulations in the rest of this chapter. The valence band offset (VBO) for SiO_x, SiN_x, and AlO_x are the measured values from Chapter 5. The effective masses, CBOs, VBO of TiO_x were the most commonly reported values. Table 4.2 details the values used for all subsequent theoretical calculations and finite element simulations.

A 1.5 nm SiO_x nanolayer provides sufficient electron tunnelling for a low ρ_c electron contact. The equivalent thickness required for a low resistivity hole contact is 1.2, 1.5, 1.8 and 1.5 nm for SiO_x, AlO_x, SiN_x, TiO_x respectively. Only SiN_x has a higher probability of hole tunnelling, compared to electrons. However, the band offset of the minority carrier has no effect on the contact properties of poly-Si contacts [250]. This is because the doping profile can provide the Selectivity. The primary importance of the dielectric band offsets is to ensure a low resistivity tunnelling contact. The low VBO for AlO_x and SiN_x hole contacts, allows a greater thickness to be tolerated compared to the SiO_x currently used.

From the band offsets TiO_x has extremely favourable properties for electrons. In this thesis TiO_x is investigated as a hole contact. The TiO_x layers used are ∼5 nm thick, so the transport mechanism is unlikely to have direct tunnelling contributions. Matsui et al [194] propose that interface traps near the silicon valence band energy provide a conduction path through the TiO_x. An alternative path could be from pinholes, formed during metallisation though the conduction mechanism has not yet been investigated. Nevertheless, since the main conduction mechanism for holes is not direct tunnelling, the simulations and calculations in the rest of the chapter could not be applied to the TiO_x. The tunnelling probability calculated in this section is used to compare the tunnelling current through SiO_x, SiN_x and AlO_x contact structures using theoretical calculations and device modelling.

Table 4.1: Literature Values of band offset parameters and effective mass.

Dielectric	CBO	VBO	Electron m*	Hole m*	Ref.
SiO_x	3.1–3.8	4.3–4.54	0.3–0.5	0.3–0.58	[186], [257], [258], [266]–[279]
SiN_x	1.8–2.4	1.1–1.9	0.5–0.6	0.3–0.55	[4], [280]–[285]
AlO_x	2.1–2.7	2.9–3.75	0.35–0.47	0.4–0.47	[180]–[184], [286]–[288]
TiO_x	0.05–0.3	2–3.4	0.1–0.5	0.1–0.8	[103], [196], [203], [289]–[293]

Table 4.2: Values used for simulations.

Dielectric	CBO	VBO	Electron m*	Hole m*
SiO_x	3.2	4.3[a]	0.4	0.4
SiN_x	2.2	1.4[a]	0.5	0.5
AlO_x	2.7	3.5[a]	0.4	0.4
TiO_x	0.1	3.3	0.3	0.4

[a] Measured

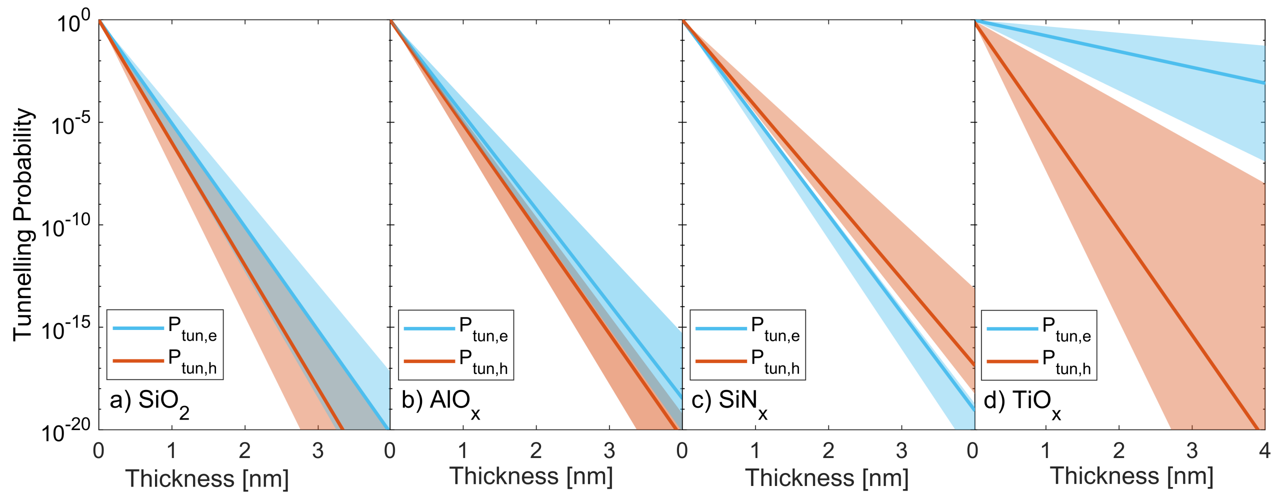


Figure 4.2: Tunnelling probability of electrons and holes a) SiO_x b) AlO_x c) SiN_x, and d) TiO_x. Values used are found in Tables 4.1 and 4.2.

4.2 Sentaurus TCAD Finite Element Simulation Set-Up

Sentaurus TCAD is a finite element modelling package that performs detailed simulations of semiconductor devices. Here it is used to simulate poly-Si contacts to determine the effect of charge and doping profiles on the transport and passivation properties. In device simulations, generating a mesh is crucial to define the structure's geometry. The mesh acts as a framework, determining the 2-D points where the simulation calculations occur. It is important to ensure the mesh has enough points for the calculations to converge, but not so many that the simulation will take an excessive amount of time. In an effective mesh, the points are concentrated in regions where the properties are changing rapidly i.e. near interfaces in the cell. Along with the mesh, input files are generated to detail the material properties in each region. The physical models to be used are also included in Table 4.3.

To perform the simulation, Sentaurus solves Maxwell's four continuity equations for electromagnetism at each mesh point. These are:

$$\nabla \cdot E = \frac{\rho}{\varepsilon_0}, \tag{4.3}$$

$$\nabla \cdot B = 0, \tag{4.4}$$

$$\nabla \times E = -\frac{\partial B}{\partial t}, \tag{4.5}$$

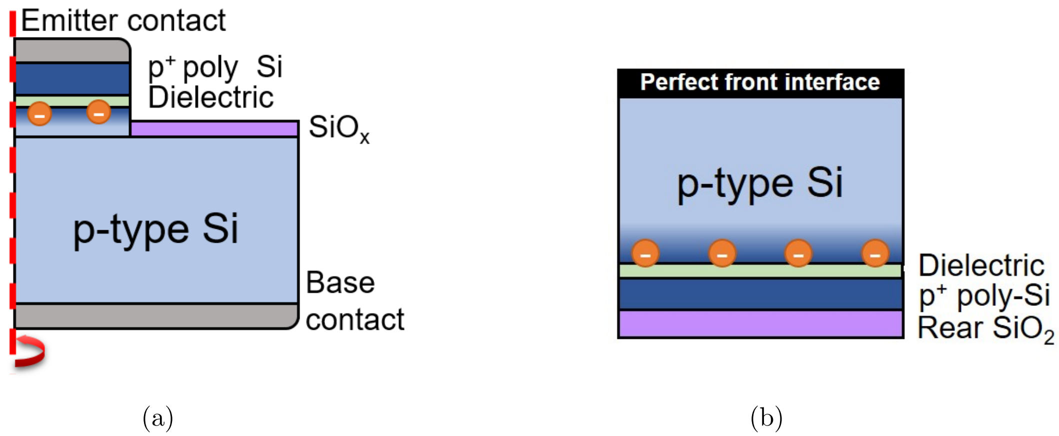
$$\nabla \times B = \mu_0 \left(J + \varepsilon_0 \frac{\partial E}{\partial t} \right). \tag{4.6}$$

Where ∇ is the 3-D gradient operator, B is the magnetic field, E is the electric field, ρ is the charge density, and μ_0 is the permeability of free space. The inputted device structure, electrodynamic models in Table 4.3, and applied external conditions enable the simulation of solar cell device parameters η, V_{OC}, J_{SC}, and FF. The structures simulated here were used to extract the specific contact properties, ρ_c and J_0. Figure 4.3 shows schematics of the structures.

Table 4.3: Default Values for Sentaurus Simulations

Parameter	Value
Wafer resistivity	1 Ω·cm (p-type)
Temperature	300 K
Poly-Si doping[a]	1.3×10^{20} cm^{-3}
Boron Diffusion[a]	Gaussian, peak = 3×10^{19} cm^{-3}, depth = 0.4 µm
Recombination Models	SRH [294], Auger [106], Radiative [295]
Mobility Models	Philips unified mobility model [296]
Band gap Narrowing	Schenk low injection [297]
Tunnelling (ρ_c))	Non-local tunnelling model using Schenk and Hassens [257]
Contact Model	Work Function
Optical injection (J_0)	Homogeneous optical injection of 1.2×10^{19} cm^{-2}
S_{p0}, S_{n0} (J_0)[a]	300, 3000 cm/s

[a] Unless specified otherwise



(a) (b)

Figure 4.3: Schematics of simulated poly-Si structure for a) contact resistivity simulations, b) J_0 Simulation.

In Sections 4.4.2, 4.5.2 and 4.6 the influence of the boron dopant profile on the contact properties is studied. The doping profiles can alter the concentration majority carriers at the interface, and the gradient of the doping concentration across the dielectric layer is a source of field-effect passivation, additional to any FEP from the fixed charge in the dielectric. The doping profiles in these simulations have a constant boron concentration in the poly-Si layer and a Gaussian profile details the in-diffusion into the wafer with a set peak concentration and diffusion depth. Figure 4.4 shows the doping profiles simulated. The poly-Si ($[B]_{\text{poly-Si}}$) is varied, with the peak concentration of the in-diffusion ($[B]_{\text{waf,peak}}$) scaled to $[B]_{\text{poly-Si}}/10$. This is used to determine the importance of the majority carrier (boron) at the Si/dielectric interfaces. Additional simulations are carried out in Appendix C, where the poly-Si doping concentration fixed and the peak doping in the in-diffusion is varied. This determines the effect of the built-in field across the dielectric.

4.2.1 Resistivity Simulation

The resistivity of the contact structures is determined from a simulated J-V curve. The total resistivity ρ_{tot} is taken from the inverse gradient of the curve, $\rho_{tot} = \left[\frac{\delta V}{\delta J}\right]_{V=0}$. The contact resistivity

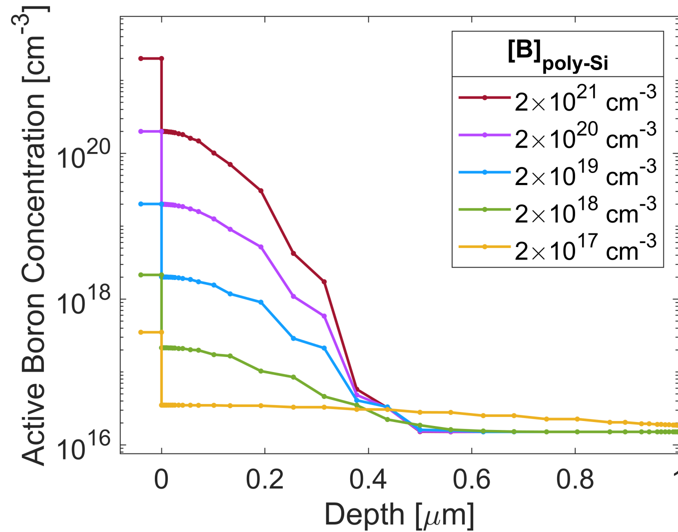


Figure 4.4: Doping profiles for a) varying dopant concentration in the poly-Si and b) varying peak dopant concentration in the wafer. The dielectric interface is at 0 μm.

is extracted by simulating a reference device without the contact stack and in-diffused region, and with a perfect front contact so only the wafer spreading resistance and rear contact resistance are present. The resistivity of the reference simulation was calculated to be 19.18 mΩ·cm^2 for a 1 Ω·cm base resistivity, therefore the contact resistivity is $\rho_c = \rho_{tot}$-19.18 mΩ·cm^2.

Cylindrical symmetry is used to mimic the circular contact used for experimental measurements. Figure 4.3(a) shows the ρ_c simulation structure. with the red dashed line indicating the rotation axis. The poly-Si contact stack was isolated from the rest of the wafer to restrict the lateral conduction in the in-diffused region. This matches the structure fabricated for experimental J-V measurements (Figure 3.3(b)). A simulation width of 1 mm is chosen to ensure the spreading resistance is fully considered, without adding unnecessary mesh points.

4.2.2 Passivation Simulation

The method developed by Kane and Swanson [298] is used to simulate the J_0 in passivating contact structure shown in Figure 4.3(b). A uniform illumination is used to generate carriers in the bulk of the wafer, though the illumination does not extend throughout the full wafer. For the simulation, the inputted illumination is the initial condition, then the illumination is turned off to stop generating carriers and the current is measured very near the Si/dielectric interface. During the simulation, the carriers recombine at the Si/dielectric interface. The current is measured over time to give the dark saturation current as a function of excess carrier concentration.

4.3 Effect of Dielectric Thickness on Contact Resistivity

The tunnelling probability calculations in Section 4.1 showed that the SiN_x and AlO_x have higher probabilities for hole tunnelling compared to SiO_x. This enables lower resistivity tunnelling contacts to be fabricated or, the same resistivity can be achieved using thicker layers, allowing more processing flexibility. The tunnelling current is calculated to determine the allowable thicknesses

of each dielectric. Figure 4.5 shows the total resistivity of the silicon/dielectric/poly-Si structure shown in Figure 4.3(a) as a function of t_{diel}. There is no interface charge present in any of the dielectrics.

The resistivity of the structures shows two clear regimes. At low thickness, the resistivity is independent of t_{diel}, as the resistivity is limited by the spreading resistance in the silicon wafer. At larger thicknesses the resistivity increases exponentially with t_{diel}, this indicates that ρ_{tot} is limited by the dielectric's tunnelling probability. As seen from Figure 4.2, SiN_x has the highest hole tunnelling probability, hence the lowest resistivity. The SiO_x has a low tunnelling probability as is indicated by the steep slope and low thickness at which tunnelling dominates. For a passivating contact the resistivity should be below around 100 mΩ·cm^2 to avoid a significant drop in the fill factor of the cell. This occurs at 1.25 nm for SiO_x, 1.4 nm for AlO_x, and 2 nm for SiN_x nanolayers.

4.3.1 Comparison of Sentaurus TCAD and Theoretical calculations

The total resistivity as a function of dielectric thickness was used to confirm that the results from theoretical calculations match the Sentaurus simulations. Figure 4.5 shows the theoretical calculations for SiO_x, SiN_x and AlO_x as solid lines and open shapes indicate the Sentaurus measurements. The two methods show good agreement in both the spreading resistance and tunnelling regime. The slight discrepancy is most likely due to the more sophisticated nature of the Sentaurus models. The theoretical calculation of spreading resistance is an approximation developed from empirical results [236], [299]. The tunnelling model in Sentaurus uses an analytical model developed by Schenk [294] and considers the image force lowering compared to the direct tunnelling current used in the theoretical calculation [107]. Despite the two models used, the results are very comparable. In the following sections, the advanced capabilities of Sentaurus are used to perform more complex resistivity simulations, where the effects of contact structure, dielectric charge and doping profiles are considered. The theoretical calculations are used in Chapter 6 to provide fitting to the experimental results.

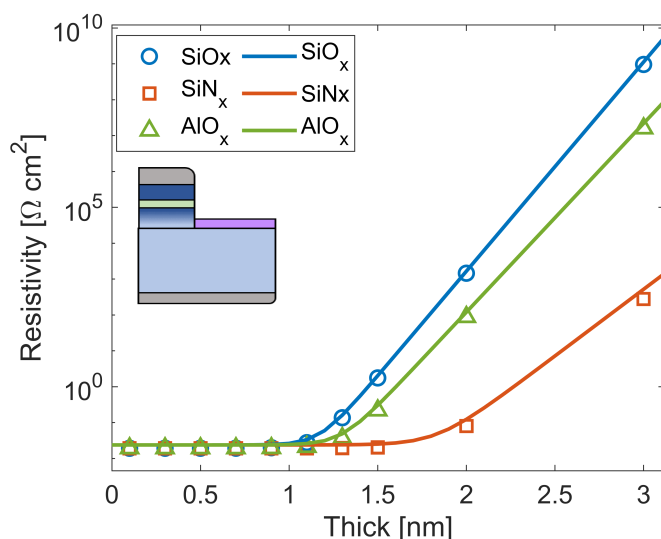


Figure 4.5: Total resistivity of a poly-Si contact structure. Solid lines indicate the theoretical calculations and open shapes indicate the Sentaurus TCAD simulations.

4.4 Effect of Interface Charge on the Contact Resistivity

It is well known that SiN_x and AlO_x have an internal fixed charge [52]. The influence of this charge on the resistivity and passivation of contact structures is investigated in the next section. A charge in the dielectric alters the concentration of majority carriers at the interface, which will influence the band bending in the silicon. The VBO is not affected, so the tunnelling probability is unchanged. However, the tunnelling current is influenced by the band bending at the silicon surface, so the transport properties are dependent on the dielectric charge. A SiN_x nanolayer is used for the following examples but the behaviour of SiO_x or AlO_x would be very similar. The simulation structure and parameters are as shown in Figure 4.3(a) and Table 4.3 and the charge concentration is varied at the silicon/dielectric interface.

4.4.1 Effect of Charge on Contact Resistivity for Varied Dielectric Thickness

Figure 4.6 shows the effect of dielectric charge on the contact resistivity for three different SiN_x thicknesses. For charge concentrations below 10^{12} cm^{-2} there is very little effect on the resistivity. At a high negative charge an accumulation layer of holes forms, which decreases the contact resistivity, while a large positive charge causes a depletion of holes, which increases the resistivity. Despite this, ρ_c has a stronger dependence on the dielectric thickness. A very high negative charge of $2{\times}10^{13}$ q/cm^2 is equivalent to a thickness reduction of $\sim$0.2 nm of SiN_x. If these simulations were carried out with SiO_x or AlO_x the thickness dependence would be even more significant as is seen by the steeper curves in Figure 4.5. Hence, while a negative charge has a beneficial effect on ρ_c, a high hole tunnelling probability through a low VBO and low thickness is crucial for achieving a low resistivity contact.

The relative reduction in ρ_c at high negative charge for the 1.4 nm SiN_x layer is smaller than for 1.8 nm and 2.2 nm. This is because the tunnelling resistance is no longer the only major contribution to the contact resistivity. At very low resistivities, the poly-Si series resistance becomes a significant contribution to ρ_c. The resistance of the poly-Si is not influenced by the interface

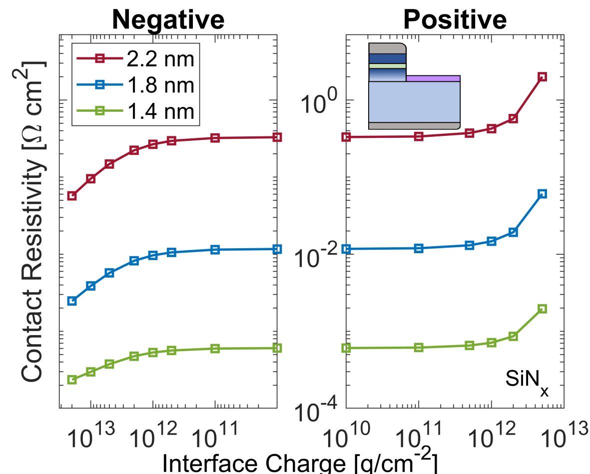


Figure 4.6: The effect of interface charge on the resistivity of a poly-Si structure for different SiN_x thicknesses.

charge so a smaller effect of the charge on ρ_c is seen. The series resistance of the poly-Si will dictate the minimum possible contact resistivity of the structure.

4.4.2 Influence of Doping Profiles on the Contact Resistivity

The dopant concentration in the poly-Si and in the in-diffused region also affects the concentrations of charge carriers at the dielectric interfaces. Therefore, the contact resistivity can depend on the doping profile in a poly-Si contact. Further Sentaurus simulations were carried out to determine how the interplay between the dielectric charge and the doping profile will influence the contact resistivity. A 2 nm SiN_x is used as the dielectric, though again, a SiO_x or AlO_x would behave in the same manner.

The poly-Si dopant concentration is varied, with the in-diffusion peak dopant concentration scaled by setting $[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$. This ensures the built-in electric field across the interface is the same for each doping profile. The red curve shows the contact resistivity for the highest doping concentrations of 10^{21} cm^{-3} in the poly-Si and $[B]_{waf,peak}$ of 10^{20} cm^{-3}. For all interface charge concentrations, the highest boron concentration provides the lowest ρ_c. This is due to the high concentration of holes at the Si/dielectric interface and in the poly-Si. At low charge concentrations, ρ_c varies by three orders of magnitude. At high negative charge, ρ_c of the different doping profiles converge. This is because the dielectric charge is causing an increased concentration of holes at the silicon surface, similar to the effect of boron doping. Finally, at a high positive charge, there is an increase in contact resistivity, as the holes are repelled from the interface. The effect is minimal for the most highly doped structure (10 to 20 mΩ·cm^2 at 5×10^{12} q/cm^2), but severe in the lightly doped structures. Thus, to achieve low resistivity contacts, high doping concentrations are essential for dielectrics with low or positive interface charge, while highly negatively charged dielectrics can achieve low resistivity contacts without the need for high doping concentrations.

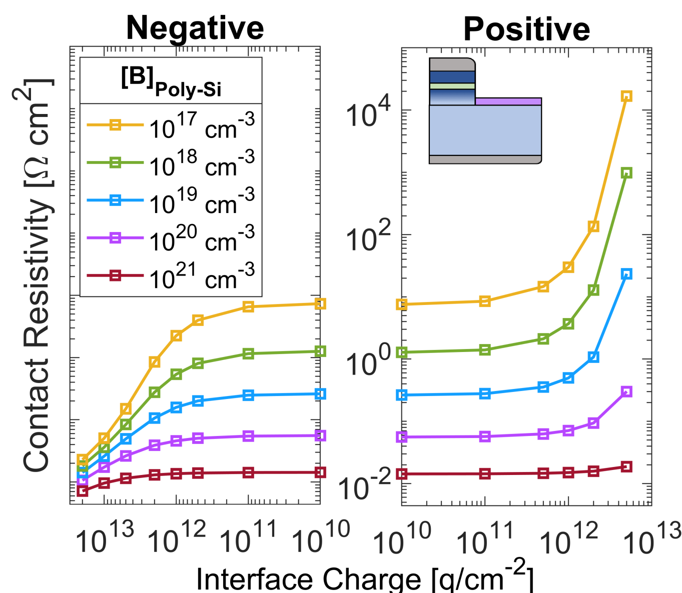


Figure 4.7: The resistivity of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for varying poly-Si doping concentration. Where $[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$.

4.4.3 Application to Realistic Structures

Having studied the effect of charge and boron doping, it is worth relating the results to the dielectrics being studied and their typical intrinsic charges. SiN_x was used as the dielectric in these simulations, though SiO_x and AlO_x would behave in a very similar fashion, except the t_{diel} required to produce a given resistivity would change. SiO_x and AlO_x would both require a thinner nanolayer to give the same resistivity as the 2 nm SiN_x.

In practice, the charge in SiO_x is very low ($<10^{11}$ q/cm^2) so the resistivity of the structure will follow the trends seen at neutral charge, with the thickness having the most significant influence on the contact resistivity and a high doping concentration is desired for low ρ_c. SiN_x typically has a positive charge between 1-2$\times10^{12}$ q/cm^2. This range coincides with the onset of the increase in ρ_c. A higher dopant concentration will minimise any detrimental increase in contact resistivity. On the other hand, AlO_x has a high negative charge of 2-10$\times10^{12}$ q/cm^2. The high negative charge means ρ_c has a significantly smaller dependence on the doping profile of the contact. There will still be a strong dependence on the dielectric thickness, but, provided a sufficiently thin layer can be formed, AlO_x nanolayers could form low resistivity contacts without the need for very high doping concentrations, such as in DPFC structures.

4.5 Effect of Interface Charge on Passivation Quality

The next section focuses on the Si/dielectric passivation quality. The dark saturation current is simulated using the method detailed in Section 4.2.2 to study the influence of the dielectric fixed charge on the passivation quality, with respect to the chemical passivation and doping profiles. The simulation structure is shown in 4.3(b) and the model parameters are found in Table 4.3.

4.5.1 Influence of Charge for Varying Levels of Chemical Passivation

The chemical passivation is dictated by the number of defects at the Si/dielectric interface with energy levels in the silicon band gap. A complete profile of the interface has D_{it} as a function of energy across the band gap, combined with capture cross sections detailing recombination efficiency at each defect energy. However, for the purposes of these simulations, a simpler model is used where the passivation quality of the interface is given by the electron capture velocity (S_{n0}). The hole capture velocity (S_{p0}) is set to $S_{n0}/10$. Figure 4.8 shows the effect of dielectric charge on the dark saturation current for various levels of chemical passivation in a poly-Si passivating contact structure.

At low charge, the passivation quality is influenced by the set values of S_{n0} and from the FEP generated by the boron doping profile. The electron capture velocity dictates the dark saturation current as electrons are minority carriers in the p-type contact. At high negative dielectric charge, J_0 is reduced due to the depletion of electrons at the interface. An interface with poor chemical passivation experiences a stronger reduction in J_0 with high negative charge. It is therefore possible for an interface with poor chemical passivation but high Q_f to provide a better overall passivation than an interface with relatively good chemical passivation but very little charge. Positive Q_f is detrimental to the contact. For the doping profile used, the effect is small for charges below 10^{12} q/cm^2.

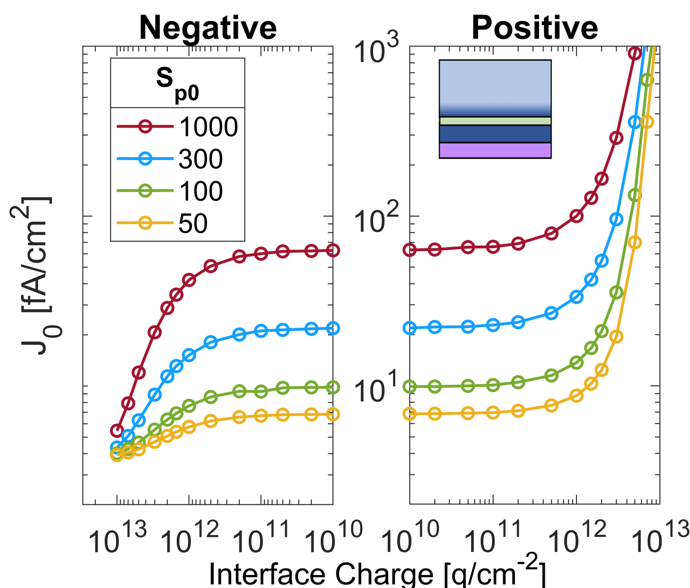
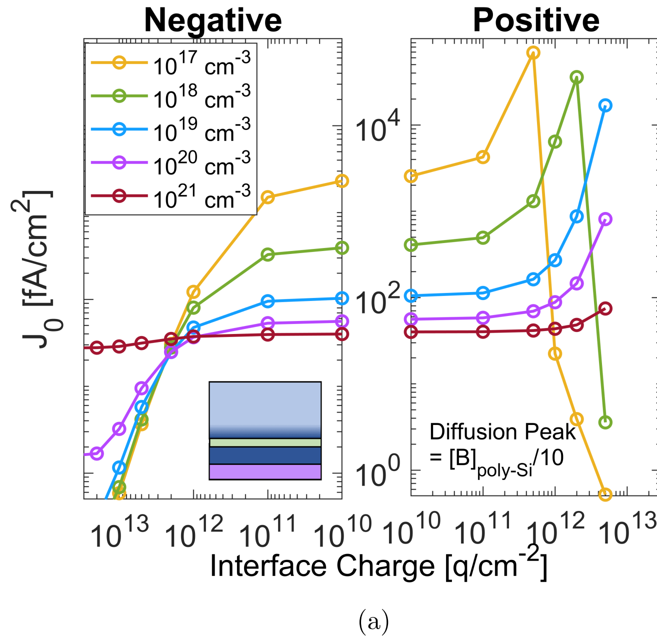


Figure 4.8: The effect of charge on J_0 for different levels of chemical passivation.

4.5.2 Influence of Charge for Different Doping Profiles

The high doping in the poly-Si layer, and the diffusion profile after firing adds FEP to the chemical passivation of the dielectric. As was discussed in Section 2.9, phosphorus and boron produce different doping profiles for SiO_x contacts. The SiO_x blocked phosphorus diffusion, causing a build-up of dopant at the oxide interface and a steep diffusion profile [158]. Boron on the other hand was not blocked, resulting in a significantly deeper diffusion. The FEP from the deeper diffusion is less effective. The Si/dielectric interface is also altered during the anneal, affecting the chemical passivation. This makes it difficult to experimentally determine the effects of the doping profile on the overall passivation of the sample. Simulations are used to isolate the contribution from the doping profile while S_{n0} and S_{p0} are kept constant at 3000 cm/s and 300 cm/s respectively. Figure 4.9 compares the dark saturation current simulated for the doping concentrations shown in Figure 4.4.

At low charge, the doping in the poly-Si is crucial to achieving a low J_0. High doping ensures the minority carrier concentration at the interface is low, reducing J_0. The interface charge has little effect on the dark saturation current of highly doped contacts. Conversely, lightly doped contacts show a significant reduction in J_0 with negative charge, resulting in a better passivation quality than the highly doped contacts at negative charges $>2\times10^{12}$. The negative charge repels the minority electrons from the interface, so the high doping is no longer necessary. The lower doping also reduces the Auger recombination which lowers the recombination in the contact structure. In a full cell, there is a trade-off as the lower doping in the poly-Si also reduces the lateral conduction to the metal contacts, increasing the sheet resistance. With increasing positive charge, the lightly doped contacts also show an initial increase in J_0, followed by a sharp decrease at high levels of positive charge. This indicates the silicon under the dielectric layer has reached inversion. Very low values of J_0 are achieved, but the high resistivity and the formation of a p-n junction prevent this low value of J_0 from being beneficial in the poly-Si cells fabricated here. Instead, it could be beneficial in an inversion layer cell [8].



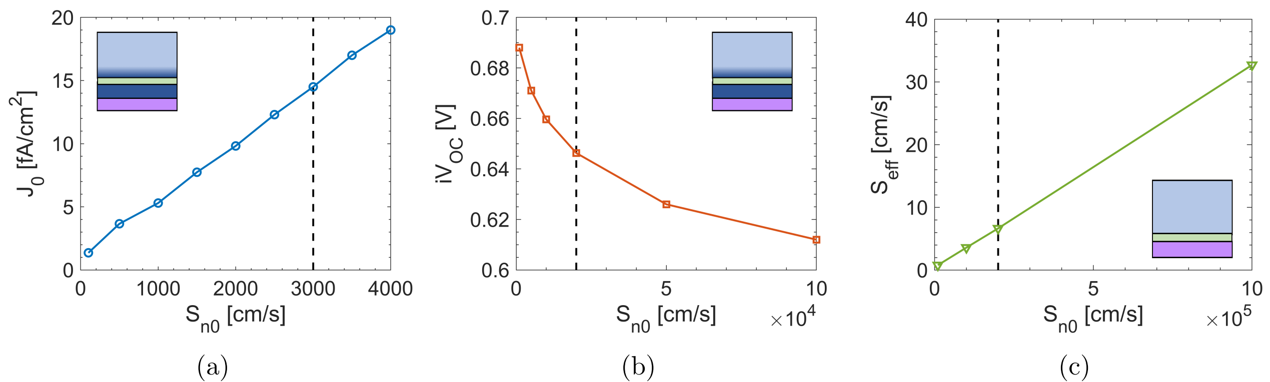
(a)

Figure 4.9: The J_0 of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for a) varying poly-Si doping concentration ($[B]_{waf,peak}$=$[B]_{poly-Si}$/10).

4.5.3 Realistic Contact Structures

In contacts fabricated with the different dielectrics studied, the chemical passivation of the interface will vary. Using values from the literature, the reported structures in [170], [176], [187] were simulated, including the dielectric charge and doping profiles. S_{n0} was varied (S_{p0} is again defined as $S_{n0}/10$.) and a plot of S_{n0} against J_0, iV_{OC} or τ_{eff} was used to obtain values of S_{n0} for SiO_x, SiN_x, and AlO_x. Figure 4.10 shows the plots used to determine values of S_{n0} for each dielectric. The exact value of S_{n0} is highly dependent on the deposition and processing conditions, so the values used here should only be taken as a general guide.

Once S_{n0} was determined from literature reports, J_0 is simulated for the poly-Si structure shown



(a) (b) (c)

Figure 4.10: S_{n0} calculated for a) SiO_x [187] SiN_x [170] and c) AlO_x [176] using values of τ_{eff} or J_0 from literature. Dash lines indicate the value of S_{n0} extracted.

in Figure 4.3(b) and the parameters in Table 4.3. Figure 4.11 shows J_0 as a function of interface charge. The typical intrinsic charge of each dielectric is indicated in the figure. The intrinsic charge in SiO_x is low and has no effect on the J_0, the positive charge in SiN_x has only a minor effect on the charge, and the high negative charge in the AlO_x provides a beneficial reduction in the J_0 of a real structure. When the intrinsic charge is considered, the AlO_x and SiN_x have similar passivation levels with a J_0 of ~100 fA/cm^2. The low S_{n0} of SiO_x means it currently provides the best passivation quality for poly-Si contacts. However, if the chemical passivation of AlO_x can be improved and combined with the high negative charge, there is scope for lower J_0. The simulations allow a simplified comparison between the dielectrics. In real fabricated structures, the diffusion rate of boron through the dielectric can vary, as well as the optimum post-deposition processing. These differences can significantly alter the doping profiles in the contacts and, as seen in Section 4.5.2, this can influence the passivation quality achieved.

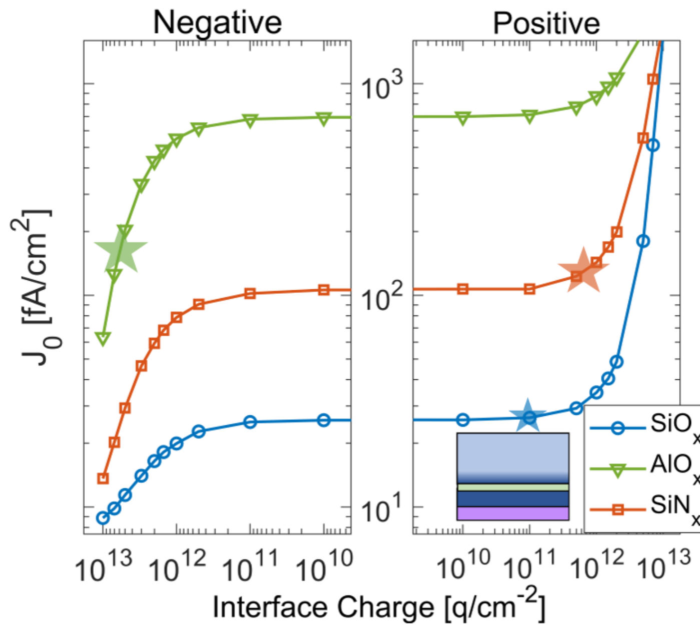


Figure 4.11: J_0 of SiO_x SiN_x and AlO_x poly-Si contacts as a function of dielectric charge. Values of S_{n0} obtained from Figure 4.10

4.6 Effect of Interface Charge on the Contact Selectivity

The results from previous sections can be combined to show the effect on the Selectivity of the contacts using Equation 4.2. Figure 4.12, combines the results from Figures 4.7 and 4.9 to give the Selectivity for doping profiles with a varying $[B]_{poly-Si}$ and $[B]_{waf,peak}$ (Figure 4.4). For neutral and positive interface charge, the higher doping levels provide a higher Selectivity due to the lower ρ_c and J_0. At high negative charge, the trend is reversed and the low dopant concentrations can provide higher Selectivity. This is due to ρ_c approaching the resistivity of the highly doped structures and the passivation quality exceeding that of the highly doped structures. The Selectivity of 13.5 for the highly doped poly-Si is lower than achieved for the best SiO_x/poly-Si contacts. The best contacts reached a Selectivity of 16, suggesting a lower thickness and improved chemical passivation compared to the values chosen here. Despite this, a high negative charge and optimised doping profile can achieve a Selectivity close to the best SiO_x contact. The Selectivity obtained from $[B]_{poly-Si} = 1\times10^{17}$ cm^{-3} shows erratic behaviour at high positive charge, this is due to the sharp drop in J_0 coinciding with a sharp rise in resistivity as an inversion region is formed in the silicon wafer.

If a contact has a high Selectivity due to a very low resistivity but only a moderate passivation quality, the highest efficiency is achieved by reducing the contact area fraction (Figure 2.9). Instead of a full-area contact, local contact fingers can be fabricated and a high-quality thick dielectric provides excellent surface passivation in the remaining area. The inverse case highlights a limitation of the Selectivity metric. If a contact has excellent passivation but a high resistivity, the area fraction cannot be increased above 100% so the fabricated cell would have a high series resistance, limiting the efficiency.

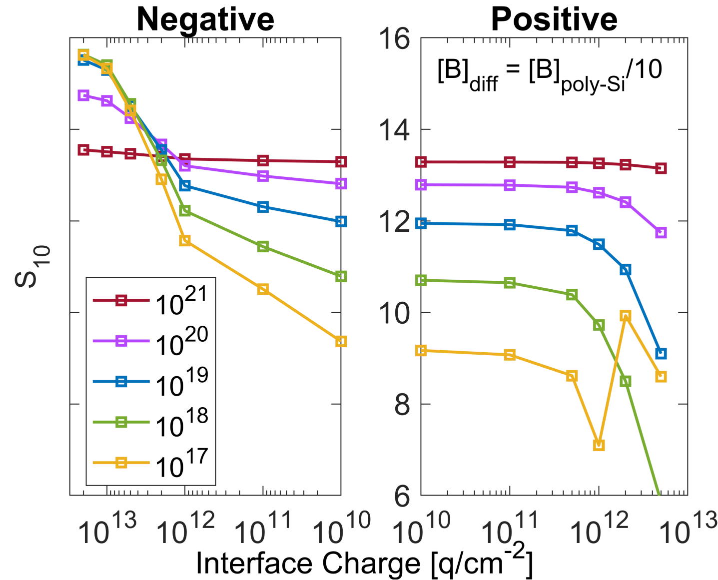


Figure 4.12: The Selectivity, S_{10} of a 2 nm SiN_x/poly-Si contact as a function of dielectric charge for varying poly-Si doping concentration ($[B]_{waf,peak}=[B]_{poly\text{-}Si}/10$)

4.7 Discussion

The combination of theoretical calculations and Sentaurus simulations in this chapter provide valuable analysis of the dielectric structures. The simulations enable a greater understanding of the dielectric/poly-Si interface and can be used to direct experimental work. For example, target thicknesses for each dielectric to produce contacts with resistivity below 100 mΩ·cm^2 were obtained as 1.2 nm, 1.5 nm, and 1.8 nm for SiO_x, AlO_x, and SiN_x, respectively. The highly flexible simulation set up in Sentaurus allows detailed analysis of complex structures, while the theoretical calculations are significantly quicker to carry out, so they can be used to provide fits for experimental measurements. The two methods were compared in Figure 4.5. The agreement for this structure gives confidence for the more complex analysis of charge and doping profiles carried out in Sections 4.4–4.6 and for the fitting of experimental measurements in Chapter 6.

The contact properties were simulated to understand the relative effects of the interface charge, doping profile and dielectric thickness on the contact resistivity. Then, the interface charge, doping profiles and chemical passivation quality were investigated for the contact passivation quality. The dielectric thickness is the most important parameter for ρ_c when the doping concentration is high in the poly-Si and at the Si/dielectric interface. At lower doping concentrations, t_{diel} is still important, but low resistivity contacts can also be achieved when the dielectric has a high negative fixed charge. The chemical passivation quality, defined by S_{n0} is key to fabricating a highly passivating contact. As was seen when studying real contact structures, S_{n0} can range by many orders of magnitude and a poorly passivated interface is unlikely to produce a low J_0, even with a high charge and optimised doping profiles. A surface with moderate chemical passivation can benefit greatly from a high charge, and optimised doping profile. The optimised doping conditions are highly dependent on the magnitude and polarity of charge at the Si/dielectric interface.

The resistivity calculations throughout this chapter have assumed that direct tunnelling is the only transport mechanism present in the dielectric. This limited the analysis of a TiO_x hole contact as the suspected transport mechanism involves trap states. Pinholes in the dielectric can also provide an alternative conduction mechanism through the dielectric. The mesh required to include conduction via pinholes is too complicated for finite element analysis, therefore Sentaurus is not an appropriate method to simulate pinhole transport. The contribution from pinholes can be included in the theoretical calculations and is used when fitting the experimental results in Chapter 6. For the J_0 simulations, previous work has shown that pinholes don't affect the passivation quality when kept below a critical density [139]. Therefore, the J_0 simulations in this chapter can be widely applied to a dielectric contact where the pinhole density is below 10^6 cm^{-2}.

SiN_x and AlO_x can form low resistivity contacts without the need for pinholes. This has additional implications for fabricating poly-Si contacts. If the transport requirements are fully met by the tunnelling current, then, the post-deposition anneal of the poly-Si can be tailored to achieve the optimum chemical passivaiton and doping profile. Fabricating a contact with a specific doping profile is extremely difficult and the doping profile may not follow the Gaussian distribution used in this work. Despite this, if the dominant conduction mechanism is tunnelling, the time and temperature of the anneal can be altered to optimise the passivation, without significantly affecting ρ_c. In the case of a SiO_x/poly-Si hole selective contact with pinhole-dominated conduction, the temperature profile must be optimised to generate the correct pinhole density and there is very little scope to alter the anneal parameters to optimise the doping concentration for passivation.

Additionally, it is suspected that the doping profiles generated with alternative dielectric layers may vary substantially from that of a SiO_x contact. This is investigated experimentally in Chapter 8.

The effect of charge and doping profiles have been simulated for hole-selective poly-Si contacts. The low doping concentrations mimic DFPC structures. A small modification to the contact is required for accurate ρ_c simulations (see Appendix C) but the overall trends are maintained. The simulations highlight the significant benefits of a high negative charge in both the ρ_c and J_0 of DFPC. The results from these simulations can also be transferred and applied to electron-selective contacts. In that case, a positive charge will be beneficial and a negative charge detrimental.

4.8 Summary

This chapter described theoretical calculations of tunnelling current through dielectric nanolayers based on the band structures of SiO_x, SiN_x, AlO_x, and TiO_x nanolayers. The tunnelling probability of holes and electrons as a function of dielectric thickness was obtained and highlights the benefit of a small VBO, such as with SiN_x, for a highly conductive hole contact. Sentaurus TCAD simulations and the theoretical calculations gave good agreement for the calculated resistivity. Sentaurus simulations were used to study the effect of dielectric interface charge and the doping profile on ρ_c and J_0 of a poly-Si contact. A negative charge is always beneficial, though the doping profile can influence the strength of this effect. The dependence on the doping profile is more complicated. High doping provides the best passivation and resistivity at low dielectric charge concentrations but at high negative charge, the J_0 is significantly improved with lower doping in the poly-Si.

Chapter 5

Fabrication and Physical Properties of Nanolayer Dielectrics

The material properties of the nanolayer dielectric films are studied for their application into passivating contact structures. The parameters of interest are the valence band offsets to Si, the composition of the nanolayers in comparison to bulk films, and the uniformity and thickness control for t_{diel} <2 nm. Methods for deposition and growth of SiO_x, SiN_x, and AlO_x are developed to enable controlled synthesis of the dielectrics. The deposition of dielectrics at specified thicknesses and with high uniformity is shown through ellipsometry measurements. XPS measurements determine the valence band offset between the dielectrics and a Si wafer, a key parameter for calculating the tunnelling current. XPS also gives a compositional analysis of the nanolayer and bulk films, adding insight on how the thin films differ from the thick layers. Chapter 3 details the experimental procedure for the deposition (Section 3.1), thickness measurements (Section 3.2) and XPS analysis of the films (Section 3.3). A summary of the techniques and analysis used in this chapter is given in Table 5.1.

Table 5.1: Summary of analysis techniques used in this chapter

Analysis	**Ellipsometry**	**XPS**
Dielectric Thickness	✓	✓
Nanolayer Stability	✓	✗
Stoichiometry	∼[a]	✓
VBO	✗	✓

[a]Some compositional information obtained from the refractive index

5.1 Nanolayer Growth and Thickness Determination

The simulations in Chapter 4 highlighted the sensitivity of the tunnelling current on the dielectric thickness. To make low-resistivity passivating contacts, it is vital to deposit the dielectrics to a controlled thickness and accurately measure the thickness of the fabricated layers. In this thesis, ellipsometry is the primary technique used to measure the thickness of fabricated nanolayers. Ellipsometry is a quick, non-destructive measurement, which enables the thickness of every fabricated sample to be measured. The models used for ellipsometry are discussed in Section 3.2. The XPS Thickogram method offers an additional means of determining thickness, as described in Section 3.3. There are potential sources of error with both of these techniques, which are discussed in more detail alongside the results.

5.1.1 Silicon Oxide

Silicon oxide is the standard nanolayer used in poly-Si contacts and can be fabricated using various techniques. Rapid thermal oxidation (Section 3.1.2), RCA2 chemical oxidation, and a UV-O_3 oxidation of silicon are used throughout this thesis. RTO is used due to the ability to control the SiO_x thickness. The growth rates were studied in detail in a Masters thesis [300]. The RCA2 oxide is used as an interlayer between the silicon and the SiN_x or AlO_x films due to its very thin nature. UV-O_3 SiO_x is fabricated by collaborators at EPFL to act as a control structure for the poly-Si structures in Chapter 8.

RTO SiO_x layers are grown on P1-5m, P10-20m and P1-10 Si substrates at 800 °C. Figure 5.1(a) shows the thickness measured by ellipsometry as a function of oxidation time. For oxidation times up to 60 s, high uniformity and consistent growth rates are measured. However, at longer oxidation times there is substantial inter- and intra-sample variation in the thickness. Overall, there is parabolic growth in the thickness with increasing time, as expected for the initial stages of dry oxidation [301]. It is noted that the SiO_x layers grown on the P1-5m Si substrate are consistently 0.1–0.2 nm thinner than those on the higher resistivity wafers. The samples for each oxidation time were processed together, thus, there is no difference in the processing of the P1-5m samples. As the thickness is lower for all oxidation times, it is unlikely that the difference in thickness is caused by a temperature variation in the RTO furnace. The high dopant concentration could affect the growth rate of the SiO_x or the boron-rich SiO_x could influence the fitting of the ellipsometry measurement [302]. Deal and Sklar [303] showed that a high boron concentration increases the oxidation rate, however, this is due to the kinetics of oxygen diffusion and the redistribution of impurities, which is important for thick oxides but is not limiting for such thin oxide layers.

The thickness uniformity of the SiO_x over a 4″ wafer was measured by taking a map of 25 measurements. The Filmsense FS-1 is not equipped with an automatic scanning stage, so the mapping is carried out manually. Figure 5.1(b) shows the oxide thickness measured for a 10 s RTO SiO_x layer. High uniformity is observed with variations $<$0.2 nm. The small variations are likely due to a non-uniform temperature in the chamber or the relative proximity of the silicon surface to the oxygen gas inlet. There is one area that shows a spike in thickness, the cause of this is unknown but may have been due to a small area of contamination.

The thickness of a 10 s RTO SiO_x layer was also determined from the XPS spectra using the Thickogram method. The thickness is evaluated using the Si $2p^{3/2}$ peak from the Si substrate and

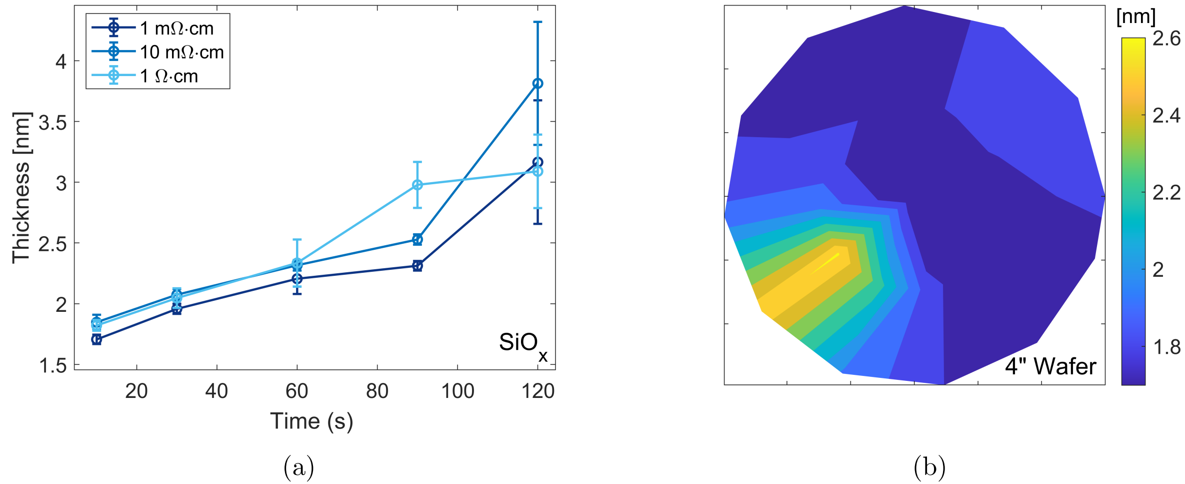


Figure 5.1: Ellipsometry thickness measurements of SiO_x a) as a function of oxidation time b) showing uniformity of a 10 s oxidation over a 4″ wafer after a 5 min 450 °C hotplate anneal.

either the bonded Si2p peak or the oxygen O1s peak from the SiO_x layer. This will give the same thickness, provided all the oxygen is from the SiO_x. The bonded Si2p peak gives a thickness of just 1.2 nm, while the O1s peak gives a thickness of 2.5 nm, suggesting there is an additional source of oxygen present in the sample. The additional oxygen is likely from some contamination on the film surface.

The RCA2 chemical oxide acts as an interlayer between the Si substrate and a SiN_x or AlO_x layer. The thickness of the RCA2 oxide on P1-10 is measured over a 2×2 cm sample. The thickness of 0.72±0.02 nm measured using ellipsometry is consistent with 0.6–0.9 nm measured by Köhler [118]. The RCA2 chemical oxide is substantially thinner than the RTO oxide layers grown since the chemical reaction at the silicon surface is self-limiting [118]. This is beneficial for use as an interlayer to ensure the overall thickness of the contact stack remains low, enabling a high probability of carrier transport across the dielectric stack and thus low resistivity. Thicknesses $<$1 nm are at the measurement limit of ellipsometry, so there could be a significant systematic error in the measured value of 0.7 nm.

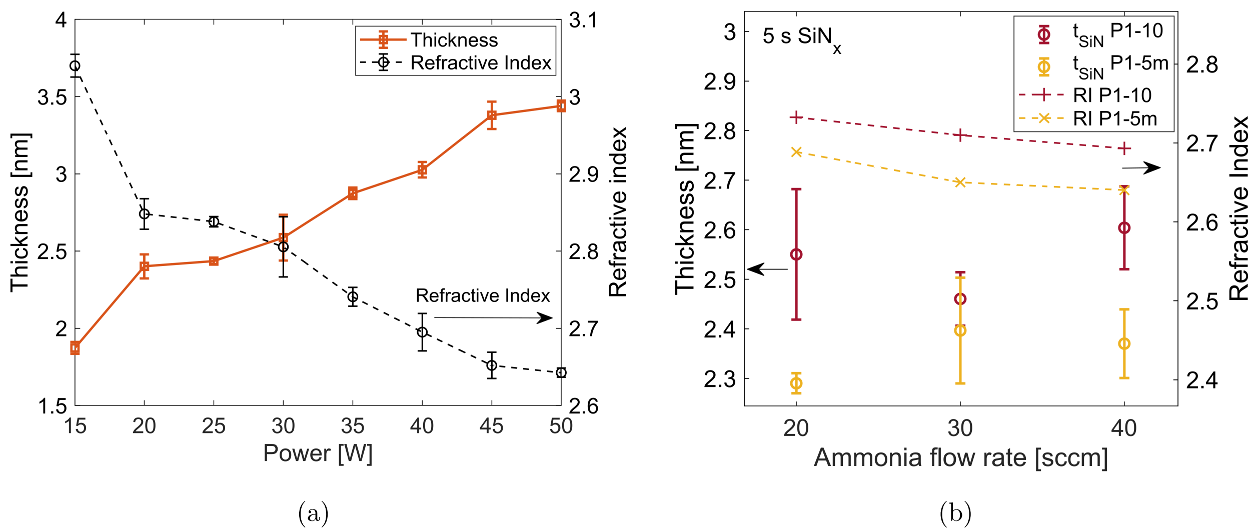
5.1.2 Silicon Nitride

SiN_x nanolayers are deposited using PECVD. Several parameters can vary the deposition rate and properties of the SiN_x nanolayer produced. Figure 5.2(a) shows the effect of the plasma power on the SiN_x deposition. The Cauchy model, described in Section 3.1.3, is used to fit the ellipsometry data to extract the thickness and refractive index (RI) of the SiN_x. As the power is increased, there is a reduction in the measured refractive index. This indicates that the films are becoming more stoichiometric. Si_3N_4 has a refractive index of 2.0 at 633 nm [304], so all manufactured SiN_x nanolayers are silicon-rich. There is also an apparent increase in the deposition rate as the power increases. To produce nanolayers with a controlled thickness a slow deposition rate is desirable so lower plasma power is favoured over a more stoichiometric film. From 20-50 W the deposition rate increase and the refractive index decrease are approximately linear. At 15 W there is a sharp

change in both the thickness and refractive index. This shows there is a minimum power required to initiate SiN_x deposition and at 15 W it is likely that there is no SiN_x deposited, the thickness measured is likely a thin oxide grown during the processing and transportation. 20 W provides the lowest deposition rate while ensuring a SiN_x nanolayer is formed. Therefore 20 W is used for all subsequent deposition of nanolayer SiN_x as the optimum power to enable the growth of thin, uniform SiN_x samples.

To achieve a more stoichiometric film while maintaining a low deposition rate the relative concentration of silane and ammonia is adjusted. To increase the concentration of N, the flow of ammonia is increased. Figure 5.2(b) shows the effect of increasing the ammonia flow rate on the thickness and RI of the SiN_x nanolayers. The nitrogen flow rate is reduced to keep the total flow rate constant. The increasing ammonia flow has no measurable effect on the thickness deposited. A slight decrease in the RI indicates the concentration of N increases, though the films are still far from being stoichiometric. This indicates it is difficult to achieve a stoichiometric thin film, which is likely related to the surface reactions in the initial stages of SiN_x PECVD deposition [82].

The deposition rate of SiN_x via PECVD with deposition parameters of 20 W plasma power and 20 sccm NH_3 is measured on P1-10, P10-20m and P1-5m wafers. Figure 5.3(a) shows the SiN_x thickness as a function of deposition time. The dashed lines are linear fits which give a growth rate of 0.25 nm/s. Extrapolating to 0 s gives an offset of 0.8 nm. The residual thickness is likely due to an unavoidable native SiO_x layer. The linear growth rates allow close control of SiN_x thickness. A 5 s deposition produces a 2 nm SiN_x layer. SiN_x deposited on the P1-10 wafer has a consistently lower t_{diel} by 0.2 nm, compared to SiN_x deposited on P1-5m or P10-50m wafers. The SiN_x growth rate is consistent across all samples. Therefore, the difference in thickness is likely due to a thinner interfacial oxide at the Si/SiN_x interface for the lower doped P-10 wafers [305]. Figure 5.3(b) shows the relationship between the refractive index and the thickness of the SiN_x nanolayers. There is a sharp decrease in RI between 2 and 3 nm. This indicates the SiN_x composition changes significantly



(a)

(b)

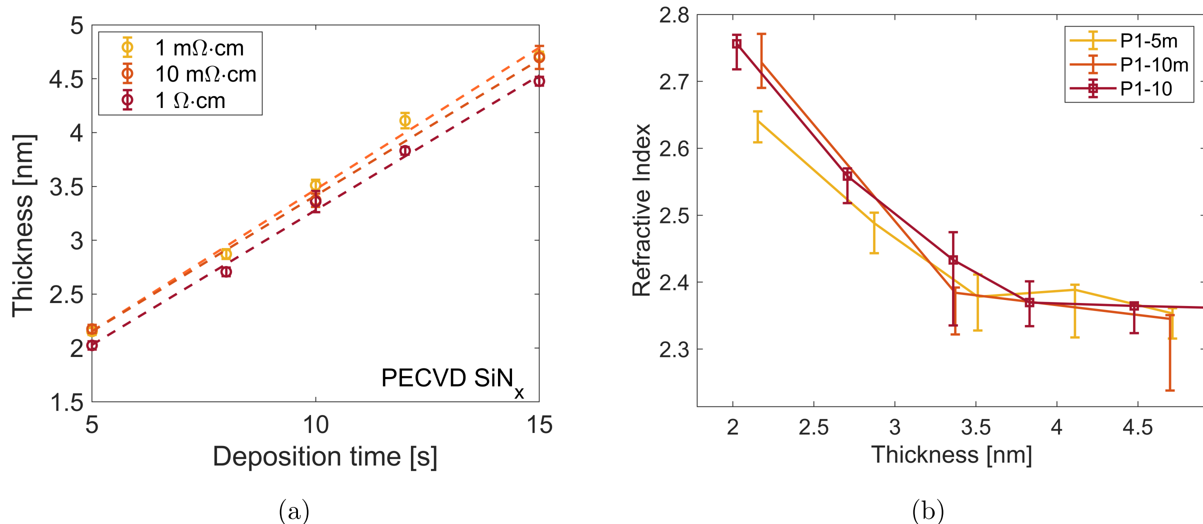
Figure 5.2: Ellipsometry measurements of thickness and RI for a) 5 s PECVD SiN_x on P1-10 silicon for increasing plasma power. The samples underwent a 450 °C post-deposition hot plate anneal and b) 5 s SiN_x with increasing ammonia flow rates using a PECVD power of 20 W. Lines are a guide to the eye.

in the first few nanometers of deposition. A 75 nm bulk SiN_x measured a RI of 1.9, which indicates a nearly stoichiometric SiN_x [306], [307]. Wan et al. [82] suggest that during the initial stages of deposition, first an a-Si:H layer forms, then the nitrogen infiltrates the a-Si layer, with the N-H bonds and Si-H bonds being replaced by Si-N bonds. This would explain the silicon-rich nature of the thin films.

Thickness determination from XPS measurements is used as a comparison to the values from ellipsometry. This is particularly important for SiN_x as the Cauchy model fits both t_{diel} and RI which can lead to inaccuracies in thin films. The XPS thickness is obtained from the N1s and bonded Si2p peaks. There is a close agreement in the values calculated from each core peak. Thicknesses of 2.4 and 2.5 nm were calculated from the N1s and bonded Si2p peaks respectively. The presence of oxygen in the SiN_x film may cause an underestimation of the thickness using the N1s peak but it is accounted for in the bonded Si2p peak. This explains the larger thickness calculated using the bonded Si2p peak. Ellipsometry measured a slightly thicker 2.8 nm, which could be due to a thin layer of carbon contamination. Nevertheless, the discrepancy of only 0.3 nm indicates good agreement.

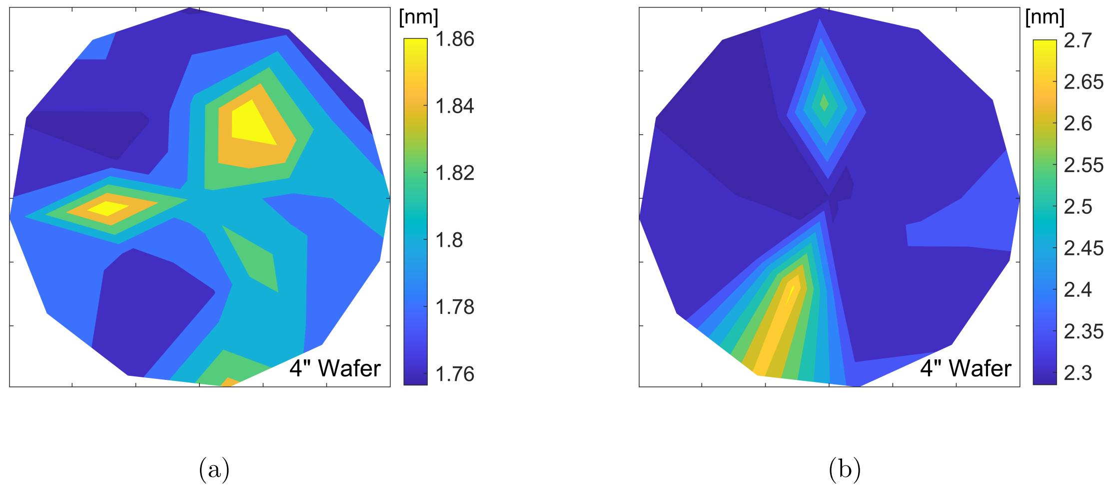
The thickness uniformity of the PECVD SiN_x on a 4″ wafer is shown in Figure 5.4(a). Excellent uniformity is seen across the wafer with <0.1 nm variation over the sample. PECVD is typically used to deposit significantly thicker layers in the range of 10–1000 nm for surface passivation and hydrogenation [52]. Lower uniformity is expected compared to the slower ALD process [308]. Here, it is shown that a high uniformity and controlled growth rate can be achieved, which is a promising result for the use of PECVD nanolayers in passivating contacts.

The thickness of an RCA2+3 s SiN_x stack is measured using ellipsometry and compared to the single layer 3 s SiN_x. The ellipsometry model used to fit the RCA2+SiN_x stack is the same as for the single-layer SiN_x. Reliable results could not be obtained for a two-layer model. This is due to the two-layer model assuming n and k values of a bulk SiO_2 and a sharp interface between the SiO_x and SiN_x layers, which is unlikely to be the case. Figure 5.4(b) shows a map of SiN_x thickness for a



(a) (b)

Figure 5.3: Ellipsometry measurements a) of SiN_x thickness for increasing deposition time as-deposited and b) comparing the RI to the SiN_x thickness.



(a) (b)

Figure 5.4: Ellipsometry thickness measurements showing uniformity over a 4″ P1-10 wafer for a) 3 s SiN_x and b) of RCA+3 s SiN_x, after a 5 min 400 °C anneal.

3 s PECVD SiN_x with an RCA2 oxide interlayer across a 4" wafer. The uniformity is better than ±0.1 nm, aside from a small area which measured a 0.4 nm increase in thickness. This may be due to contamination during processing. Compared to the 3 s PECVD SiN_x deposited immediately after an HF dip (Figure 5.4(a)), there is a 0.5 nm increase in the measured thickness. The RCA2 oxide alone measured 0.7 nm. The smaller increase of 0.5 nm suggests either the ellipsometry value for the RCA2 layer is too high, or there is an unintentional SiO_x layer present in the SiN_x single layers. The refractive index measured for the RCA2+SiN_x stack is 2.9, identical to a 3 s SiN_x single layer.

The XPS Thickogram method is also used to measure the thickness of the RCA+SiN_x stack. The thickness is calculated using the bonded Si2p peak and an attenuation length for the SiO_xN_y stack. The attenuation length was calculated to be 2.9 and a thickness of 0.8 nm was measured. The oxygen and nitrogen peaks can be used to calculate the thickness of SiO_x and SiN_x separately. The SiO_x and SiN_x thicknesses are found to be 1.4 and 0.1 respectively. The sum of these values gives an approximation of the total stack height of 1.5 nm. The nitrogen signal is very low, suggesting the film formed during the 3 s PECVD deposition is a silicon and oxygen-rich SiO_xN_y. The composition of the SiN_x layers is discussed further in Section 5.3. The SiO_x thickness is likely overestimated due to a contribution from oxygen contamination.

5.1.3 Aluminium Oxide

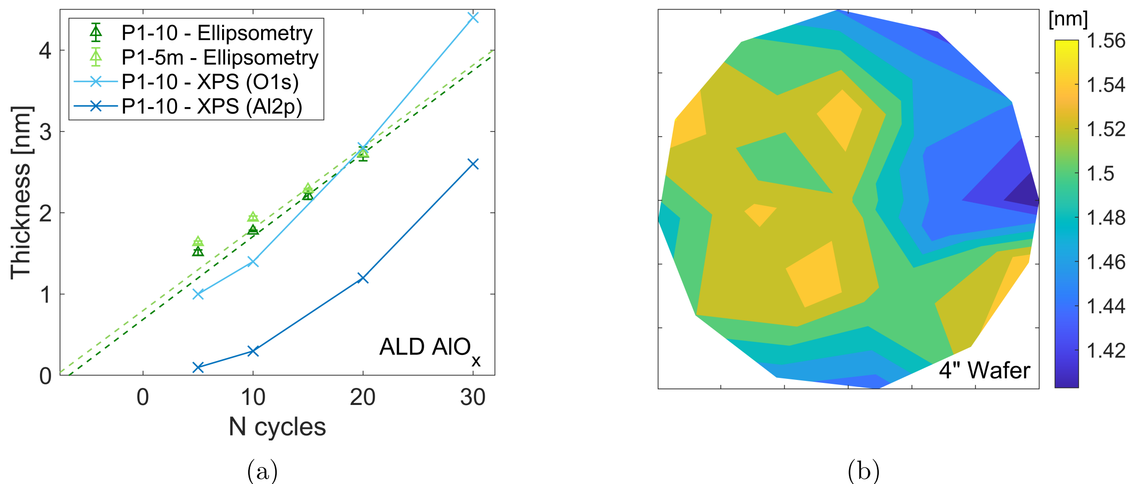
Thermal ALD is used to deposit the AlO_x nanolayers, with the deposition parameters given in Table 3.3. Figure 5.5(a) compares the measured thickness from ellipsometry and XPS for an increasing number of deposition cycles. Both measurement techniques show evidence of island growth in the initial stages of deposition, indicated by the small thickness increase between 5 and 10 deposition cycles. This is expected from ALD of AlO_x on H-terminated silicon [309]. The growth per cycle (gpc) is obtained using linear fitting of the ellipsometry data. A thicker layer of 50 cycles is also measured and used in the fitting, while the 5 cycles AlO_x is excluded due to the island growth.

The growth rate was calculated as 0.10 nm/cycle.

For XPS, thicknesses are calculated using the Al2p and O1s peaks. The Al peaks are known to be solely due to the AlO_x nanolayer, while the O1s peak will have contributions from a SiO_x interlayer. The thicknesses obtained from the Al2p and O1s peaks are shown in Figure 5.5(a). The Al peaks give a lower thickness than the ellipsometer values, particularly at low thicknesses, where there is a very small signal from the Al. The O1s peak provides a relatively close agreement to the ellipsometry values. The offset between the Al2p and O1s peaks is consistent at ∼1 nm and this gives an approximation of the SiO_x interfacial layer thickness.

The AlO_x uniformity across a 4″ wafer is measured using ellipsometry and shown in Figure 5.5(b). The thickness variation is just over 0.1 nm. The contour map shows the non-uniformity is due to a larger thickness on one side of the wafer. This could be explained by the position of the wafer relative to the gas inlet in the ALD chamber. Optimisation of the pulse and purge time of the precursor gases could minimise this variation, yet the uniformity is already sufficient so optimisation was not carried out. The high level of uniformity is expected for ALD and confirms that a highly controllable AlO_x nanolayer can be grown [310].

The thickness of an RCA2/5 cycles AlO_x stack is also measured through ellipsometry and XPS. For ellipsometry, a single layer AlO_x model is used. As with the RCA2/SiN_x, a two-layer model did not provide a reliable fit. The thickness is measured as 1.85±0.01 nm over a 2×2 cm sample. A control sample was processed in the ALD at the same time, with the deposition occurring immediately after an HF dip. This sample measured a thickness of 1.25 nm, indicating a 0.6 nm thickness increase due to the RCA2 oxide. The XPS analysis of the RCA+AlO_x stack measured a thickness of 0.6 and 1.8 nm for the Al2p and O1s peak respectively. As with the AlO_x single layers, the O1s peak shows good agreement with the ellipsometry value.



(a) (b)

Figure 5.5: Thickness measurements of AlO_x a) Measured using ellipsometry and XPS for increasing number of deposition cycles b) Ellipsometry measurements showing thickness uniformity of 5 cycles thermal ALD over a 4″ wafer after a 5 min 400 °C anneal.

5.1.4 Titanium Oxide

The TiO_x samples are deposited using thermal (tALD) and plasma (pALD) ALD by collaborators at AIST. The deposition parameters are detailed in Table 3.3. Figure 5.6 shows the uniformity of the thermal TiO_x layer over a 4×4 cm sample. The uniformity is high, as expected with ALD deposition. A TiO_x thickness of 5 nm, with a SiO_x interlayer of ∼1.5 nm is measured via TEM at AIST [3]. A larger thickness of nearly 7 nm is measured here. The SiO_x layer will result in an increase in the thickness measured via ellipsometry and the sample was measured after ∼10 months in lab conditions, so an additional increase may be due to further oxidation, moisture absorption, or a layer of contamination.

The thickness for one pALD and one tALD sample was measured by XPS using the Ti2p and O1s peaks. A thickness of 4 nm and 4.1 nm was obtained from the Ti2p peak for thermal and plasma ALD, respectively. A high level of carbon contamination (>20%) is seen in the TiO_x samples. An oxygen contribution from organic contaminants is indicated by a signal at 531–533 eV in the O1s core level. A peak is fitted at 531.5 eV in the O1s spectra and is removed from the oxygen signal for the TiO_x thickness determination. The O1s peak fitting for TiO_x is shown in Appendix F. The thickness determined from the O1s peak is slightly larger than from the Ti2p, measured at 5.3 and 5.7 nm for thermal and plasma ALD, respectively. The increase in thickness results from the SiO_x interfacial layer. XPS measurements remove the effect of contamination and enable the contributions from SiO_x and TiO_x to be distinguished. The results show a good agreement with the quoted thickness from AIST. The electrical measurements in Chapter 7 were carried out immediately after the samples were received, so there should not suffer from this contamination.

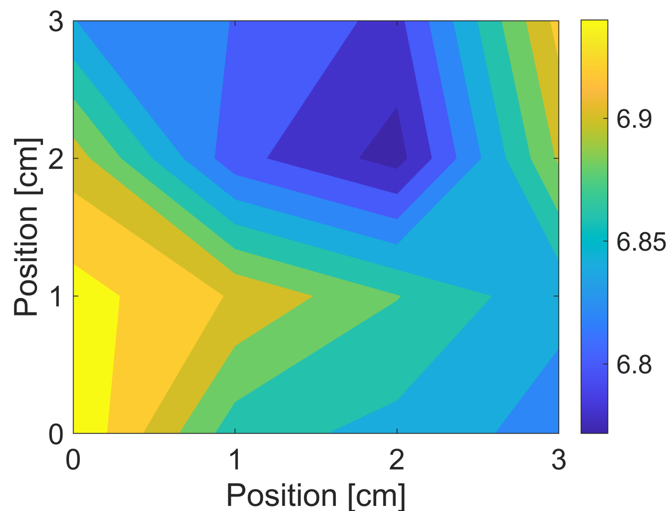


Figure 5.6: Uniformity measurements of the TiO_x over 4 cm sample.

5.2 Nanolayer Stability

When measuring the fabricated nanolayers, it was noted that the thickness increased after storage in lab conditions. It was hypothesised that this could be due to (additional) oxidation of the films during storage or absorption of moisture. To study this effect, the films were deposited and then transported to the ellipsometer under a desiccated N_2/vacuum atmosphere. The sample thickness was measured, and then the samples were left in lab conditions overnight. The next day the samples were re-measured before being annealed on a hotplate at increasing temperatures. Figure 5.7 shows the variation in the measured thickness for SiO_x, SiN_x and AlO_x. All dielectric nanolayers measure a thickness increase of ∼0.3 nm overnight. The thickness is reduced to the as-deposited value at the optimum T_{ann} for each dielectric. Figure 5.7(a) shows the change in thickness for the RTO SiO_x. As the SiO_x is grown at a temperature of 800 °C, the low-temperature anneals used here are unlikely to change the film structurally. The increase in thickness overnight and subsequent decrease with annealing is likely to be caused by the absorption of moisture. The SiO_x thickness decreases with increasing T_{ann}. Either the higher temperatures promote further desorption of moisture, or further time at elevated temperatures is required to remove the moisture fully. The evolution of the SiN_x thickness is shown in Figure 5.7(b). The SiN_x sample undergoes an initial anneal immediately after deposition before being left overnight. This shows a slight decrease in the thickness, which could be due to a densification of the film, possibly through the release of hydrogen [311]. As with SiO_x, the increase and decrease of thickness overnight and after annealing are also likely to be caused by moisture adsorption. The thickness remains constant with increasing T_{ann}, suggesting a lower activation energy to remove the moisture compared to the SiO_x. For AlO_x, the same increase overnight and decrease with annealing at 300 °C is seen in Figure 5.7(c). However, at T_{ann} >300 °C an increase in the thickness is seen. The increase could be due to additional oxidation, forming a thicker SiO_x interfacial layer between the Si and AlO_x.

The properties of all films are seen to change in the hours after deposition. It is speculated that the increase is associated with moisture absorption into the films. To minimise the effect of the degradation, the samples are stored in a desiccated N_2/vacuum atmosphere, any additional layers are deposited as soon as possible after deposition and measurements are carried out promptly. The final contact structure will have capping layers such as poly-Si or metal. These layers protect the thin films from the environment so this degradation will not pose a problem for the films' practical use.

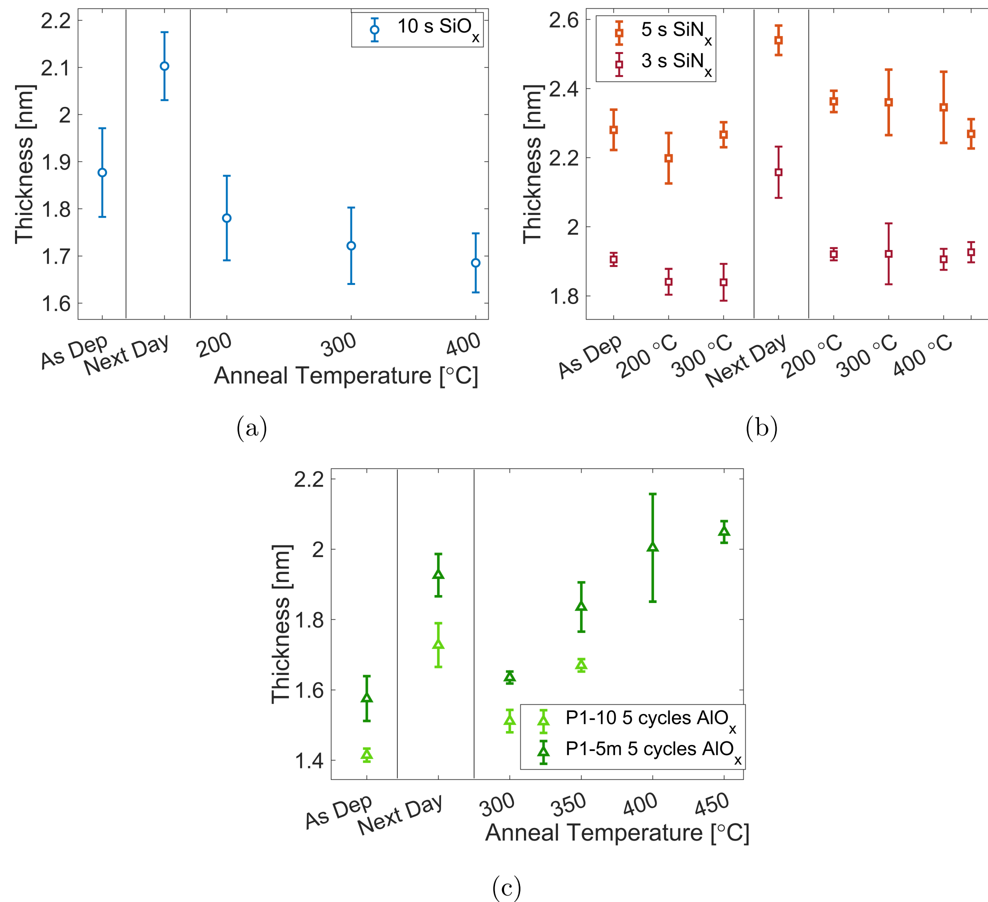


Figure 5.7: Evolution of dielectric film thickness overnight and after hotplate anneals. a) SiO_x b) SiN_x and c) AlO_x.

5.3 Stoichiometry

The RI extracted from ellipsometry measurements provided some qualitative information on the stoichiometry of the SiN_x films. The RI measurements indicate that the nanolayer dielectrics can have very different properties to thick layers, >10 nm. XPS provides a quantitative compositional analysis of the nanolayer and bulk dielectrics. The chemical differences between the thin films and bulk dielectrics can provide valuable information to understand the films better. The stoichiometry can be used to explain the trends seen in other material properties, such as the VBO (Section 5.4) and the passivation quality (Chapter 7). This understanding is critical to fabricating effective passivating contact structures.

As XPS is an extremely surface sensitive technique, contamination on the surface can influence the measurements. It is possible to remove the contamination by in-situ ion sputtering. This etches the sample, leaving a pristine surface. The PhiV XPS was used to etch the surface of bulk SiN_x, AlO_x and a Si wafer. By removing the surface contamination of the thick films it can be ascertained if the surface contamination is influencing the measurements. The thin dielectrics could not undergo sputtering to remove surface contaminants as it would alter the film thickness and very likely remove the film entirely. The sputtered bulk samples are therefore used as a reference for the influence of the surface contamination.

The composition of a bare Si substrate is checked for reference. It should be almost entirely Si, with only a small concentration of oxygen due to a native oxide and carbon due to surface contamination. P1-5m and P1-10 silicon is measured in the TSK XPS. Significant oxygen and carbon peaks are observed corresponding to 7–8 at%. There is no bonded Si2p peak detected indicating that the Si surface was H-terminated and no native oxide formed during sample transportation. The PhiV XPS measurement of a P1-10 wafer has a larger oxygen concentration of 10 at% and a small bonded Si2p peak indicating a thin native oxide layer. Ion milling is used to etch the surface of a P1-10 wafer. After milling there are no longer oxygen or carbon peaks and the bonded Si peak is removed, confirming these peaks are purely due to surface layers.

The thermally grown SiO_x films are expected to be close to stoichiometric SiO_2. The TSK XPS is used to measure the bulk and thin SiO_x layers. Figure 5.8 compares the fabricated films to the stoichiometric Si:O ratio. The 100 nm thermal oxide is silicon-rich which is unexpected as it would normally be stoichiometric. The 10 nm is also slightly silicon-rich while the thin SiO_x are oxygen rich. The oxygen-rich thin layers are also unexpected as typically the thin films have lower valence Si (i.e. $Si^{1,2,3+}$) [119], [128], [130] and therefore incomplete oxidation. If the oxygen concentration found in the bare silicon sample is assumed to be due to contamination at the surface, it can be removed from the measured oxygen concentration to give a true oxygen concentration in the SiO_x film. When this analysis is carried out, the stoichiometry of the thin films matches closely to the bulk SiO_x.

The stoichiometry of the SiN_x films can vary significantly depending on the processing parameters. The ellipsometry measurements showed that the refractive index changes significantly in the first few nanometers of growth, indicating changes in the stoichiometric of the nanolayer films. Figure 5.9(a) shows the Si, N and O concentrations in the bulk and thin SiN_x films with and without a hotplate anneal. In all cases, the samples that underwent a hotplate anneal show an increased oxygen concentration. In the PhiV XPS, an annealed bulk sample is sputtered to remove the contribution of surface layers. The sputtered bulk sample shows a significant reduction in the

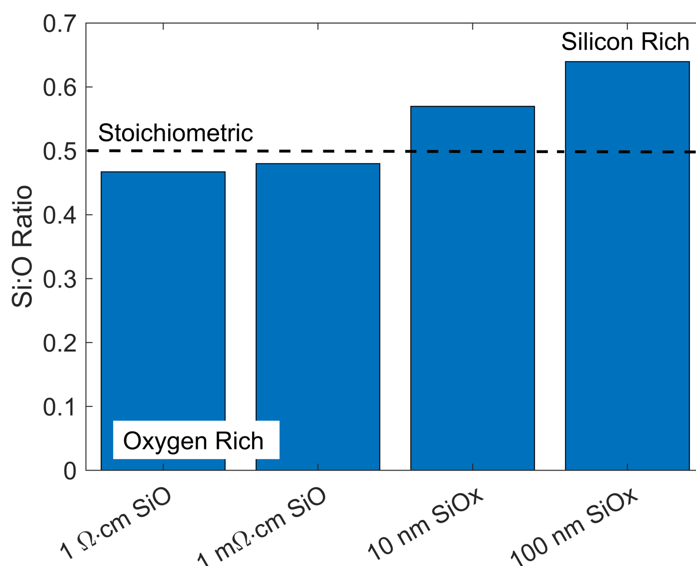
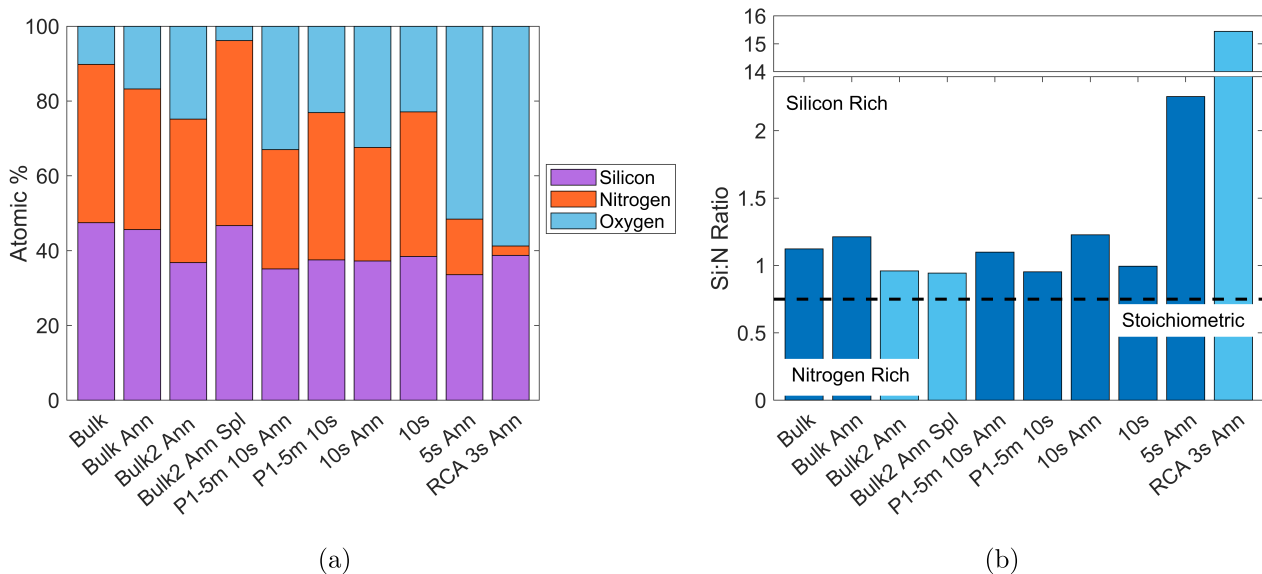


Figure 5.8: Si:O ratio for bulk and thin SiO_x films

oxygen concentration, indicating that a proportion of the oxygen detected is surface contamination or within the first few nanometers of the surface of the films. The oxygen peak is not completely removed through sputtering, with an oxygen concentration of ~4% in the bulk of the film. The oxygen concentration is significantly higher in the thin samples, which indicates the presence of a SiO_x interfacial layer, or the formation of an SiO_xN_y layer in the initial deposition stages. The thinner SiN_x layers, formed with 5 and 3 s depositions, show a significant reduction in the proportion of nitrogen in the films. The concentration of bonded Si remains roughly constant so the increase in oxygen is not due to an increase in the contribution from surface contamination.

Figure 5.9(b) plots the Si:N ratio of the layers measured in the TSK (dark blue) and PhiV (light blue) systems. The dashed line indicates the Si:N ratio of stoichiometric Si_3N_4. The bulk SiN_x is silicon-rich with the Si:N ratio close to 1, this fits with the refractive index of 1.9 determined from ellipsometry [307]. When the SiN_x sample is sputtered there is no change in the Si:N ratio. This shows that surface contamination does not change the relative intensity of the Si and N peaks, so the Si:N ratio is representative of the dielectric films. The Si:N ratio for the 10 s SiN_x is also close to 1, indicating that the stoichiometry of the SiN_x film is close to the bulk. The Si:N ratio increases significantly to 2.5 when the deposition time is reduced to 5 s. The RI of 2.7 from ellipsometry gives good agreement with literature [306], [307]. The RCA2/3 s SiN_x stack has an extremely high Si:N ratio. The RCA2 oxide will partly contribute to this increase, however, the reduction in N concentration is more severe than expected. The low concentration of N indicates that the initial nucleation of PECVD SiN_x is Si-rich, and in the short deposition time there is not sufficient film growth to form stoichiometric SiN_x [82]. Significant alteration of the PECVD deposition conditions could enable a more stoichiometric SiN_x to form and is an avenue for further work.

The deposition conditions of the ALD AlO_x can also have a significant influence on the stoichiometry of the deposited films. The Al:O ratios of the thin layers are shown in Figure 5.10.



(a) (b)

Figure 5.9: a) Atomic concentrations of silicon, nitrogen and oxygen and b) Si:N ratio in SiN_x bulk and thin films. Ann denotes the hotplate anneal and Spl the sputtered bulk. In b) dark blue plots indicate measurements taken with the TSK XPS and light blue bars represent PhiV XPS data.

The untreated bulk sample from the PhiV is slightly oxygen-rich, compared to the measurement in the TSK, this is likely due to higher levels of contamination. When this is removed via sputtering the composition measured in the PhiV gives close agreement with the TSK. The thin AlO_x becomes increasingly oxygen-rich as the number of cycles is reduced. Oxygen contamination on the surface will have a larger influence as the film thickness is reduced, contributing to the high oxygen concentration seen in these films. However, Al-depletion is also common in the initial ALD AlO_x cycles [312] and it is not possible to separate the contribution from each of these effects.

The RCA/AlO_x stack has an Al:O ratio of 0.2. Interestingly, this is a higher Al concentration, compared to 5 or 10 cycles deposited after HF dip. This is due to differences in the surface chemistry of the silicon substrate in the initial stages of deposition. The single-layer stacks have a hydrogen-terminated Si surface after the HF dip, which prevents Al adsorption in the initial stages of growth [312]. The oxygen-terminated substrate after RCA2 oxide growth could enhance Al adsorption, forming a more stoichiometric AlO_x layer and accelerating growth in the initial ALD cycles. For the thin films grown here, the initial nucleation of AlO_x is crucial to the final properties of the film.

The compositions of tALD and pALD TiO_x are compared using XPS analysis. The oxygen associated with the carbon contamination was removed following the methodology described in Section 5.1.4. The SiO_x interlayer was assumed to be stoichiometric and the oxygen associated with this is also removed to determine the oxygen concentration in the TiO_x. The tALD gave a stoichiometry of $TiO_{1.8}$, while the pALD gave $TiO_{1.7}$. The layers are slightly Ti-rich, with the pALD having a larger oxygen deficiency. Previous energy-dispersive X-ray spectroscopy measurements performed at AIST, found the stoichiometry of both pALD and tALD to be close to TiO_2 [194].

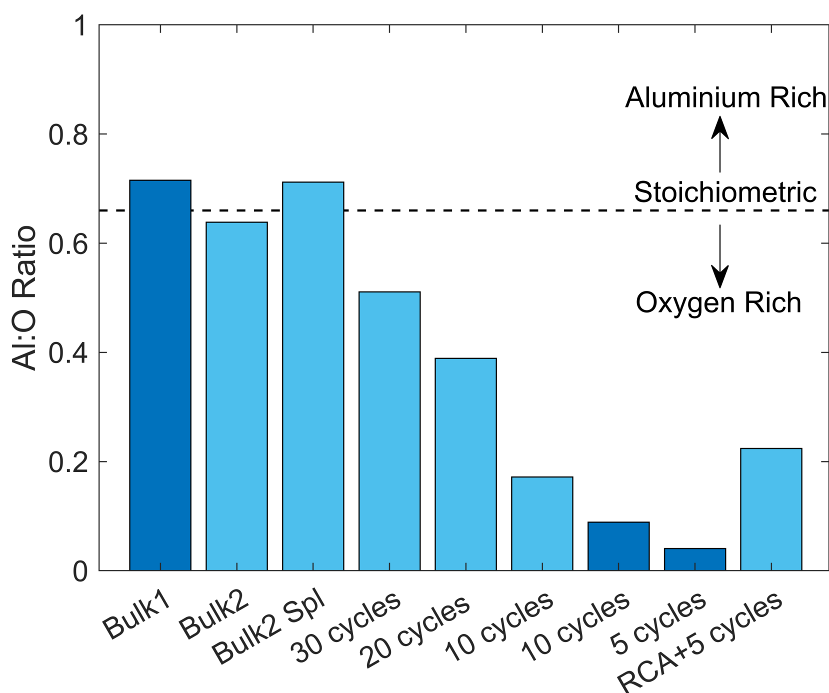


Figure 5.10: Al:O ratio for bulk and thin AlO_x films. Dark blue indicates measurements taken with the TSK XPS and light blue represent the PhiV XPS data. Spl refers to the sputtered Bulk

The TiO_x peak measurements are shown in Appendix F. A noteable difference is seen in the size of the SiO_x interlayer peak for the plasma and thermal TiO_x layers. The thermal ALD has a smaller SiO_x peak indicating a thinner interfacial layer. This fits with the energy-dispersive X-ray spectroscopy measurements [194].

5.4 Valence Band Offsets

The Krauts method described in Section 3.3 is used to measure the valence band offset between silicon and the dielectrics studied in this work. The VBO can be calculated using any core peak present in the dielectric films. This allows two values of VBO to be calculated for each sample. The value of VBO obtained from the different peaks should be consistent; if this is not the case, the reasons are discussed. The VBO is also calculated for various different processing conditions. The influence of the Si substrate, dielectric thickness and post-processing on the VBO are all investigated. The VBO was always determined using bulk and interlayer measurements from the same XPS to ensure consistency between measurements. Example peak fits and VB onset determination for each dielectric are shown in this chapter, along with a summary table of the calculated VBO. The full set of XPS results can be found in Appendix F.

5.4.1 Influence of Sputtering

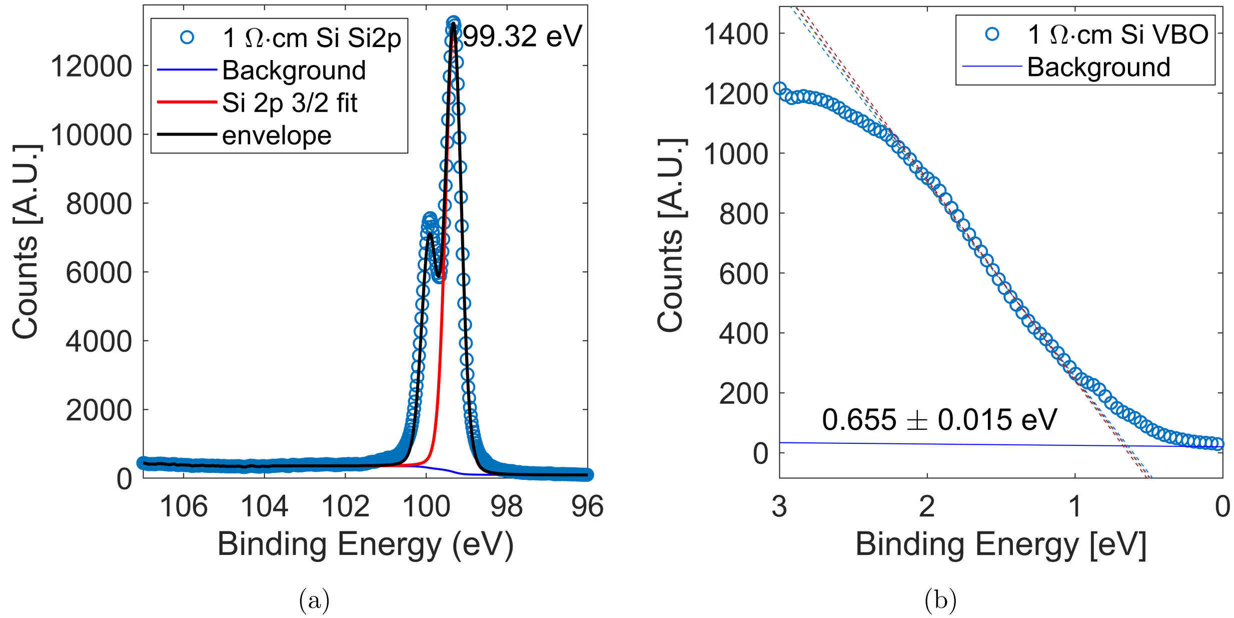
Using the PhiV XPS, the bulk samples were sputtered to remove the surface contamination. The separation between the VB onset and the core peaks was compared before and after sputtering. The bulk AlO_x showed no change in the energy separation of the VB to the Al2p or O1s peak. The separation in the Si increased by 0.5 eV and the separation in the SiN_x increased by 0.5 in the N1s peak and 0.2 in the bonded Si peak. The cause of the change in energy separation is not known, but it could have a significant impact on the VBO determined. It is not possible to sputter the interlayer samples as this would completely remove the thin dielectric. Thus, to ensure consistency, it is best to use the values for the un-sputtered bulk.

5.4.2 Bare Silicon

The Si2p core level and valence band onset for bare silicon are required for all VBO calculations. Figure 5.11(a) shows the Si 2p peak fitting for the bare P1-10 Si wafer. The red line shows the fit for the Si $2p^{3/2}$ peak, while the black line shows the total fit, including the Si $2p^{1/2}$ peak. Figure 5.11(b) shows the valence band onset for the bare Si sample. The energy range considered for the linear extrapolation of the leading edge is varied to find the error in the valence band onset. The same analysis to determine the valence band onset is applied to the bulk dielectric films in later sections. A P1-5m wafer was measured for comparison and the results are shown in Appendix F.

5.4.3 Silicon Oxide

Silicon oxide has been studied extensively so the VBO to silicon is well understood. The RTO SiO_x sample is used as a control to validate the experimental procedure. The core levels and valence band onset required for VBO determination are shown in Figure 5.12 for SiO_x on P1-10 Si. The thick



(a) (b)

Figure 5.11: TSK XPS of bare P1-10 silicon wafer a) valence band onset b) Si 2p peak with fitting.

oxide sample was fabricated using RTO. The capabilities of the RTO furnace limit the thickness to 10 nm, which is not thick enough to completely prevent the signal from the underlying silicon wafer. The signal from the wafer is seen as the small elemental silicon peak at 99 eV in Figure 5.12(a) and the small increase in signal near 0 eV in Figure 5.12(e). The contribution to the signal is minor so it should not influence the silicon oxide peak at 103 eV or the determination of the SiO_x VB onset. A 30 s RTO SiO_x is used for the interface sample. It is expected to be 2-3 nm thick. Figure 5.12(c) shows the clear signals from the Si substrate at 99 eV and the SiO_x layer at 103 eV, indicating that a suitable SiO_x layer thickness was used. A 10 s RTO SiO_x, a 30 s RTO SiO_x layer grown on P1-5m Si, and a bulk 100 nm thermal oxide are all measured for comparison. Either the bonded silicon or the O1s core peak can be used for VBO determination. From the measured samples there are several possible options for determining the VBO of the SiO_x layer. The comparison of VBOs calculated is used to check the consistency of the measured band offset. Table 5.2 shows the calculated VBO measurements and compares the VBO for the different Si wafer doping, bulk SiO_x and SiO_x core peaks used.

An average VBO of 4.4±0.2 eV is calculated. This shows good agreement with the values reported in literature (Table 4.1). The XPS core peak gives no significant difference in the VBO calculated across the samples. This shows that samples behave consistently across all binding energies and validates the assumption that any band bending at the surface affects all core levels equally. The choice of bulk SiO_x shows a small difference of 0.1 eV. The standard deviation is larger than this variation. However, close inspection of the bulk SiO_x results shows a systematic difference in the results for VBO calculated with the 100 nm bulk and the 10 nm bulk SiO_x. When all other conditions are the same, the calculations using the 100 nm bulk SiO_x are consistently ∼0.1 eV smaller than the equivalent calculation using the 10 nm bulk. The cause of this is predicted to be due to the difference in the stoichiometry of the two bulk films rather than due to the small signal from the underlying Si wafer seen in the 10 nm bulk sample. The VBO increases by 0.4 eV for

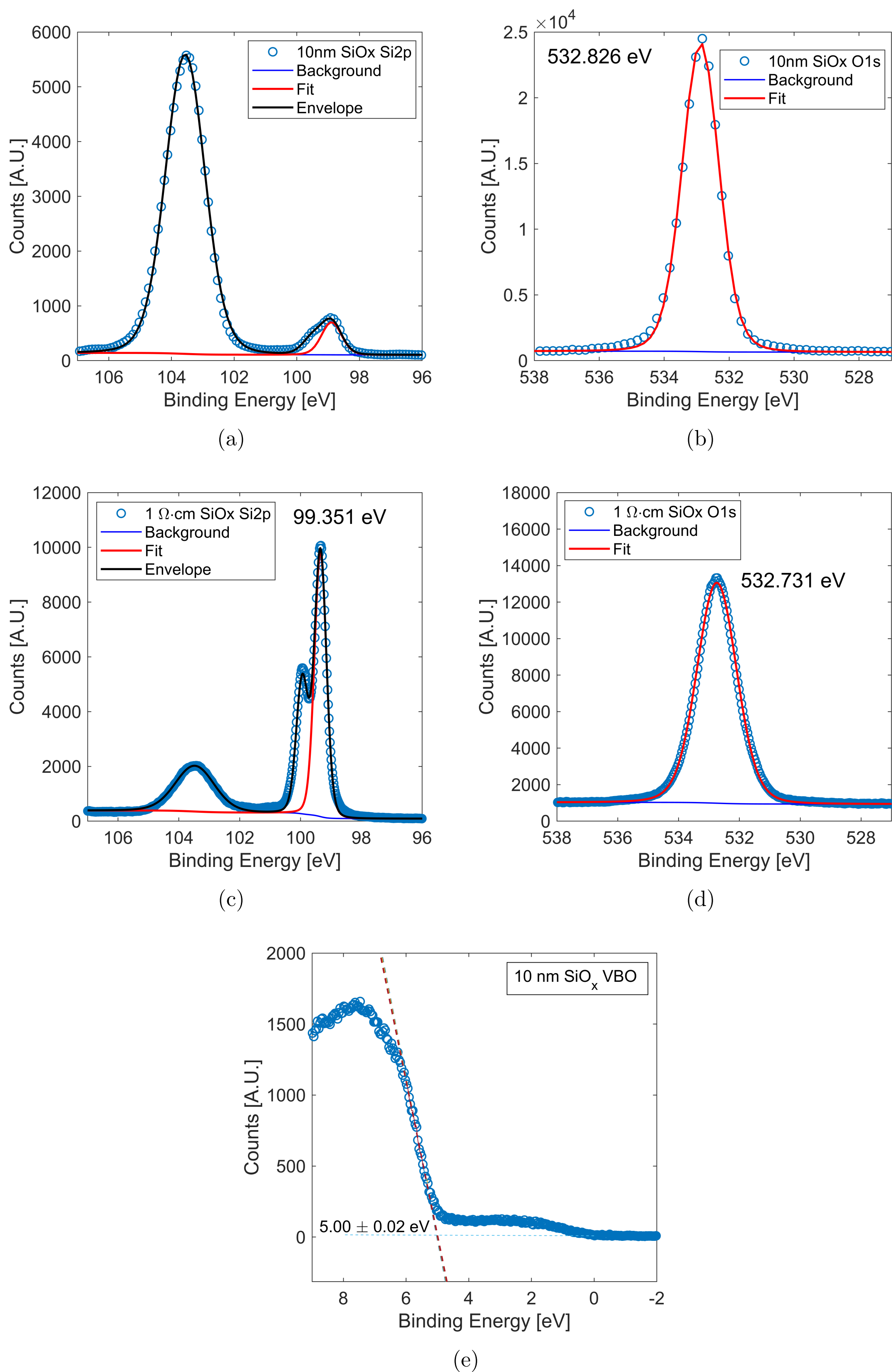


Figure 5.12: TSK XPS peaks for SiO_x a) 10 nm SiO_x Si 2p peak, b) 10 nm SiO_x O 1s peak c) 3 nm SiO_x Si 2p peak, d) 3 nm SiO_x O 1s peak, e) 10 nm SiO_x valence band onset.

Table 5.2: XPS Values for SiO_x VBO determination.

SiO_x Bulk	Wafer	Peak	VBO [eV]
10 nm	P1-10	O1s	4.46
10 nm	P1-10	Si2p	4.54
10 nm	P1-10	O1s	4.23[a]
10 nm	P1-10	Si2p	4.18[a]
100 nm	P1-10	O1s	4.36
100 nm	P1-10	Si2p	4.43
100 nm	P1-10	O1s	4.11[a]
100 nm	P1-10	Si2p	4.08[a]
10 nm	P1-5m	O1s	4.77
10 nm	P1-5m	Si2p	4.81
100 nm	P1-5m	O1s	4.69
100 nm	P1-5m	Si2p	4.6
	Average		4.4 ±0.2
	Average (P1-10)		4.30±0.16
	Average (P1-5m)		4.74±0.10
	Average (10 nm SiO_x)		4.50±0.2
	Average (100 nm SiO_x)		4.39±0.2
	Average (Si2p peak)		4.40±0.17
	Average (O1s peak)		4.42±0.2

[a] 10 s SiO_x interface sample

the SiO_x grown on P1-5m compared to P1-10 wafers. The low resistivity wafers will experience band gap narrowing in the Si due to the high doping concentration. The band gap narrowing is ~0.1 eV for boron concentrations of 10^{20} cm^{-3}, so it cannot fully explain the large discrepancy. The stoichiometry measured using the XPS shows similar Si:O ratios, but a high boron concentration could impact the SiO_x layer. The SiO_x grown into P1-5m Si will contain a high concentration of boron, which could alter the band structure of the SiO_x and result in a larger VBO.

5.4.4 Silicon Nitride

The VBO of SiN_x can vary depending on the deposition conditions and stoichiometry of the film. A large spread of VBO values is reported in the literature (Table 4.2). Hence, measuring the VBO of the PECVD SiN_x films grown here is critical. A 75 nm SiN_x layer is used for the bulk film and a 10 s deposition is used for the thin SiN_x layer, with a thickness of approximately 3 nm. The measurements were taken on P1-10 and P1-5m Si substrates, and for samples as-deposited and after a 450 °C hotplate anneal. In addition, an annealed 5 s PECVD SiN_x layer is also measured. The bonded Si2p and the N1s peaks are used to calculate the VBO. Figure 5.13 gives an example of peak fitting for SiN_x. The full set of peak fitting can be found in Appendix F and a summary of the calculated VBO values is given in Table 5.3.

There is substantial variation in the calculated VBOs in Table 5.3 with a minimum VBO of less than 1 eV and a maximum of over 2 eV. There are two clear trends in the results: an increased VBO is measured for the samples which have been annealed and a larger VBO is calculated when

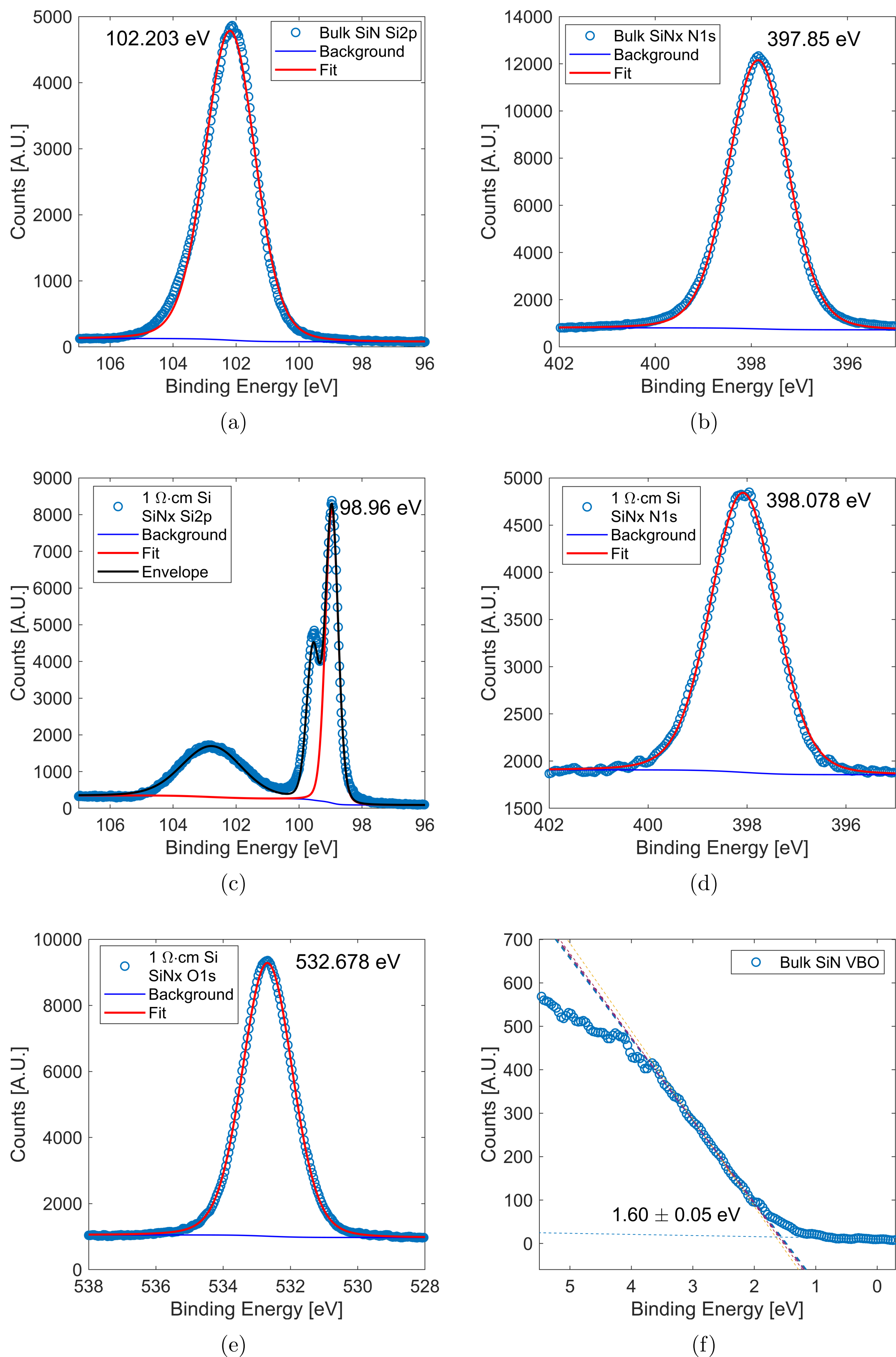


Figure 5.13: TSK XPS peaks for SiN_x annealed at 450 °C on P1-10 Si a) Bulk SiN_x Si 2p peak, b) Bulk SiN_x N 1s peak c) 3 nm SiN_x Si 2p peak, d) 3 nm SiN_x N 1s peak, e) Bulk SiN_x valence band onset.

Table 5.3: XPS Values for SiN_x VBO determination

Wafer	SiN_x Peak	Annealed	VBO [eV]
P1-10	Si2p	No	1.01
P1-5m	Si2p	No	1.32
P1-10	Si2p	Yes	1.51
P1-5m	Si2p	Yes	1.85
P1-10	Si2p	Yes	2.085[a]
P1-10	N1s	No	0.96
P1-5m	N1s	No	1.448
P1-10	N1s	Yes	1.244
P1-5m	N1s	Yes	1.58
P1-10	N1s	Yes	1.58[a]
		Average	**1.47±0.3**
		Average (P1-10)	1.41±0.4
		Average (P1-5m)	1.55±0.2
		Average (As Dep)	1.20±0.3
		Average (Ann)	1.64±0.4
		Average (Si2p peak)	1.57±0.15
		Average (N1s peak)	1.36±0.4

[a] calculated with a 5 s SiN_x interface sample

using the Si2p peak. These trends can be explained in relation to the composition of the films, shown in Figure 5.9(a). The anneal in air resulted in an increase in the oxygen concentration and suggests the formation of an oxy-nitride interfacial layer. This corresponds to an increase in the VBO as the nature of the interface is closer to that of the SiO_x. The VBO calculated from the 5 s PECVD SiN_x layer (indicated with superscript *a* in Table 5.3) is also larger than the equivalent sample with a 10 s PECVD SiN_x. The percentage of oxygen increases in the thinner SiN_x due to a larger contribution from the interfacial SiO_xN_y layer.

The presence of oxygen in all samples explains the increase in the VBO calculated when using the Si2p peak. This is because the Si is bonded to both nitrogen and oxygen, so using the Si peak will be influenced by the relative contribution of the SiO_x and SiN_x. It is seen that the discrepancy between the VBO values for the N1s and Si2p calculations is greater for the samples with a higher percentage of oxygen. Figure 5.14 compares the bonded Si2p peak for as-deposited SiN_x, SiN_x after annealing, an RCA+SiN_x stack after annealing, and an SiO_x layer. The spectra were normalised to the Si2p 3/2 peak maximum. The relative height of the bonded Si2p peak is dependent on the thickness of the dielectric layer. The position of the bonded Si2p peak gives some information on the nature of the dielectric layer and interface. The SiN_x has the lowest binding energy of 101.8 eV, which relates the lower oxygen content and VBO. After annealing, the oxygen content increases, which shifts the binding energy to 102.3 eV and results in a larger VBO. The RCA2+3 s SiN_x shifts the binding energy further to 103.1 eV. A distinct difference is seen between the RCA2+3 s SiN_x peak energy and the pure SiO_x so despite the very low N concentration in the stack, the SiN_x component is influencing the band structure of the dielectric layer. The SiO_x peak energy is measured at 103.75 eV, close to the expected value of 103.5 eV [313].

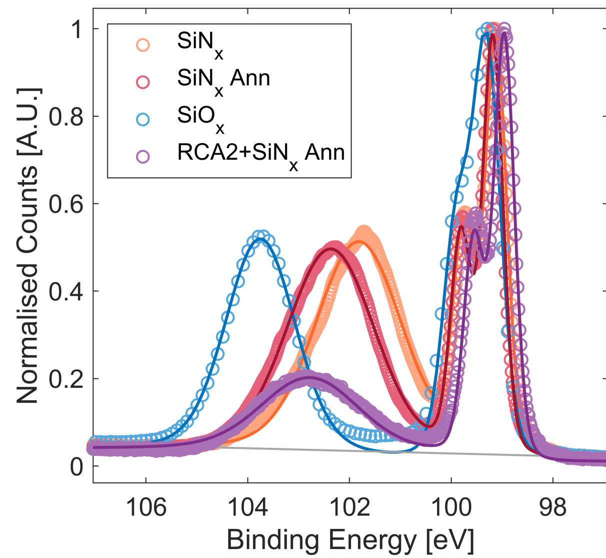


Figure 5.14: Normallised XPS spectra of the Si2p peak for SiN_x, annealed SiN_x, annealed a RCA+3 s SiN_x and an SiO_x layers on P1-10 wafers.

5.4.5 Aluminium Oxide

The AlO_x VBO is measured using 150 cycles for the bulk and 5, 10, 20, or 30 cycles for the thin film. This corresponds to a 15.5 nm bulk film and 1.2-4 nm thin layers. The AlO_x is deposited on P1-10 wafers and all samples had a 300 °C hotplate anneal before measurement. The Al2p or the O1s peaks are used for the core levels. Samples are measured in both the TSK and PhiV XPS. 10 cycles AlO_x measured in the TSK XPS is used for the example peak fittings and valence band onset measurement shown in Figure 5.15. A summary of the calculated VBOs is given in Table 5.4.

In the TSK XPS, there is a notably low signal-to-noise ratio for the Al2p peaks, as seen in Figure 5.15(a). The low signal is due to the AlO_x thickness of just 1.5 nm, and this may partly explain the large variation in the measured VBO between the 5 and 10 cycles. Another contribution to the discrepancy could be a variation in the stoichiometry of the films in the initial stages of deposition. The tabulated values of VBO show the calculated values using the O1s peak have a larger value than the Al2p peak. The VBO could be influenced by the interstitial SiO_x layer, similar to the effect seen using the bonded Si peak for the SiN_x offset. The excessive concentration of oxygen in the AlO_x thin films is also due to contamination on the film. The contribution of this is highest for the very thin films used here.

The PhiV measurements show more consistent results. The VBO is stable for an increasing number of deposition cycles, which means that the change in the measured stoichiometry of the AlO_x does not strongly influence the VBO of the film, at least for deposition cycles $\geq$10. Thus, using a single value of VBO is a valid approach for the simulations and theoretical fitting in Chapters 4 and 6, despite the changes in the stoichiometry of the thinnest layers. The PhiV XPS also shows an offset between VBO calculated using the Al2p and O1s peaks. A larger VBO is calculated using the oxygen peak, though the difference is smaller than seen in the TSK instrument. As the AlO_x thickness increases, the SiO_x interlayer will have a smaller influence on the signal. If the SiO_x interlayer is responsible for the increase in VBO then the discrepancy between the Al2p and O1s

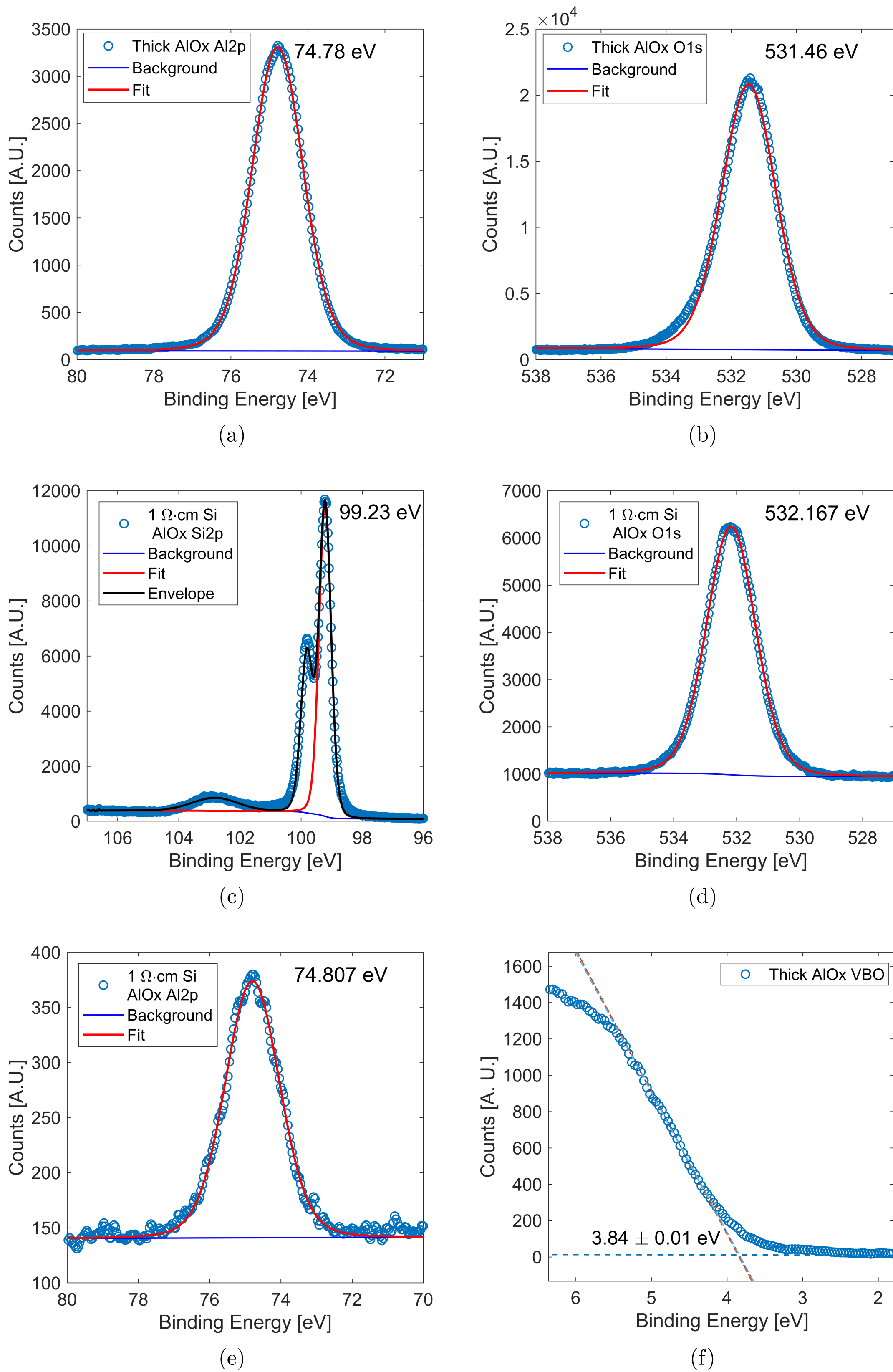


Figure 5.15: TSK XPS peaks for ALD AlO_x a) Thick AlO_x Al 2p peak, b) Thick AlO_x O 1s peak c) Thin AlO_x Si 2p peak, d) Thin AlO_x O 1s peak, e) Thin AlO_x Al2p peak, f) Thick AlO_x valence band onset.

VBO calculation would reduce as the AlO_x thickness increases. This is not seen and suggests that surface contamination is the cause of the increase.

5.4.6 Comparison of VBO for Dielectric Nanolayers

Figure 5.16 compares the calculated VBO for SiO_x, SiN_x, and AlO_x measured on P1-10 Si. Silicon oxide has the largest VBO of 4.3 eV. The value measured here is within the values reported in literature (Table 4.1). The variation between different samples and core level peaks is greater than the errors resulting from the core peak energies and valence band onset, so the error bars in Figure 5.16 are obtained from the standard deviation of the calculated values.

The processing conditions of SiN_x and AlO_x can alter the band offsets, as was seen in the VBO measurements of SiN_x before and after annealing. The values calculated in this section are within the range of reported literature values (Table 4.1). The SiN_x VBO is calculated as 1.4 eV, which is the lowest barrier to hole tunnelling of the dielectrics studied in this work. The largest SiN_x VBO of 2.09 eV, calculated for the thinner SiN_x sample after annealing, is still substantially lower than the AlO_x and SiO_x. The AlO_x VBO of 3.7 eV is one of the largest values reported in literature, though is still significantly lower than the SiO_x VBO and thus, SiN_x and AlO_x can produce higher tunnelling currents for the same thickness of nanolayer.

Table 5.4: XPS Values for AlO_x VBO determination on P1-10 wafers.

XPS	**AlO_x**	**Peak**	**VBO [eV]**
TSK	5 cycles	Al2p	3.69
TSK	10 cycles	Al2p	3.295
TSK	5 cycles	O1s	4.025
TSK	10 cycles	O1s	4.005
PhiV	10 cycles	Al2p	3.57
PhiV	20 cycles	Al2p	3.66
PhiV	30 cycles	Al2p	3.71
PhiV	10 cycles	O1s	3.76
PhiV	20 cycles	O1s	3.73
PhiV	30 cycles	O1s	3.79
	Average		3.72±0.2
	Average TSK(AL2p peak)		3.5±0.2
	Average TSK(O1s peak)		4.01±0.1
	Average TSK		4.01±0.1
	Average PhiV(Al2p peak)		3.65±0.1
	Average PihV(O1s peak)		3.76±0.2
	Average PhiV		3.7±0.1
	Average PhiV 10 cycles		3.7±0.1
	Average PhiV 20 cycles		3.7±0.1
	Average PhiV 30 cycles		3.75±0.1

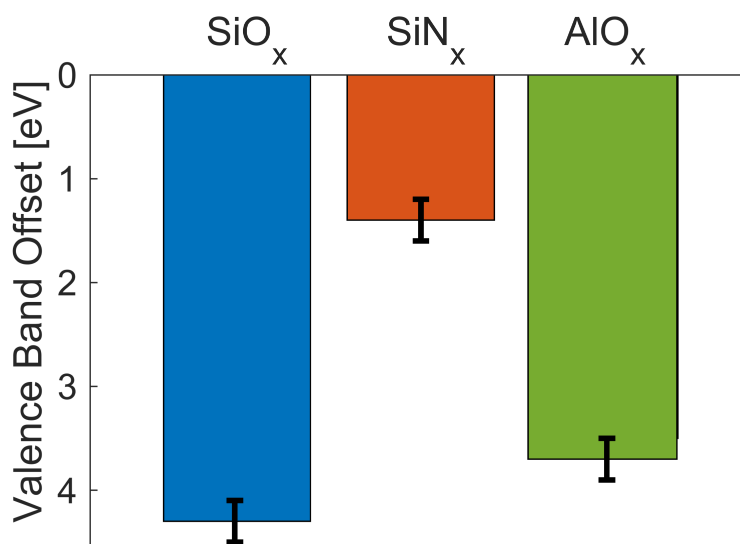


Figure 5.16: Valence band offsets of SiO_x, SiN_x and AlO_x to P1-10 Si.

5.5 Discussion

The growth of nanolayer dielectrics for tunnelling passivating contacts requires uniform thicknesses <2 nm, enabling a low resistivity and uniform passivation quality. SiO_x has been widely used, and many techniques have been used to grow the SiO_x layer. The growth is often self-limiting as the SiO_x is grown into the Si wafer. This aids the formation of uniform film thickness. The deposition of alternative dielectrics is generally carried out using ALD due to the slow controllable growth rates [170], [178], [205]. It was shown here that PECVD is also a viable technique for depositing nanolayer dielectrics. A plasma power of 20 W, has a sufficiently slow deposition rate to grow <2 nm films with uniformity ±0.1 nm. PECVD is widely used in industry, so could be an attractive option compared to the slower and more expensive ALD.

Accurately measuring the thickness of nanolayer films is difficult, with each of the different techniques having its own limitations. Ellipsometry is sensitive at nanometre thicknesses, provided the film's refractive index is known, but layers of surface contamination can impact the measurement. XPS is highly surface sensitive, with 80% of the signal generated in the first 5 nm of the sample. The relative intensity of the substrate and nanolayer peaks can be used to measure thin films <1 nm. Chemical analysis of the films can remove the contribution from the surface contamination, provided the peaks do not overlap with the sample's. However, XPS accuracy is limited by the assumptions required to determine the attenuation lengths and relative sensitivity factors, particularly when comparing results between different set-ups. TEM is an alternative method used to determine the thickness of nanolayer films [3], [128]. TEM gives atomic scale resolution images of the interface and therefore is the only technique to measure the thickness directly. However, the imaged region is highly localised, <100 nm, so the measured thickness may not represent the whole sample. The time-consuming nature of the measurements also means it is unfeasible to take measurements on multiple regions or for many samples.

Comparing the thickness obtained from two different measurement techniques can increase confidence in the accuracy of the measurements. This is particularly important due to the difficulties associated with measuring nanolayer films. Ellipsometry and XPS thickness measurements were used here. There were some discrepancies between the thicknesses measured using each method. However, given that ellipsometry and XPS calculate the thickness via two separate methods, and the difficulties discussed, it is not surprising that the results differ slightly. The difference is generally $<$0.5 nm, and given the assumptions in both techniques, there is reasonable agreement. In the cases where the difference is $>$0.5 nm the discrepancy could generally be explained by the stoichiometry of the film. It is also shown that the ellipsometry measurements have a high sensitivity for the relative thickness measurements between samples. The close fitting of the SiN_x and AlO_x growth rates indicates that ellipsometry measurements are self-consistent and valuable for a quick assessment and comparison between samples.

It was determined that the films can degrade in lab conditions, likely due to moisture absorption. To mitigate this, samples are stored in a N_2/vacuum and desiccated atmosphere and further processing, such as metal contact formation, is carried out as soon as possible after deposition. In poly-Si contact stacks, the poly-Si acts as a capping layer protecting the nanolayer dielectrics from degradation. For the poly-Si samples in Chapter 8, the dielectric nanolayers had to be transported to collaborators at EPFL for the poly-Si deposition. The samples were packaged in a vacuum and desiccated atmosphere to minimise any degradation. The SiN_x and AlO_x showed evidence of additional oxidation during the hotplate annealing in air. The impact of the additional oxidation is discussed in future chapters, though it could be avoided by annealing in an inert atmoshphere.

The stoichiometry of the bulk and nanolayer films was determined using the XPS spectra. The composition can vary significantly between the thin and bulk films. In all cases, the thin films have a higher concentration of oxygen, partly due to an increased contribution from contamination, but also a change in stoichiometry of the dielectrics for low thicknesses. The 3 s and 5 s SiN_x has an extremely low N concentration while the 10 s SiN_x has a Si:N ratio close to the bulk SiN_x. The ALD AlO_x samples show a gradual reduction in the Al concentration as the thickness is reduced, except the 5 cycles AlO_x deposited on oxide has a larger Al concentration. The deposition of nanolayer films is highly sensitive to the surface chemistry of the substrate. To deposit stoichiometric nanolayers $<$2 nm, the deposition parameters need to be significantly altered. The change in stoichiometry for the thin films could also indicate a potential error in the Krauts method for determining the VBO. The calculation assumes the core values in the bulk and thin film samples are the same. The different stoichiometry in the thin films could alter the energy of the core values. This effect is seen by the shift of the bonded Si peak in the SiN_x samples after annealing, and when an intentional SiO_x is added (Figure 5.14). In the AlO_x samples the stoichiometry did not strongly influence the VBO, and for $\geq$10 deposition cycles the calculated VBO was consistent.

The VBO calculations show significant variation for almost all parameters, including the XPS system, the Si wafer, the core level, and the processing conditions chosen. The calculation involves 6 energy levels that must be determined with high precision and accuracy. Slight errors in these measurements can result in significant differences in the final VBO calculated. Substantial variations in VBO are quoted in the literature, shown in Table 4.1. The large differences shown here highlight the sensitivity of the technique and, combined with variation in the dielectric deposition parameters, offer an explanation for the inconsistency in the VBO in the literature. Despite the variation in

VBO measured, there is a clear difference for the different dielectrics with SiN_x and AlO_x having a smaller energy barrier for hole tunnelling compared to SiO_x. For passivating contacts, a lower VBO allows thicker layers to be deposited, while maintaining a low tunnelling resistivity, thus relaxing the processing constraints for the dielectric synthesis. For SiO_x to form low resistivity contacts it requires the formation of pinholes. The density of pinholes must be carefully controlled to ensure low resistivity without reducing the passivation. The SiN_x and AlO_x layers can be deposited to 1.5–2 nm and, from simulations, can have a low resistivity, purely from tunnelling. This enables the post-deposition processing to be optimised for passivation without carefully controlling the pinhole formation and is investigated experimentally in Chapter 6.

The TiO_x nanolayers are fabricated by collaborators in AIST and therefore the deposition and processing details are not studied. The thickness of the TiO_x samples was measured as 6.8 nm using ellipsometry, a slight increase from the 5 nm measured in AIST. The increase is accounted for by high levels of contamination measured in XPS. The thickness of 4-5 nm measured using the Thickogram method agrees with the values from AIST. The stoichiometry of pALD and tALD TiO_x layers was compared. The layers had similar compositions, close to stoichiometric TiO_x. The difference between the pALD and tALD was in the interstitial SiO_x layer, with the layer being thinner in the tALD TiO_x. It is hypothesised that the interlayer could be crucial to determining the electronic properties of the Si/TiO_x interfaces. The VBO of the TiO_x could not be measured as the required bulk layers were not available. It was established in Chapter 4 that the dominant transport mechanism in TiO_x is not direct tunnelling so the VBO is not a critical parameter for TiO_x hole selective contacts.

5.6 Summary

The nanolayer growth, stoichiometry and VBOs of RTO SiO_x, PECVD SiN_x, and ALD AlO_x was studied. Uniform layers of <2 nm thickness were achieved for each dielectric. The layers are susceptible to degradation, predicted to be related to moisture absorption. The stoichiometry of the nanolayer films was shown to vary substantially from the bulk films, with the thin films measuring an increase in the oxygen concentration and a decrease in nitrogen and aluminium for SiN_x and AlO_x, respectively. The VBOs of SiN_x and AlO_x were shown to be lower than that of SiO_x. Table 5.5 provides the values of VBO used for simulations in Chapter 4 and for fitting the current-voltage measurements in Chapter 6. Due to the availability of the XPS and the measurement schedule, the values used were all taken from the TSK XPS, on P1-10 wafers.

Table 5.5: XPS Values for Simulations and Theoretical Fitting

Dielectric	VBO [eV]
SiO_x	4.3
SiN_x	1.4
AlO_x	3.5

Chapter 6

Carrier Transport in Nanolayer Dielectric Contact Structures

Dielectric nanolayers with thicknesses <2 nm have been fabricated with high levels of uniformity, and the VBO of the dielectrics to a silicon absorber was determined. A study of the carrier transport through the nanolayers is now presented. Temperature-dependent current-voltage (T-JV) is used to determine the conduction mechanisms in the dielectrics and confirms whether the nanolayer dielectrics form a complete layer, or if pinholes are present in the samples.

Contact resistivity (ρ_c) is a crucial parameter for passivating contacts. Full-area contacts require a contact resistivity below 100 mΩ·cm^2 to prevent a significant increase of the series resistance in a cell [108]. This is used as a target resistivity for the fabricated contact structures. The methods used to measure contact resistivity are described in Section 3.4 and some common pitfalls are discussed in Section 2.10. The current-voltage characteristics of metal-insulator-semiconductor (MIS) contacts using SiO_x, SiN_x, AlO_x, and TiO_x nanolayer structures are measured.

6.1 Contact Resistivity of Dielectric Nanolayers in MIS Structures

6.1.1 Influence of Capping Metal and Wafer Doping

In MIS contact structures, the contact resistivity is dictated by the probability of tunnelling through the dielectric and the energy of the Schottky barrier which forms at the silicon/dielectric interface. The type of metal contact, base wafer, and dielectric/Si interface will all affect the Schottky barrier and therefore influence the resistivity of the contact. The effect of the wafer resistivity and contact metal is measured and shown in Figure 6.1 for a 10 s RTO SiO_x layer.

The Au contacts give similar resistivity measurements for all wafer doping concentrations due to the high metal WF, which forms a low Schottky barrier. Conversely, the Al has a lower WF that results in a larger Schottky barrier height. In the P1-10 wafer, the electrons must be thermally excited over the barrier, resulting in a high resistivity. The P10-50m wafer has a similar resistivity, indicating thermal excitation over the barrier is still the primary conduction mechanism. The P1-5m sample has a significantly lower resistivity. This is due to a narrow Schottky barrier with a

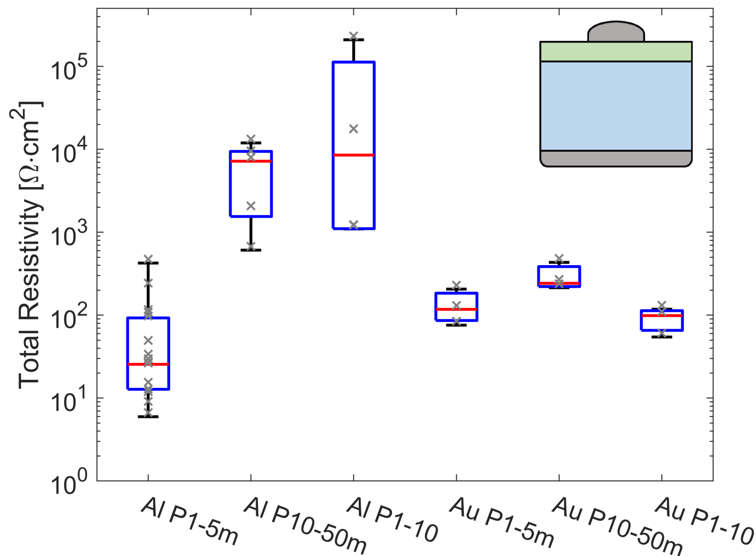


Figure 6.1: Resistivity of a SiO_x nanolayer determined from I-V measurements showing the influence of wafer doping and capping metal. Crosses show the resistivity of each measured metal contact. The inset shows a schematic of the sample structure.

high probability of holes tunnelling through. The probability of tunnelling is high, so it does not contribute significantly to the total tunnelling probability through the Schottky Barrier and the dielectric. The Al contacts all show a larger spread in the measured resistivity. This may be due to oxidation of the Al during deposition, causing a variation in the quality of the contact. The extent of the oxidation depends on the vacuum pressure, temperature, and deposition rate, which may change depending on the exact location of each contact dot within the chamber. The Au contacts are reliable, which is surprising as the Au does not adhere well to the silicon. This can result in the Au peeling off when the probes come into contact during testing, causing the contact area to vary. Incomplete contacting of the Au could explain the higher resistivity measured for Au contacts on P1-5m wafers.

Typical solar cell wafers have a resistivity of 1-10 Ω·cm. Dopant-free passivating contact (DFPC) structures must achieve a low contact resistivity on these wafers without the advantages of doping in poly-Si or PERC structures. This can be achieved using a high work function contact such as gold, but that is not a commercially viable option. Silver has a moderate WF of 4.7 eV [314] and is currently used in industry. ITO also has a high WF and is typically used in DFPC structures as a transparent contact to provide lateral conduction to metal contacts. Sustainability issues exist with using indium in solar cells, so an alternative high WF TCO is required for DFPCs. In poly-Si contacts, the poly-Si forms a silicon-insulator-silicon (SIS) contact, which does not form the same Schottky barrier. Additionally, the high-temperature anneal forms an in-diffused region of high dopant concentration, which increases the majority carrier concentration at the oxide interface and can lower resistivity. Low-resistivity wafers are used in the following section to mimic the effect of the diffusion and SIS structure of the poly-Si contacts.

6.1.2 Resistivity Dependence on Dielectric Thickness

J-V curves for SiO_x, SiN_x and AlO_x MIS structures are measured and shown in Figure 6.2. The shaded areas indicate theoretical curves for the thicknesses indicated in the legend. The thickness values in the plot show the measured thickness values from ellipsometry. The valence band offsets from Chapter 5 are used for the fitting (4.3 eV, 1.4 eV and 3.5 eV for SiO_x, SiN_x and AlO_x, respectively). The other fitting parameters are shown in the inset of each sub-figure. ϕ_b was set to 0 for the P1-5m wafers. This is because the high doping results in a narrow Schottky barrier, which can be tunnelled through. For a 1 mΩ·cm wafer and a barrier height of 0.15 eV, the Schottky barrier width is ∼3 nm. The probability of a hole tunnelling through this silicon barrier is ∼0.75. This has a very small effect on the tunnelling current, equivalent to an increase in SiO_x thickness of 0.02 nm.

The J-V curves of RTO SiO_x layers in Figure 6.2(a) show good agreement with the theoretical fits. The spread in the measured data requires a thickness variation of 0.1 nm in most cases, similar to the measured thickness variation from ellipsometry. The SiN_x J-V curves (Figure 6.2(b)) have a significantly larger spread in the J-V data, particularly for the thicker layers. The thinnest, 1.8 nm layer gives consistent measurements, and a similar thickness is obtained from fitting and ellipsometry. The large variation is not expected to be from thickness variations in the SiN_x as ellipsometry measured variation of <0.2 nm, and the SiN_x is less sensitive to changes in the dielectric thickness due to the lower band offset. The theoretical curves in Figure 6.2(c) show poorer fitting to the AlO_x experimental data, particularly at positive voltages. This corresponds to a reverse bias in the p-type Si substrate. The thickness determined from the theoretical fitting is considerably lower than the measured values from ellipsometry. The high reverse bias and lower thickness needed for fitting could indicate the presence of pinholes in the AlO_x samples.

The total resistivity of each structure is determined from the inverse gradient between ±0.01 V in the J-V curve and plotted in Figure 6.3. The ellipsometry measurements are used to define the thickness on the x-axis. A sample contacted immediately after an HF dip is used to indicate the minimum resistivity of the set-up. The parameters for the theoretical curves are shown in the insets of Figure 6.2. The SiO_x is the most resistive, with a 1.8 nm layer almost 3 orders of

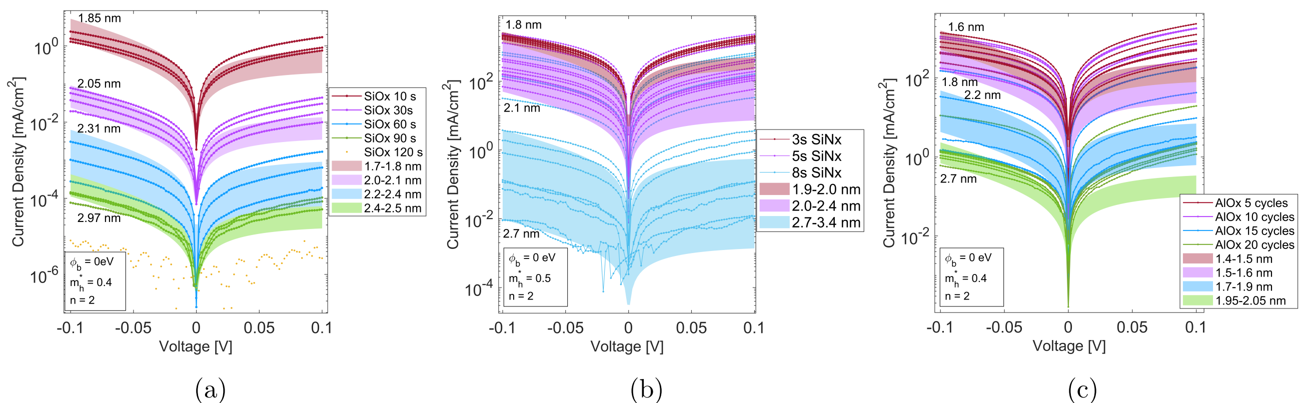


Figure 6.2: J-V curves of a) SiO_x b) SiN_x and c) AlO_x on P1-5m wafers. Experimental data are depicted as points with lines for a guide to the eye. Shaded areas give theoretical fitting and the thicknesses indicated on the plot are the values determined from ellipsometry.

magnitude larger than SiN_x or AlO_x contacts. For a given thickness, the lowest resistivity contacts are formed with SiN_x and the resistivity of AlO_x is between the SiO_x and SiN_x, as expected from the theoretical calculations. The slow growth rate of ALD allows thinner AlO_x to be fabricated, so a resistivity <100 mΩ·cm^2 is obtained for both the AlO_x and SiN_x nanolayers.

The SiO_x and SiN_x follow the predicted values, while the resistivity measured from the AlO_x nanolayers is lower than the theoretical tunnelling current. This could indicate the presence of pinholes in these samples. The SiN_x and AlO_x samples show a large spread in ρ_c at larger thicknesses. If this is due to a variation in the tunnelling probability, then (i) the thickness, or (ii) the VBO or m_h^* must be changing. For (i), the ellipsometry measurements in Chapter 5 indicate that the thickness is uniform across the sample to <0.1 nm. This is not a large enough variation to explain the large spread in resistivity. For (ii), although there is uncertainty in the determination of the VBO in Chapter 5, it is not expected that the VBO would vary across a sample. An explanation for the resistivity spread is if island or non-uniform growth occurs, on a scale too small to be measured by ellipsometry. Then there may be regions of native SiO_x that formed to cover exposed Si regions. Depending on the thickness of these regions compared to the deposited layer, this could increase or decrease the expected resistivity. Finally, the spread in the resistivity could be due to issues contacting the metal to the dielectric. This could result in variations in the quality of the contact, which could change the effective contact area.

6.1.3 Resistivity of RCA2+Dielectric Nanolayer Stacks

As discussed in section 2.3, it has been shown that the passivation quality of SiN_x and AlO_x can be significantly improved with the addition of a silicon oxide interlayer. SiO_x/dielectric stacks are widely used for surface passivation [52], however, the addition of the SiO_x will have an impact on the resistivity of the contact. An RCA2 oxide was chosen due to the self-limiting thickness of ∼0.7 nm [315]. Figure 6.4 compares the resistivity of the dielectric nanolayers with and without

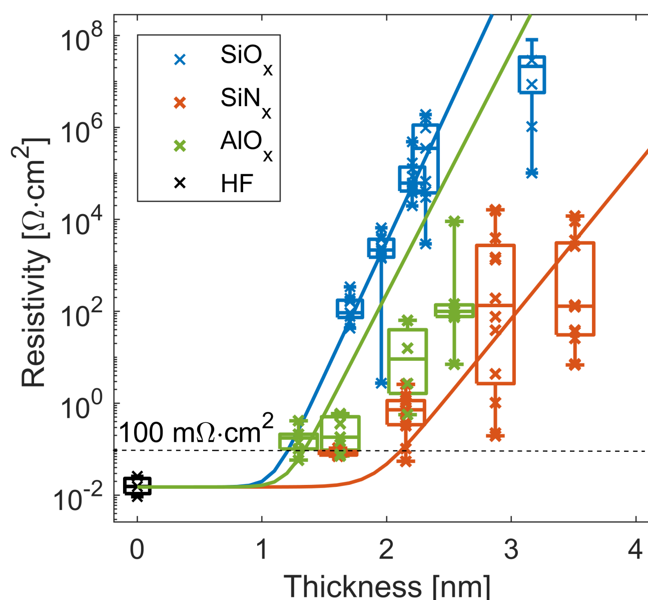
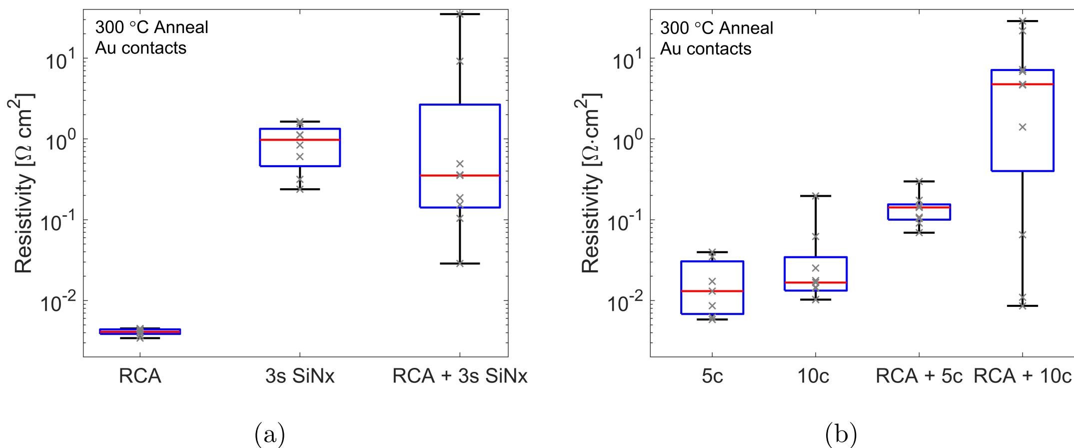


Figure 6.3: Resistivity as a function of dielectric thickness for SiO_x, SiN_x and AlO_x. Solid lines indicate the theoretical fitting for each dielectric, assuming the transport mechanism is purely tunnelling

the addition of an RCA2 interfacial layer. An RCA2 single layer is measured for reference. A single deposition was used for samples with and without the RCA2 to give a direct comparison.

The RCA2 alone forms the lowest resistivity contact, which is expected since it is a very thin oxide. In the 3 s PECVD SiN_x and the RCA2+3 s PECVD SiN_x samples in Figure 6.4(a) the resistivity is similar, though the RCA2+SiN_x stack shows a larger variation in the measured values. This was somewhat unexpected as the SiO_x nanolayer was thought to provide a more uniform sample surface, Photoluminescence images in Chapter 8 highlight non-uniformity in the RCA2+SiN_x process and could account for this spread. The resistivity of RCA2+AlO_x stacks and AlO_x single-layers are shown in Figure 6.4(b). The single-layer stacks show only a minor increase in the resistivity for the 10 cycles compared to the 5 cycles AlO_x. However, there is a clear increase in the resistivity for the RCA2 samples, particularly for the 10 cycles of AlO_x. The single layer SiN_x has a higher ρ_c compared to Figure 6.2, while the AlO_x ρ_c is lower, indicating some inconsistencies in the sample processing.

The contact resistivity is expected to increase by 10^4 due to an additional 0.7 nm SiO_x layer. Although the addition of the RCA2 oxide contributed to increased contact resistivity, the increase is smaller than expected. This is likely due to an unintentional oxide that forms in the single layers, even when the dielectrics are deposited immediately after the HF dip. A large unintentional oxide would explain the similar resistivity of the SiN_x and RCA2+SiN_x stacks.



(a) (b)

Figure 6.4: Resistivity of RCA2 stacks on P1-5m with gold contacts a) RCA2 single-layer, SiN_x single-layer and RCA2+3 s SiN_x stack b) RCA2+5 cycles AlO_x and RCA2+10 cycles AlO_x. Crosses show the resistivity of each measured metal contact.

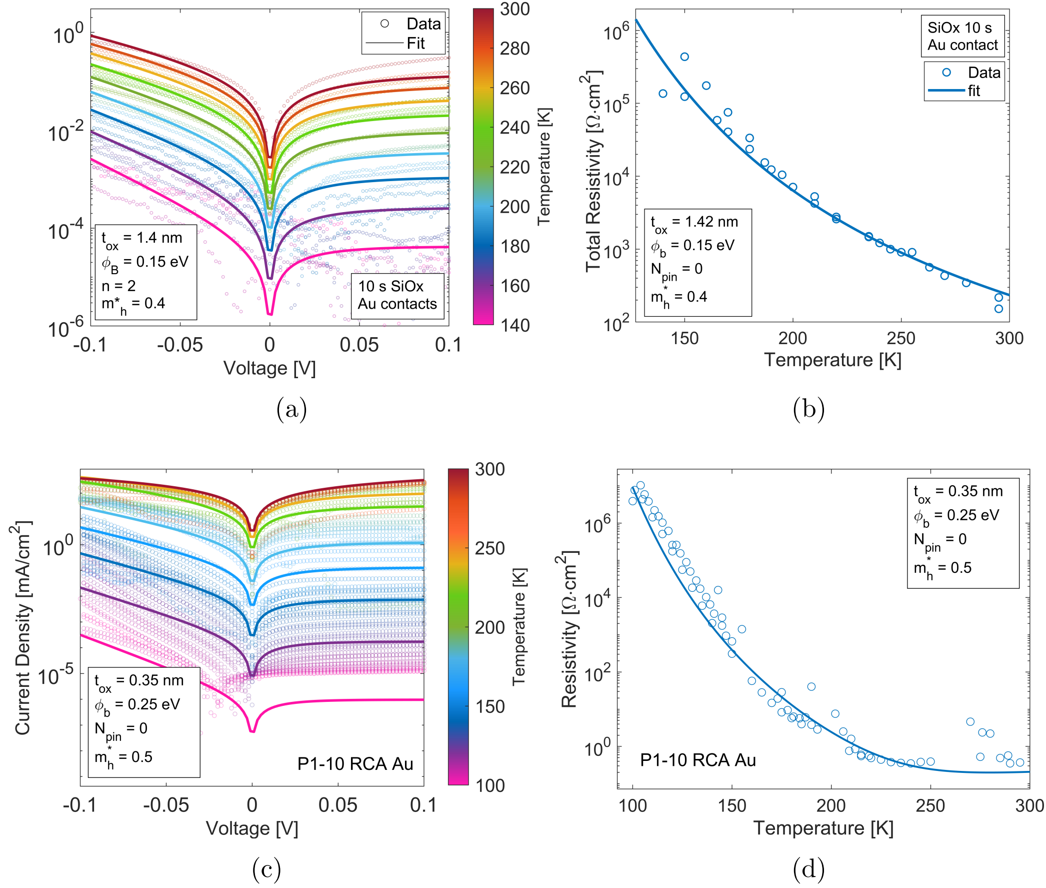
6.2 Determination of Conduction Mechanisms through Temperature-Dependent J-V

Temperature-dependent current-voltage (T-JV) are used here to determine the transport mechanism across each dielectric. The methodology is detailed in Section 3.4. The conduction mechanisms considered in the dielectric layer are direct tunnelling and direct silicon-metal contacts via pinholes. The temperature dependence of each mechanism is distinct, so the T-JV measurements allow the contribution of each to be distinguished. The tunnelling probability is independent of temperature, however, the tunnelling current strongly depends on temperature due to the thermal excitation of carriers over the Schottky barrier, thus the resistivity increases as the temperature decreases (Equation 3.19). Pinhole conduction has a weak temperature dependence related to the temperature dependence of the base wafer (Equation 3.17). At lower temperatures, the wafer resistivity decreases as there are smaller vibrations of silicon nuclei, resulting in fewer scattering events of the charge carriers. The fitting of the experimental curves was carried out using the resistivity data to determine the best parameters, these parameters were then used to generate theoretical J-V curves, which were compared to the experimental J-V measurements. P1-10 wafers are used in this section. The P1-5m wafers are unsuitable due to the narrow Schottky barrier that forms. Carriers tunnel through the Schottky barrier and the tunnelling current becomes independent of temperature. The P1-10 wafers result in a higher resistivity at room temperature compared to the ρ_c measured on the low resistivity P1-5m wafers (Figure 6.3).

6.2.1 Silicon Oxide

Current-Voltage measurements of a 10 s RTO SiO_x at temperatures from 300-150 K are shown in Figure 6.5. Figure 6.5(a) shows J-V curves (circle symbols), and Figure 6.5(b), the total resistivity as a function of temperature. The temperature-dependent resistivity is fitted to find the parameters shown in the inset. These values are inputted into the theoretical current equations (detailed in Section 3.4) and compared to the experimental J-V curves. The values used to fit the resistivity data also provides a close fit with the J-V curves, validating the models used. The fit is obtained with a purely tunnelling current, which shows that the SiO_x nanolayer does not present pinholes.

The temperature dependence of an RCA2 single-layer is measured before it is inputted into a stack with SiN_x or AlO_x. Figure 6.5(d) shows the RCA2 has a low resistivity at room temperature, but a steep increase when the temperature is lowered. This requires a large ϕ_b of 0.25 eV to fit the resistivity data. The measured thickness of the RCA2 oxide was ∼0.7 nm, but a lower thickness of 0.35 nm is required to fit the data. It is likely that the ellipsometer did not provide accurate thickness measurements for the <1 nm RCA2 oxide. The parameters fit the J-V curves in 6.5(c) closely.



(a) (b) (c) (d)

Figure 6.5: Temperature-dependent J-V measurements with theoretical fitting a) 10 s RTO SiO_x and c) RCA2 chemical SiO_x. The total resistivity as a function of temperature for b) 10 s RTO SiO_x and d) RCA2 chemical SiO_x. Open symbols show the experimental data and solid lines are obtained from theoretical calculations.

6.2.2 Silicon Nitride

The temperature dependence of a 5 s PECVD SiN_x layer is shown in Figure 6.6(b). The fitting procedure described above is used, and the results are shown in Figures 6.6(a) and 6.6(b). The best fit is again achieved for purely tunnelling current and provides close fitting to the J-V curves. The fitting is excellent in the forward bias (negative gate voltage due to the p-type substrate), though the reverse bias current is slightly larger than predicted from the model. This could be due to a small contribution from another conduction mechanism such as trap-assisted tunnelling or electron tunnelling. The addition of pinholes would not aid the fitting of the J-V curve so it is confirmed that a complete SiN_x nanolayer forms despite the short deposition time and ultra-thin nature of the film. The temperature dependence of an RCA2+3 s SiN_x stack is shown in Figures 6.6(c) and 6.6(d). To fit the data, the additional resistivity from the RCA2 oxide is incorporated into the SiN_x thickness, rather than adding the RCA2 layer separately. This is because the exact VBO and thickness of the RCA2 layer are not known. The analysis gives an effective SiN_x thickness for the stack. The RCA2+3 s SiN_x stack formed lower resistivity contacts than a 5 s SiN_x layer. The data is fitted with a tunnelling current and there is no contribution from pinholes. The addition of the RCA2 layer results in a lower ϕ_b compared to the SiN_x single-layer.

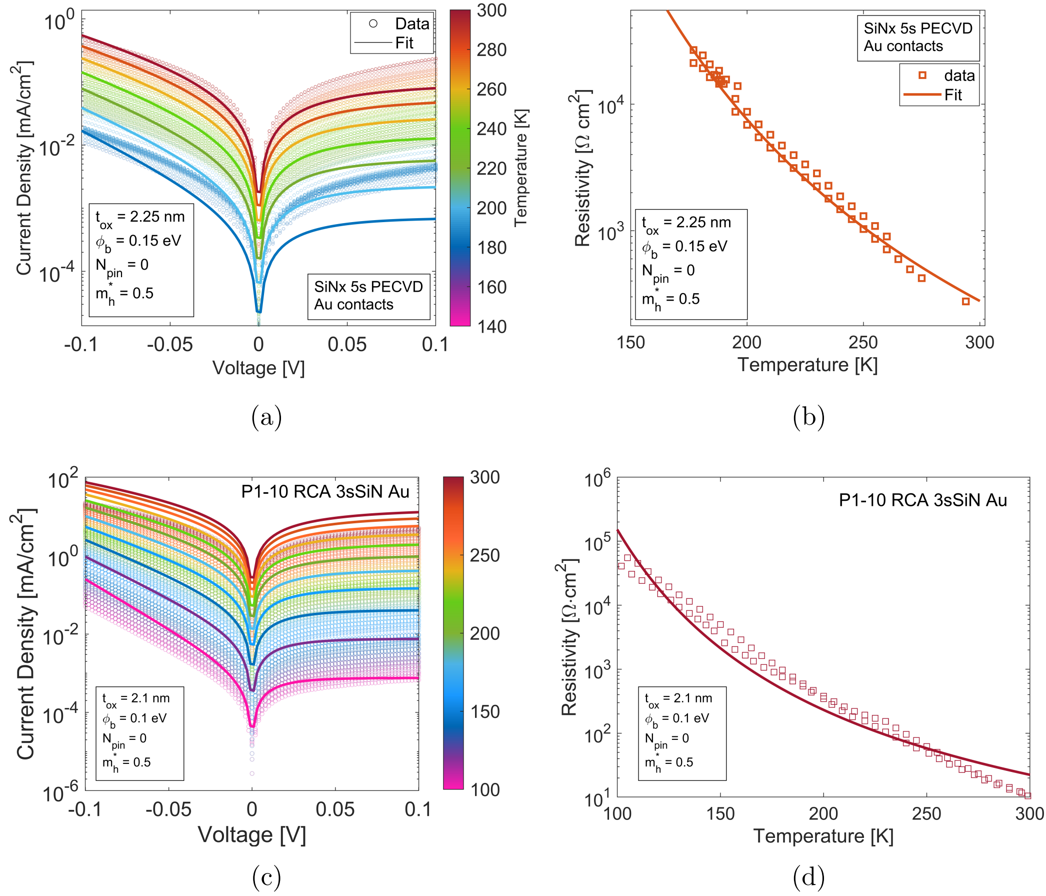


Figure 6.6: Temperature-dependent J-V measurements with theoretical fitting for a) 5 s SiN_x and c) RCA2+3 s SiN_x. Total resistivity as a function of temperature for b) 5 s SiN_x and d) RCA2+3 s SiN_x. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations.

6.2.3 Aluminium Oxide

A 5 cycles AlO_x nanolayer is measured in the same manner as the SiO_x and SiN_x. The J-V and resistivity curves are shown in Figures 6.7(a) and 6.7(b). A different trend in the resistivity is seen below ∼200 K, compared to the SiO_x and SiN_x T-JV curves. This indicates the presence of pinholes in the AlO_x nanolayer. The fitting of the J-V curves in Figure 6.7(b) uses a model which allows 'mixed mode' conduction with contributions from both tunnelling and pinholes. A close agreement with the experimental results is obtained. The tunnelling current dominates at higher temperatures and pinhole conduction becomes prominent below 200 K.

The temperature dependence of RCA2+5 cycles AlO_x stack is shown in Figures 6.7(c) and 6.7(d). A low ϕ_b is measured and is the cause of the lower resistivity compared to the AlO_x single-layer. An increase in the effective AlO_x thickness is due to the RCA2 oxide layer. The addition of the RCA2 oxide has not prevented pinholes from forming in the sample. This is surprising as the RCA2 single-layer stack did not contain pinholes. It indicates that chemical reactions at the interface between the AlO_x and the RCA SiO_x lead to structural changes in the film, likely due to the formation of Al-O complexes that dissolve or consume the thin SiO_x [316]. The concentration of pinholes is higher than the AlO_x single-layer, yet this could be attributed to sample variation.

Figure 6.7(f) shows a possible fit of the resistivity curve with pure tunnelling conduction. While this provided a close fit to the resistivity curve, poor fitting of the J-V curves is seen (Figure 6.7(e)). Hence the model including pinholes is representative of the sample.

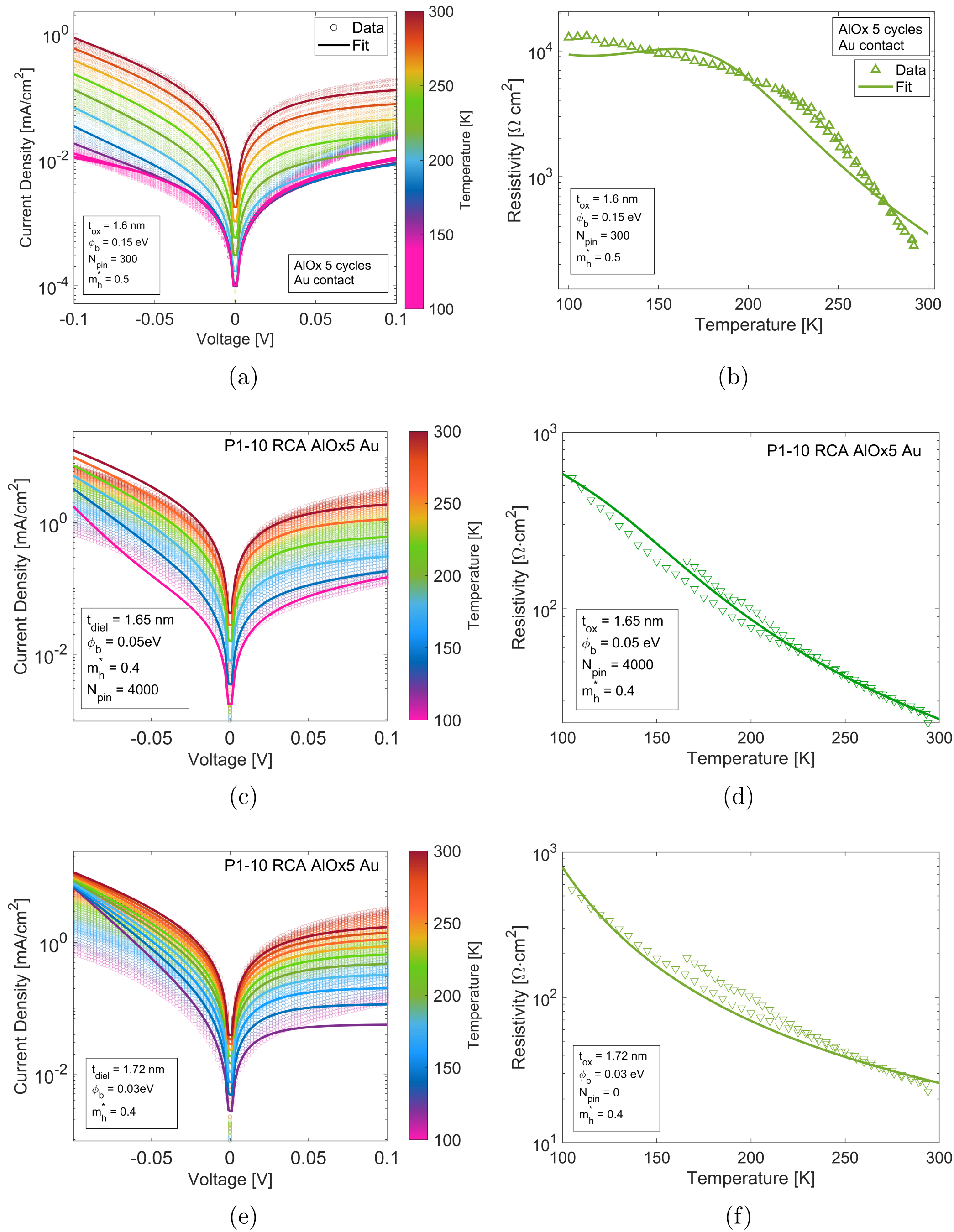
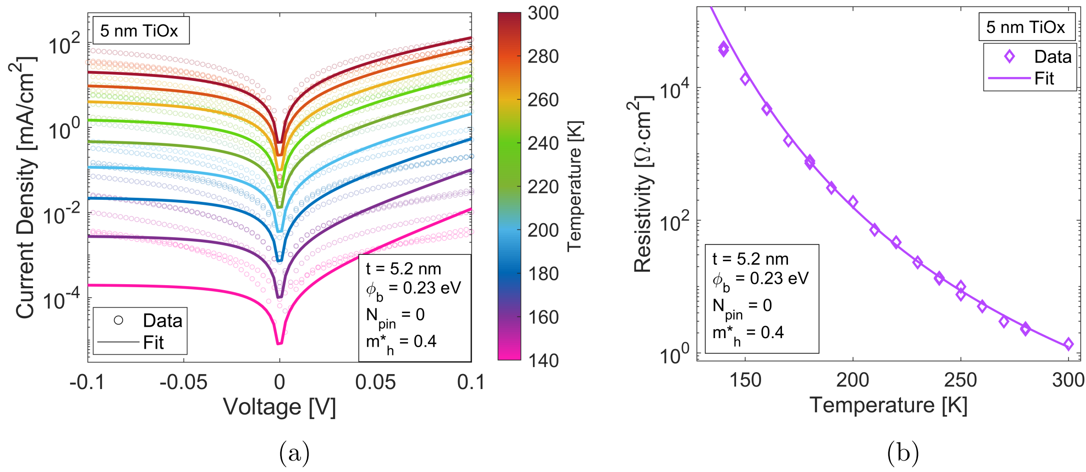


Figure 6.7: Temperature dependent J-V measurements with theoretical fitting for a) 5 cycles AlO_x and c) RCA2+5 cycle AlO_x. Total resistivity as a function of temperature b) 5 cycles AlO_x and d) RCA2+5 cycles AlO_x. e) and f) are the RCA2+5 cycles AlO_x measurements fitted with a purely tunnelling current. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations.

6.2.4 Titanium Oxide

The TiO_x samples are fabricated on 3 Ω·cm n-type wafers. T-JV is measured for the 5 nm TiO_x layer. A high current is obtained, with a total resistivity of 1 Ω·cm^2 at 300 K. This is modelled with a tunnelling current, but this is an electron tunnelling current as the n-type wafer has a supply of electrons which can tunnel through the small CBO of 0.1 eV or thermionic emission can excite electrons over the barrier. The fitting gives a thickness of 5.2 nm, which agrees with the XPS measurements (Section 5.1.4) and the TEM images from AIST [3]. A ϕ_b of 0.23 eV is measured, larger than the ϕ_b for the other nanolayers. The presence of a negative charge at the interface or the high WF of Au on n-type Si could cause increased band bending at the TiOx interface and contribute to the large value of ϕ_b.



(a) (b)

Figure 6.8: a) Temperature-dependent J-V of 5 nm TiO_x layer with Au contact b) TiO_x resistivity as a function of thickness. Open symbols show the experimental data and thick solid lines are obtained from theoretical calculations.

6.3 Discussion

The resistivity of nanolayer dielectrics is measured using MIS structures. Low resistivity wafers were used to mimic the high doping in poly-Si passivating contacts. This reduced the influence of the Schottky barrier, resulting in SiN_x and AlO_x contacts with a resistivity of 100 mΩ·cm^2. The use of low-resistivity wafers is not a perfect replacement for the poly-Si, as poly-Si contacts also include a high temperature anneal >800 °C. This anneal could alter the structure of the dielectrics, forming localised pinholes, or causing a widespread break-up of the film. The results on low resistivity wafers act as a proof of concept for SiN_x and AlO_x dielectrics to form low resistivity tunnelling contacts. Similar dielectrics have also been investigated in both DFPC and poly-Si contact structures [112], [115], [170], [207], [317]. The lowest resistivities previously reported are 200 mΩ·cm^2 for a AlO_x/poly-Si [170], [317] structure and 500 mΩ·cm^2 for a DFPC SiN_x [4]. Thus, the resistivities measured here are the lowest achieved for SiN_x and AlO_x nanolayer contacts. SiO_x p^+ poly-Si contacts have shown considerably lower resistivities, <10 mΩ·cm^2 [156], [187], [318], but it is expected to be from purely pinhole conduction [147]–[149]. The T-JV measurements are the first determination of the conduction mechanisms in nanolayer SiN_x and AlO_x nanolayers. It

was found that the low resistivity SiN_x contacts have a purely tunnelling current, with a close agreement to the simulations in Chapter 4. The ALD AlO_x has a small current contribution from pinholes in the thin films measured, though hole-tunnelling contributes significantly, and would dominate conduction at a cell's operating temperature.

In DFPC structures, the highest performing cells typically have ρ_c between 30-200 mΩ·cm^2 [112]. Metal oxides with a negative valence band offset are commonly used, which allow the use of thicker layers. The resistivity of ~100 mΩ·cm^2 reported in this work for both the SiN_x and AlO_x nanolayers are comparable, though for DFPCs the low contact resistivity must be obtained on 1–10 Ω·cm wafers. For the nanolayers to be implemented into DFPCs in full cells, lateral conduction is required, either through a full-area metal contact or a transparent conductive oxide (TCO). The choice of metal or capping material can have a significant influence on ρ_c (as shown in Figure 6.1). Further investigation into the contact resistivities for different TCO layers is necessary for implementing the nanolayers into full cells. There is also scope to combine the nanolayers in stacks with the metal oxides currently used in DFPCs [319].

The RCA2 oxide produced contacts with a low resistivity of 10 mΩ·cm^2. However, this low resistivity cannot simply be added in series to the resistivity of a SiN_x or AlO_x single-layer to give the total resistivity of a contact stack. The resistivity of the stack is determined by combining the tunnelling probability through the RCA2 oxide and additional dielectric layer together. The addition of a 0.7 nm SiO_x layer is expected to increase the contact resistivity by a factor of ~10^4. However, fitting the RCA2 oxide temperature-dependent J-V measurements gave a lower thickness of 0.35 nm. A 0.35 nm SiO_x would increase the contact resistivity by a factor of 100. The resistivity of an RCA2+SiN_x contact did not increase compared to the SiN_x single-layer, and only a small increase in the contact resistivity was observed for an RCA2+5 cycles AlO_x contact. There are two mechanisms which account for the small increase in resistivity. First, the SiN_x and AlO_x single-layer stacks have an unintentional SiO_x layer. This is estimated in Chapter 5 to be ~0.8 nm for PECVD SiN_x and thermal ALD AlO_x, so the thickness increase with the intentional RCA2 layer is minimal. Secondly, from inspection of the T-JV curves, it is seen that the addition of the RCA2 oxide results in a reduction of the ϕ_b. The smaller ϕ_b compensates for the increased thickness and as a result, the RCA2 stacks do not cause a large increase in the resistivity. The lower ϕ_b also implies a lower D_{it} at the Si/dielectric interface. This is an encouraging indication that the RCA2 oxide can improve the passivation quality of the nanolayer dielectrics, as was intended. Poly-Si contacts with a thermal SiO_x interlayer in combination with AlO_x or SiN_x nanolayers have been fabricated [170], [187]. The stacks measured a ρ_c of 70 mΩ·cm^2 in both cases, lower than achieved for the SiN_x or AlO_x single layers. As these contacts are SIS structures, a Schottky barrier is not present and therefore does not explain the reduction in resistivity. A possible explanation for the lower ρ_c in AlO_x structures is a higher negative charge for AlO_x deposited on SiO_x, compared to H-terminated silicon. This is discussed further in Chapter 7.

The hole conductivity across the TiO_x layer could not be assessed as the layers were deposited on n-type wafers. The low contact resistivity obtained from dark J-V measurements is purely a result of electron conduction over, or through, the small CBO in the TiO_x. To assess the hole transport through the layer, illumination of the sample is required to generate a concentration of holes. A light J-V measurement could be performed, where poor hole collection through the TiO_x would be seen as a high series resistance. Additionally, if the TiO_x also allows electron collection,

a low shunt resistance would be observed. Alternatively, the TiO_x could be deposited on p-type wafers. Matsui et al. [194] measured the dark IV and obtained ρ_c of 1 Ω·cm^2. T-JV measurements could offer insight into the conduction mechanisms in the TiO_x and provide possible routes to decrease the resistivity.

6.4 Summary

The transport properties of the dielectric nanolayer films are crucial for their application to passivating contact structures. MIS structures were used to study the conductivity of the films. The experimental results showed good agreement with the theoretical calculations, with the thinnest SiN_x and AlO_x samples exhibiting a contact resistivity <100 mΩ·cm^2. In the RCA2+dielectric stacks, the increase in dielectric thickness is compensated for by a reduction in ϕ_b so the contact resistivity increase is smaller than expected from theory. Temperature-dependent resistivity measurements were used to determine the conduction mechanisms in the films. The SiO_x, SiN_x and TiO_x films could all be fitted through a model based on tunnelling current alone, while the AlO_x showed contributions from tunnelling and pinholes in both the single-layer and the RCA2+AlO_x stack.

Chapter 7

Passivation at Silicon-Nanolayer Dielectric Interfaces

The silicon/dielectric interface is investigated in each dielectric system to determine the passivation quality. Several methods are used and compared to develop a detailed understanding of the Si/nanolayer interfaces. Lifetime measurements provide the overall passivation quality of the interface but cannot distinguish between chemical or field-effect passivation. The high conductivity of the nanolayer films prevents many standard techniques from being used to find the density of interface states and fixed charge at the Si/dielectric interface. SPV is an effective technique for analysing the thin dielectrics as the probe is not in contact with the sample, so no carrier transport can occur. SPV can give approximate values of D_{it} and Q_f, however, the parameters are linked so neither can be obtained with high precision. In addition, two novel methods were developed to give a more complete view of the silicon/dielectric interface. The first uses the conductance-voltage curve to determine the charge at the interface, and the second utilises a PECVD SiO_x capping layer to block the high leakage current from the nanolayer, allowing a high-quality C-V measurement to be taken. The details of these new techniques are covered in the next section, then the techniques are applied to the nanolayer dielectric structures in this work.

The high doping concentration in P1-5m wafers affects the techniques and prevents the extraction of D_{it} and Q_f. In SPV, the minority carrier density generated by the light is significantly lower than the majority carrier concentration in the wafer, so the light does not manipulate the carrier concentration sufficiently to influence the band bending in the silicon. In C-V, the extremely narrow Schottky Barrier means there is no distinction between the accumulation and depletion capacitance, and in G-V, high conduction is observed in depletion, so V_{FB} cannot be determined. Instead, the SPV, C-V and G-V analysis is carried out on P1-10 wafers. N30-60 wafers are used for lifetime measurements, due to the low bulk lifetime of the P1-10 and P1-5m wafers.

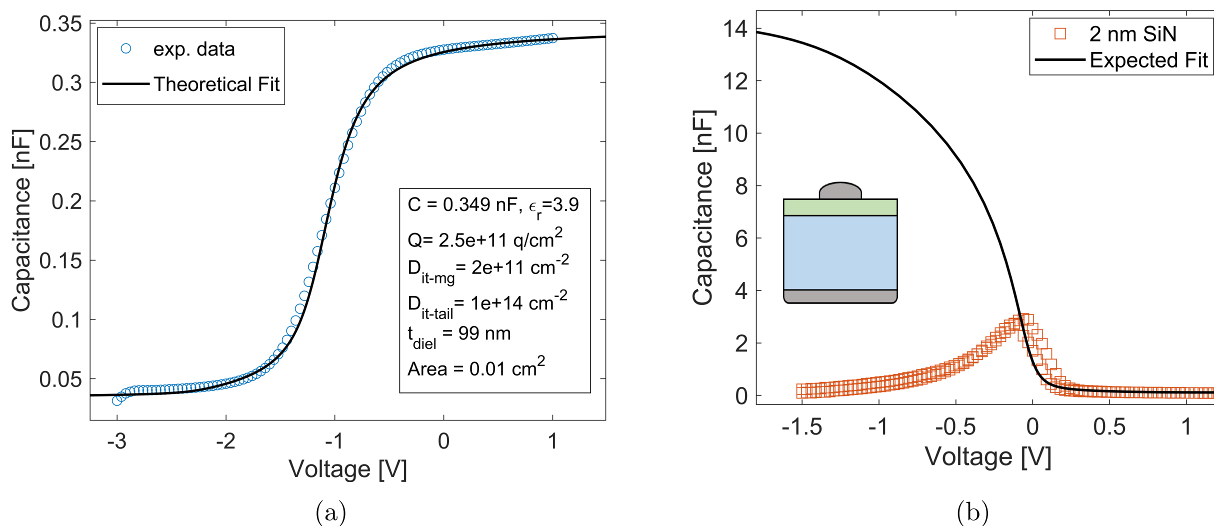
7.1 Development of Novel Characterisation Techniques

Capacitance-voltage, conductance-voltage, SPV, and biased photoconductance all provide information on the relative contribution of chemical and field-effect passivation at silicon/dielectric interface. Fitting the measurements to theoretical calculations enables the fixed charge and defect density at silicon/dielectric interfaces to be determined. These techniques use the modification of the carrier

concentrations at the silicon surface to alter the band bending and induce changes in the measured property. An example of this is shown in Figure 7.1(a). Capacitance-voltage measurements are performed on a 100 nm thermal silicon oxide. The S-shaped capacitance curve can be fitted to obtain D_{it} and Q_f with high accuracy and precision. The analysis is described in detail in Section 3.6. Figure 7.1(b) highlights the difficulty with applying this technique to MIS structures with a thin dielectric. The C-V curve for a 2 nm SiN_x layer is compared to the expected capacitance for the structure. In depletion, the curves are well matched as the depletion region in the silicon dominates the capacitance. Near the flatband voltage, there is an increase in the capacitance as charge density at the silicon surface begins to increase. However, as the voltage applied becomes more negative, the capacitance drops and deviates from the expected curve. This is due to the high conductivity in the nanolayer film. As the carrier concentration at the Si/dielectric interface increases, the carriers will conduct through the dielectric. The high density of carriers being swept across the interface will prevent any further increase in the carrier density at the Si surface. This means full accumulation is not reached and the measured capacitance does not reach the expected insulator capacitance. The high conductivity also affects the source meter's ability to measure capacitance accurately and is seen by the drop in capacitance to ∼0 nF at high negative potential. Extracting quantitative values for D_{it} and Q_f is not possible. Therefore, alternative methods are here developed to analyse the nanolayer dielectrics, to understand and improve passivating contact structures.

7.1.1 Conductance-Voltage, G-V

Conductance-voltage measurements were introduced in Section 3.6.1. The procedure for determining the dielectric charge using G-V is now described. In a well-insulated MOS structure, the conductance is generated by the movement of charge in and out of interface defect states. Figure 7.2(a) shows the G-V curve for a 100 nm thermal SiO_x layer. When V_{gate} is far from the band gap of silicon, the conductance is low as the AC signal does not affect the carriers in the silicon. The increase in the conductance is seen when $V_{gate} \approx V_{FB}$ The spike is due to the defect states at the interface. Figure



(a) (b)

Figure 7.1: C-V curves for a) thermal 100 nm SiO_x layer on n-type Si b) a thin, leaky dielectric on p-type Si.

7.2(a) shows the effect of D_{it} and Q_f on the theoretical G-V curves. The reduction of Q_f shifts the curve right on the voltage axis, as is seen in C-V measurements. The change in D_{it} narrows the conductance peak but also shifts the voltage at which there is maximum conductance.

Figure 7.2(b) gives an example of the case where the dielectric is thin and leaky, carriers being transported across the junction under forward bias can contribute to the conductance signal. When V_{gate} instigates a reverse bias on the junction, the silicon is in depletion, and there are very few minority carriers, so the conductance is low. Thus, as the voltage is swept from depletion, through V_{FB} and to accumulation, the conductance will rise at V_{FB} and stay high when the silicon is in the accumulation regime. Near V_{FB} the conductivity could have contributions from both the interface states and carrier transport across the interface. To carry out the analysis, the onset of high conductance was taken at the value above which the high conductivity could not be explained by interface states. Once V_{FB} has been determined, the charge in the dielectric can be obtained. It is determined by comparing the voltage to the absolute charge at the silicon/dielectric interface, ($|Q_{abs}|$). The bottom plot in Figure 7.2(c) shows the fitting of the G-V curve to the $|Q_{abs}|$ minimum. The green line shows that the $|Q_{abs}|$ is almost entirely independent of D_{it}, and thus the Q_f can be extracted without significant influence from the other interface parameters. The dielectric thickness has a significant influence on the $|Q_{abs}|$ curve. The orange line in Figure 7.2(c) shows the influence on the $|Q_{abs}|$ curve for a 1 nm decrease in t_{diel}. For quantitative extraction of Q_f, an accurate thickness of the dielectric is required.

The interface state conductivity is dependent on the measurement frequency. High-frequency measurements show higher conductivity when the conductivity is dominated by highly mobile charge carriers, such as electrons, switching in and out of interface defect states [46]. For thin dielectrics, with conductivity dominated by the carrier transport across the interface, the conductivity is independent of measurement frequency, as seen in Figure 7.2(b). G-V curves are measured at various frequencies to ensure the conductivity is dominated by the charge transport through the dielectric. The final measurements are taken at a low frequency ($\leq$10 kHz) to minimise the contribution of interface states.

7.1.2 Capped C-V measurements

An alternative method to determine the interface properties of a highly conductive dielectric is to obtain high-quality C-V measurements by limiting the conductivity of the thin film. The standard measurement procedure is described in Section 3.6. The capped C-V method developed here uses a 100 nm PECVD SiO_x layer deposited onto the nanolayer dielectrics using the recipe described in Section 3.1.3. The thick SiO_x suppresses the high conductivity, while the original Si/dielectric has the strongest influence on the C-V. The low charge in the silicon oxide ensures that no additional FEP is added with the additional layer. Some beneficial hydrogenation may occur, though this is not a problem as hydrogenation steps would always be carried out in a full contact structure. Figure 7.3 shows a C-V curve for the PECVD SiO_x layer. The charge and D_{it} are slightly higher than the thermal 100 nm SiO_x. The high D_{it} is as expected for a low-temperature deposition of SiO_x and will not affect the measurements. The charge of 7–8$\times10^{11}$ q/cm^2 might have a small influence on the underlying dielectric, this will result in a small systematic error in the absolute value of Q_f extracted. The charge likely forms at the Si/dielectric interface, which is not present when PECVD SiO_x is used as a capping layer on another dielectric. Therefore, it cannot be corrected for by simply

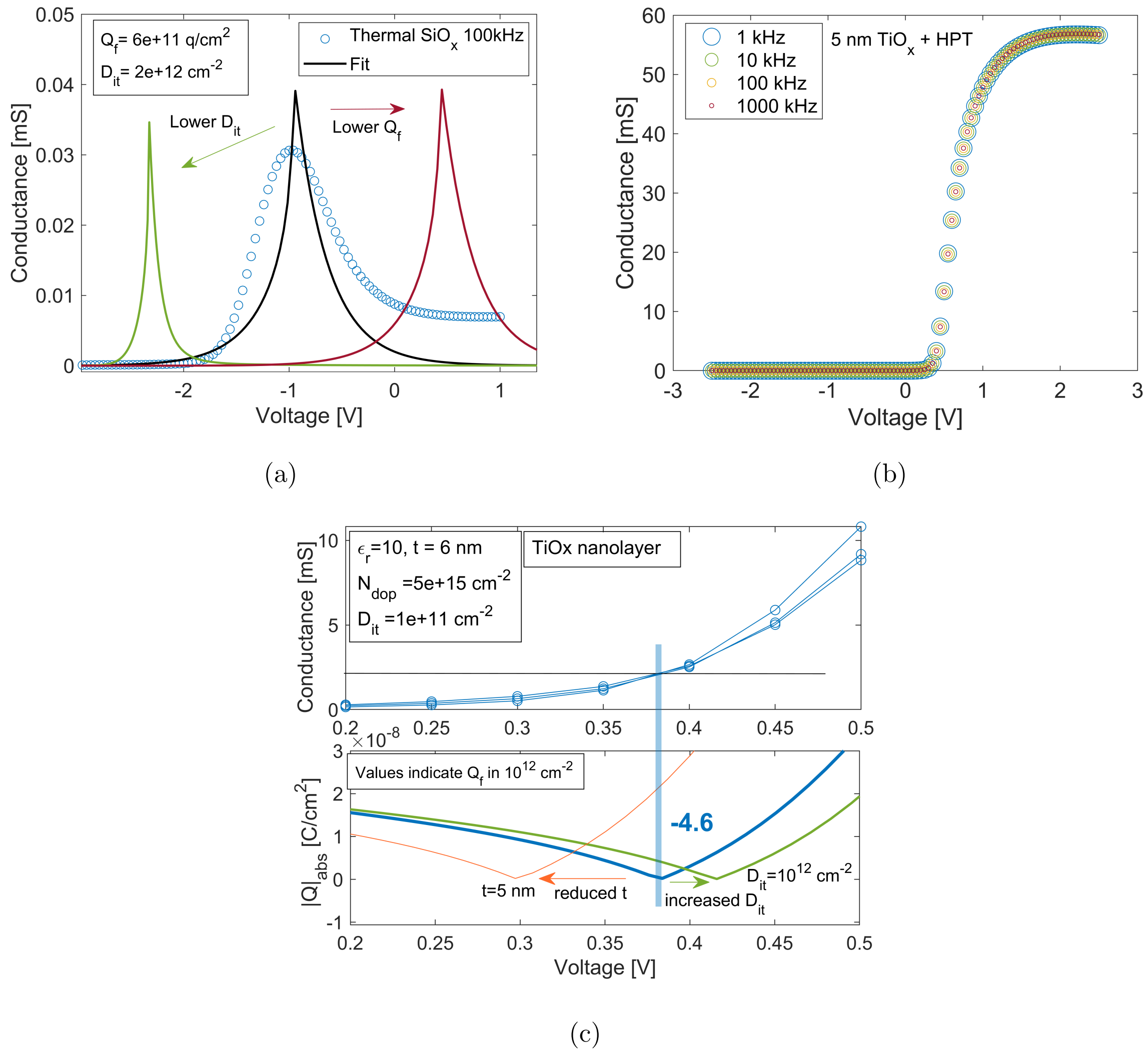


Figure 7.2: G-V curves for a) a highly resistive, thick dielectric b) thin, leaky dielectric c) Example of fitting the G-V curves to the $|Q_{abs}|$.

subtracting the charge in the PECVD SiO_x from the value measured in the dielectric/SiO_x stack. The influence of this charge is considered in the discussion of the results. The error is systematic, so is consistent for all measurements and therefore the comparison between samples is unaffected.

C-V measurements are performed on P1-10 wafers at 1 MHz using aluminium contacts. The work function for Al is set to 4.2 eV and the contact area is used as a fitting parameter. The maximum minority carrier lifetime of the PECVD SiO_x layers was measured at an anneal temperature of 350 °C. This is considered the optimum anneal T for C-V measurements, though in some cases the dielectric+SiO_x stack was annealed to temperatures up to 550 °C.

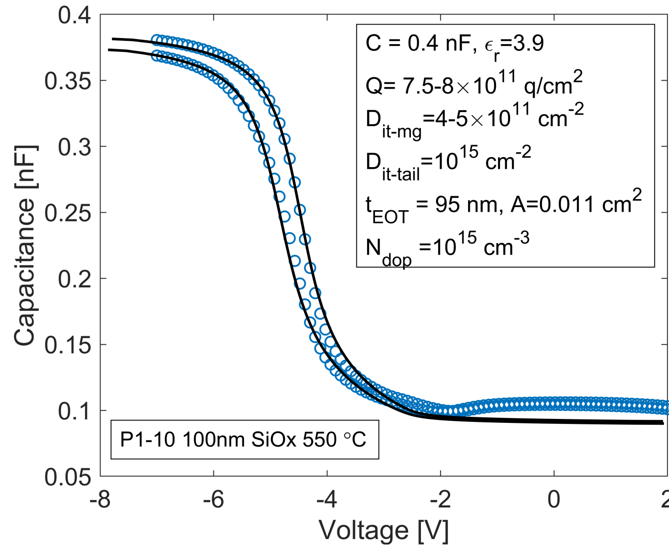


Figure 7.3: C-V measurement of 100 nm PECVD SiO_x with 350 °C hotplate anneal and Al contacts

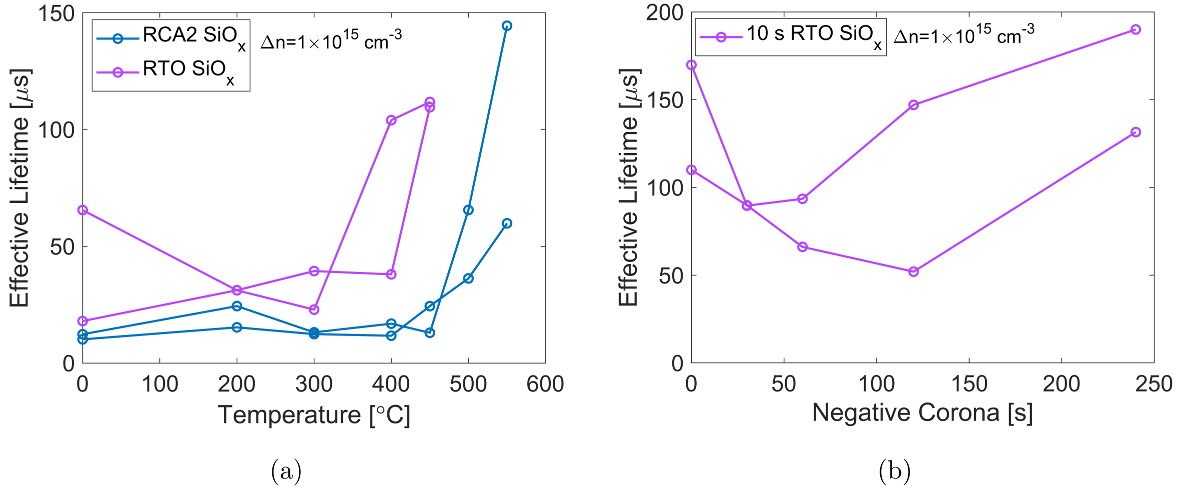
7.2 Silicon Oxide Interface Nanolayers

The interface properties of RTO and RCA2 silicon oxide nanolayers are investigated. SiO_x has been studied extensively as a thick layer and is the most thoroughly studied nanolayer dielectric. A low charge is expected, while the D_{it} depends on the processing route [130]. Lifetime measurements, SPV and the capped C-V measurements are carried out to characterise the interface properties.

7.2.1 Lifetime Measurements

Photoconductance lifetime measurements give an overview of the passivation quality. Figure 7.4 shows the effective lifetime of SiO_x nanolayers on N30-60 wafers during post-oxidation treatments. In Figure 7.4(a), each samples underwent a series of hotplate anneals. The samples were heated for 5 min at each temperature, then allowed to cool before the lifetime measurement. The lifetime is low, considering the bulk lifetime of >1 ms and wafer thickness of 700 µm of the N30-60 wafers. The RTO was grown at 800 °C so the low-temperature anneal should have a minimal influence. There is a small increase in the lifetime during the anneal, most likely due to the expulsion of moisture. The removal of moisture during low-temperature annealing was seen in thickness measurements carried out in Chapter 5. The maximum lifetime of 100 µs is low and indicates a high D_{it} in the thin film, or potential contamination in the furnacre. The RCA2 oxide is much thinner and formed at a low temperature, so the low lifetime is not unexpected. An increase in the lifetime is observed during annealing at temperatures above 500 °C. This could be due to some additional oxidation of the SiO_x, or the re-ordering of bonds at the Si/RCA2-SiO_x interface to reduce the D_{it}.

In Figure 7.4(b) negative corona charge was deposited on both sides of the SiO_x nanolayer. This was to imitate the FEP obtained during the deposition and anneal of poly-Si in full contact structures. An initial decrease in the lifetime indicates a small positive charge in the SiO_x dielectric structures. The density of charge on the sample due to the corona charge is difficult to estimate as the dielectric structures' thin, leaky nature will neutralise the charge, and this is seen by the large variation in the time to reach the minimum τ_{eff} in each sample. The peak lifetime of the



(a) (b)

Figure 7.4: Effective lifetime of a) 10 s RTO SiO_x and an RCA2 SiO_x on N30-60 with a hotplate anneal, and b) a 10 s RTO SiO_x with negative corona charging. Lines are a guide to the eye, with each line representing a separate sample

SiO_x remains low, which either shows the SiO_x nanolayers cannot hold a high density of charge or provides further evidence that the bulk may be contaminated.

7.2.2 SPV

Figure 7.5 shows SPV measurements of 10 s RTO SiO_x on P1-10 as a function of annealing temperature. The CPD is measured in the dark and under illumination. In all cases the SPV value ($CPD_{dark} - CPD_{light}$) is negative and there is little change with annealing temperature. This is expected for the high-temperature growth method. The increased spread in the data is likely a result of sample manipulation during the measurements. The as-grown SiO_x has a dark CPD value of -0.3±0.05 V and a light CPD of -0.05±0.05 V, indicating a SPV value of ∼0.25 V. D_{it}-Q_f maps are shown in Figure 7.6 and the parameters used are detailed in Appendix D. Estimations of the density of interface states, $D_{it,mg}$ and interface charge, Q_f can be made and are indicated by the red lines in the figure. It suggests a low charge $<1\times10^{11}$ q/cm^2 and a D_{it} around 1×10^{12} cm^{-2}.

7.2.3 Capped C-V

Capped C-V measurements of the RCA2 oxide were carried out. The RCA2 oxide was grown on P1-10 Si and then 100 nm of SiO_x was deposited. The samples were then measured after an anneal at 350 °C or 550 °C. Figure 7.7 plots the experimental and fitted capacitance-voltage curves for the RCA2+SiO_x stacks and the extracted values of Q_f and D_{it} are shown in Table 7.1.

Table 7.1: Fitted Q_f and D_{it} from C-V of RCA2 SiO_x

Anneal T [°C]	Q_f [$\times10^{12}$ q/cm^2]	D_{it} [$\times10^{12}$ cm^{-2}]
350 °C	1.05	0.4–0.6
550 °C	0.87	0.6–0.9

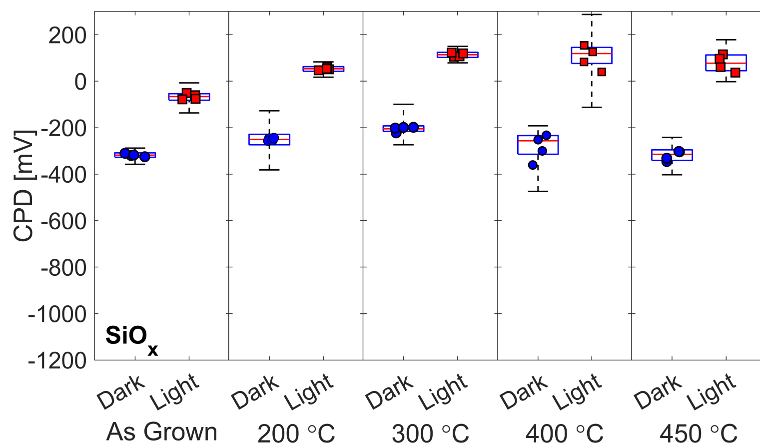


Figure 7.5: CPD of SiO_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map.

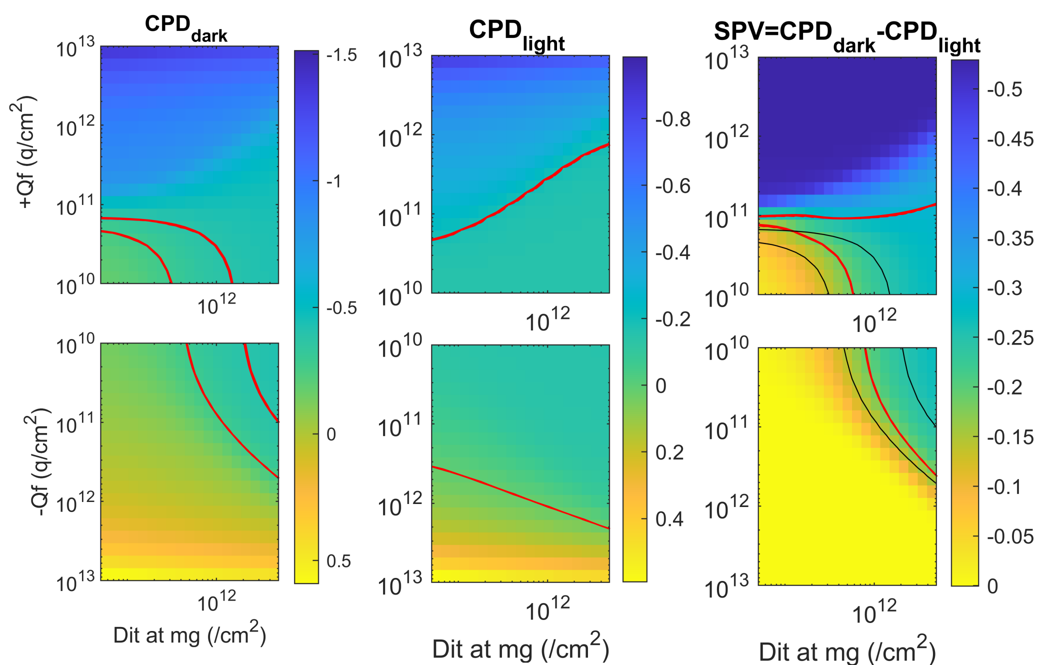


Figure 7.6: Estimated D_{it} and Q_f from SPV results. Red lines indicate the CPD values from Figure 7.5. Black lines show the CDP_{dark} values superimposed on the SPV plot.

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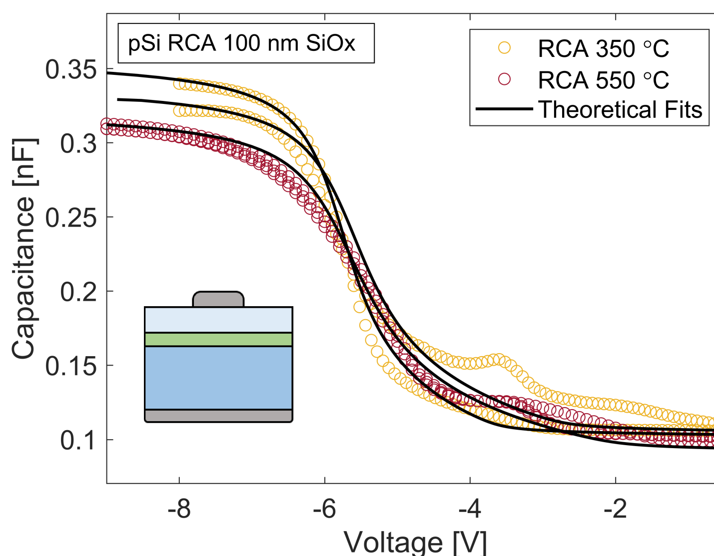


Figure 7.7: Capped C-V measurements of RCA2 SiO_x layer for varying anneal temperature. Inset shows a schematic of the measured structure.

The charge of 0.9–1×10^{12} q/cm^2 is similar to that of the PECVD SiO_x. The PECVD SiO_x may contribute to a slight increase in the charge, but in any case, the charge is low. There is a slight increase in the D_{it} at higher anneal temperatures. Higher annealing temperatures typically reduce the D_{it} due to the re-ordering of bonds at the Si/dielectric interface [185]. A potential cause of the increase could be due to thermal shock when the sample is remove from the hotplate.

7.2.4 Summary

The SPV, capped CV and the corona-lifetime measurements all indicate a low positive charge in the RTO and RCA2 SiO_x. The interface is not significantly altered by the moderate temperature anneals. A low Q_f of $<10^{11}$ q/cm^2 combined with a D_{it} of 1×10^{12} cm^{-2} is estimated from SPV measurements. The combination of low charge and moderate D_{it} can account for the low lifetime. The capped C-V measurements produced a slightly lower D_{it} of 4–9×10^{11} cm^{-2} for the RCA oxide, likely due to the result of some hydrogenation during PECVD. These results are in reasonable agreement with literature values of nanolayer oxides [119], [130], which gives confidence in the techniques when implementing them on the novel dielectrics discussed in the rest of this chapter.

7.3 Silicon Nitride Interface Nanolayers

The interface properties of PECVD SiN_x layers and RCA2+SiN_x stacks are investigated following the same methodology as with the SiO_x.

7.3.1 Lifetime

The effective lifetime of the SiN_x nanolayers is shown in Figure 7.8. The SiN_x was investigated as a single layer and in a stack with an RCA2 oxide interlayer. Figure 7.8(a) shows the change in

the effective lifetime for increasing hotplate anneal temperature. The single-layer stacks have low initial lifetime, and only a small increase is seen with the hotplate anneal. The stack shows a more promising lifetime with an increase to over 200 µs for the 600 °C anneal. The increase in lifetime occurs at the same temperature as the RCA2 single layer in Section 7.2.1. The lifetimes are still relatively low compared to the bulk lifetime of the N30-60 wafer.

Figure 7.4(b) shows the effect of negative corona charge on the effective lifetime. The negative corona was applied after the hotplate anneal. The single-layer stacks show a small improvement in lifetime. The RCA2+SiN_x stack effective lifetime decreases with the negative corona charge, indicating positive charge inside the dielectric stack. The minimum τ_{eff} is reached after 30 s corona charge. The total charge deposited after 30 s is $\sim 5\times10^{12}$ q/cm^2, representing an upper limit to the Q_f in the RCA+SiN_x stack. It is likely that carrier transport through the dielectric neutralised some of the deposited charge, so the true Q_f is likely considerably lower. After the minimum is reached the lifetime does not reach the same high value of τ_{eff}. The low lifetime after a negative corona suggests that either: the conduction of carriers across the dielectric prevents a high concentration of holes forming at the interface so an inversion layer in the Si is not formed, or a large capture cross-section of electrons limits the lifetime, as has been seen elsewhere [320], [321]. A Si-Si defect in the SiN_x is proposed to contribute to the large capture cross-section [320], [321]. The silicon-rich nature of the films, determined in Chapter 5, could result in a high density of these defects.

7.3.2 SPV

SPV analysis is performed on the SiN_x layers after the hotplate anneals at increasing temperatures. Figure 7.9 shows the CPD values for a 5 s PECVD SiN_x. In all cases, the SPV is negative, though there are clear changes in the signal over the temperature range measured. Anneal temperatures up to 350 °C cause an increase in CPD values, indicating a reduction of positive charge, or formation of negative charge. At 350 °C the CPD_{dark} is -0.4 V and the CPD_{light} is -0.35 V, with a very low SPV of just 0.05 V. Above 350 °C the CPD becomes more negative, and the SPV increases, suggesting a

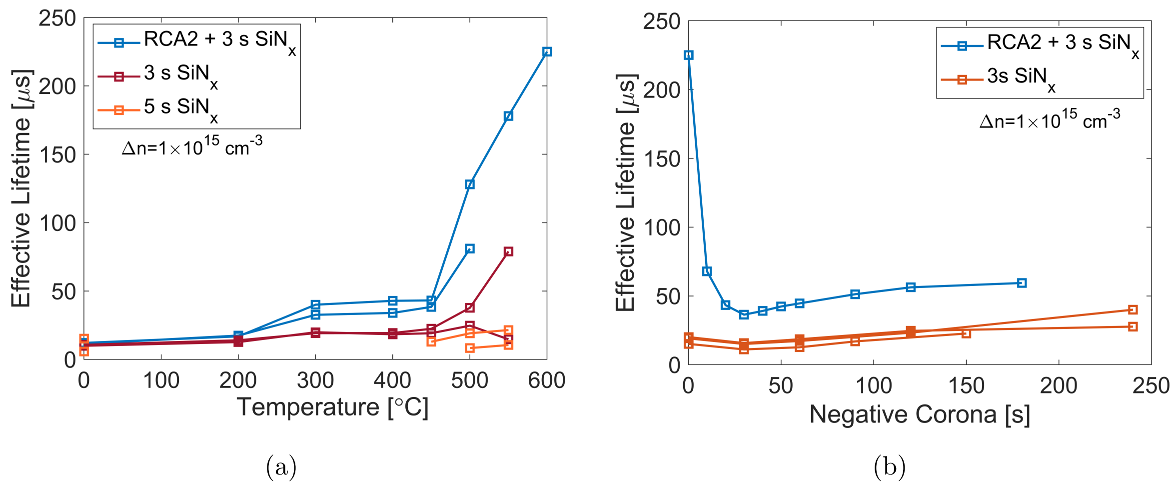


Figure 7.8: Effective Lifetime of SiN_x on N30-60 for a) increasing anneal temperature b) deposition of negative corona charge. Lines are a guide to the eye, with each line representing a separate sample.

positive charge is formed. Figure 7.10 shows simulated D_{it}-Q_f maps for the SiN_x nanolayers. CPD values for 350 °C are indicated with the contour lines. From inspection, the values indicate a low positive Q_f ($\sim10^{11}$ q/cm^2) and D_{it} ($\sim10^{11}$ cm^{-2}) in the SiN_x. At 450 °C the CPD becomes more negative, with a larger SPV, indicating an increase in the positive charge between 10^{11}-10^{12} q/cm^2.

7.3.3 Capacitance and Conductance Measurements

Capacitance and conductance-voltage measurements of the SiN_x nanolayers are shown in Figure 7.11 for increasing SiN_x deposition times. The deposition times correspond to t_{diel} from 2-4 nm. The C-V shows the S-shaped curve however, the accumulation capacitance is $\sim\frac{1}{3}$ of the expected value for the films. The G-V curves show the sharp increase in conductivity for the thinnest films, but the thicker layers maintain low conductance. The bottom plot in Figure 7.11 shows the G-V fit for the 5 s SiN_x layer. A large charge density of 1.1×10^{13} is required to match the onset of high conductivity. There is also an offset between the rise in capacitance at 0.2–0.5 V and the initial rise in conductivity at -0.4 V. It is therefore suspected that the SiN_x nanolayers are in an intermediate regime between the low conductance regime that enables reliable C-V analysis, and the high conductance regime, where the charge can be accurately extracted via the G-V measurements.

The capped C-V analysis is used for a more precise determination of the charge and D_{it} present in the nanolayer dielectrics. The samples are measured after 350 or 550 °C hotplate anneals. Figure 7.12 shows the C-V curves for the SiN_x single layers and RCA2 stacks and Table 7.2 summarises the extracted Q_f and D_{it}. The C-V measurements show similar curves for all processing conditions. The charge and D_{it} are similar to that of the RCA2 single layer. The most significant shift is seen for the RCA2+5 s SiN_x after a 350 °C anneal. A larger Q_f of 1.4×10^{12} q/cm^2 is measured in combination with a slight reduction in D_{it} to 5×10^{11} cm^{-2}.

7.3.4 Summary

The SiN_x nanolayers have low effective lifetimes, particularly under negative corona. The cause of this low lifetime is analysed via SPV, G-V and capped C-V measurements. The SPV and C-V

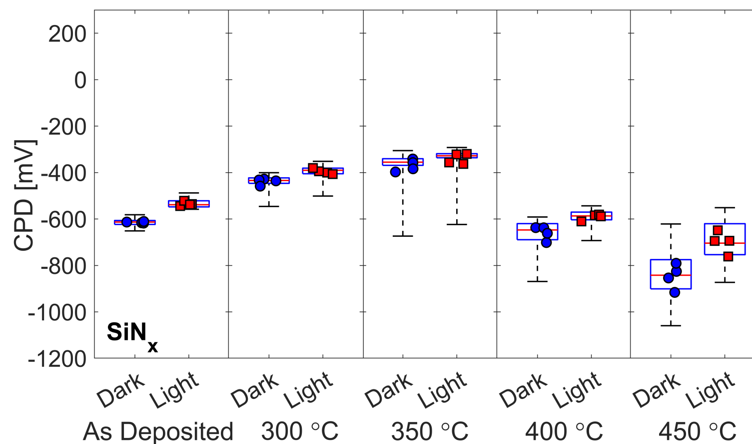


Figure 7.9: CPD of SiN_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map.

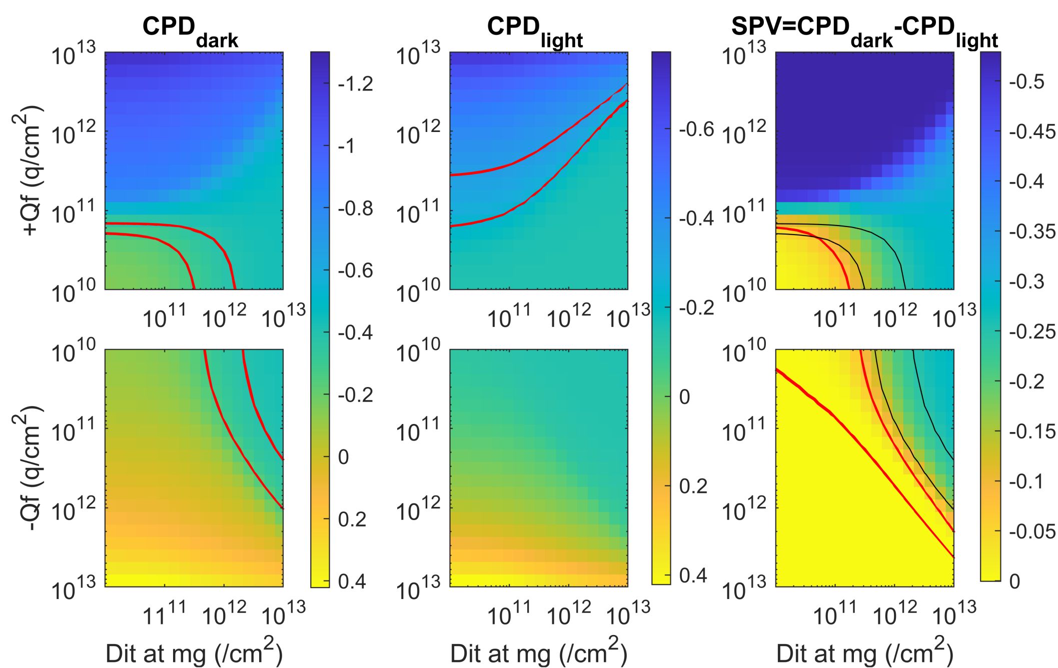


Figure 7.10: Estimated D_{it} and Q_f from SPV for a 5 s SiN_x annealed at 350 °C. Red lines indicate the CPD values from Figure 7.9. Black lines show the CDP_{dark} values superimposed on the SPV graph

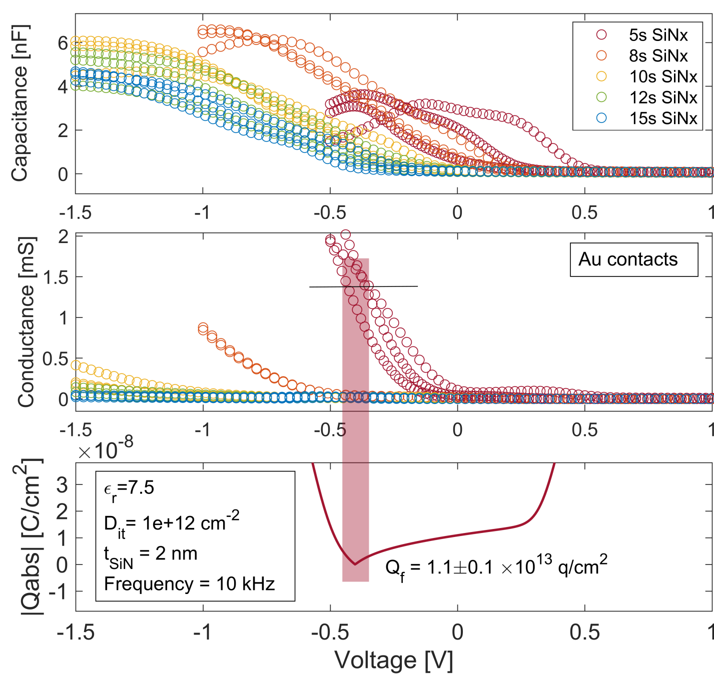


Figure 7.11: G-V of SiN_x for increasing deposition time on P1-10 wafers and with Au contacts.

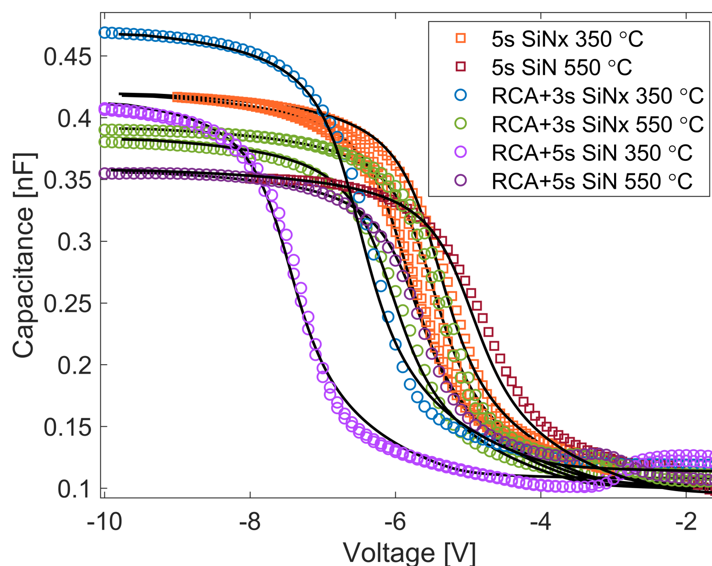


Figure 7.12: Capped C-V measurements of SiN_x and RCA2+SiN_x layers for varying anneal temperature.

Table 7.2: Fitted Q_f and D_{it} from C-V of SiN_x and RCA2+SiN_x stacks

Dielectric	**Q_f [$\times 10^{12}$ q/cm^2]**		**D_{it} [$\times 10^{12}$ cm^{-2}]**	
Anneal T [°C]	350	550	350	550
SiN_x 5 s	0.9	0.8	0.6	0.6
RCA2+SiN_x 3 s	1.15	0.1	0.6	0.6
RCA2+SiN_x 5 s	1.4	1	0.5	0.5

measurements show agreement with Q_f $<10^{12}$ q/cm^2 and D_{it} $<10^{12}$ cm^{-2}. This can fit the low lifetime measurements provided the charge is low. The charge determined from the minimum lifetime in Figure 7.8(b) and the G-V measurements are significantly higher. It is likely that these techniques have overestimated the charge. The RCA2+SiN_x samples show a promising increase in the effective lifetime. The C-V measurements show no clear change in the D_{it}, which suggests the improvement is due to the increase in the positive charge. A high positive charge could be detrimental to a hole-selective contact, though the simulations in Chapter 4 show the effect is minimal for Q_f $<10^{12}$ q/cm^2.

7.4 Aluminium Oxide Interface Nanolayers

The passivation properties of AlO_x nanolayers on Si are investigated as single layers and RCA2+AlO_x stacks. Again, the effective lifetime, SPV, G-V and C-V measurements are used to extract the interface parameters, Q_f and D_{it}.

7.4.1 Lifetime

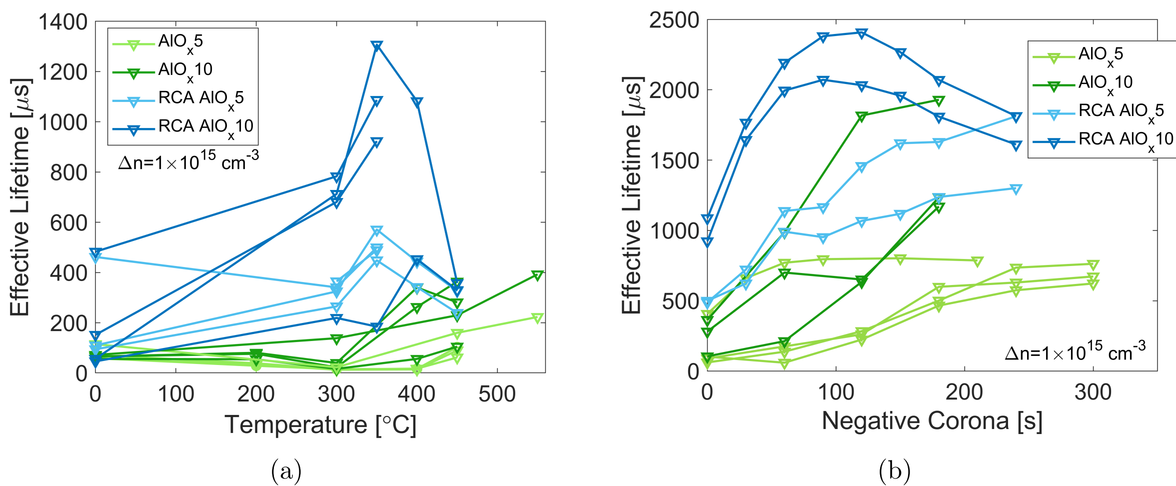
The effect of a 5 min hotplate anneal and negative corona charge on the effective lifetime of the AlO_x nanolayers is investigated. Figure 7.13(a) shows the effective lifetime as a function of the anneal temperature. The single layer AlO_x samples show a decrease in lifetime at temperatures around

300 °C followed by a sharp increase. This is likely due to the development of a negative charge, first causing depletion at the Si/AlO_x interface, then producing beneficial FEP once the charge is sufficiently high. 5 cycles of AlO_x give maximum lifetimes around 100-200 µs, while 10 cycles reached lifetimes of >400 µs. The addition of an RCA2 interlayer resulted in a further increase in lifetime with a maximum lifetime of 1.3 ms measured for RCA2+10 cycles AlO_x, corresponding to a J_0 of 128 fA/cm^2. Interestingly, the lifetime peaked at 350 °C. This may be due to competing effects of negative charge in the AlO_x but positive charge forming in the RCA2, diffusion of hydrogen away from the interface, or thermal shock when the sample is removed from the hotplate. Further analysis of the interface is required to understand this fully.

The addition of negative corona to the samples is shown in Figure 7.13(b). In all cases, the negative corona charge increases the lifetime. No minima value indicates a negative charge is present in the AlO_x nanolayer, as expected from previous literature [176]. The maximum lifetime indicates the potential lifetime that could be achieved in these samples if the FEP is optimised. Effective lifetimes of >1 ms are achieved for AlO_x single layers, with the maximum τ_{eff} of 1.9 ms corresponding to a J_0 of 130 fA/cm^2. The RCA2+AlO_x stack is exposed to corona after a 350 °C anneal as this corresponds to the maximum lifetime. A maximum lifetime of 2.4 ms is achieved for RCA2+10 cycles AlO_x, corresponding to a J_0 of 94 fA/cm^2. The RCA2+5 cycles AlO_x shows similar behaviour to the 10 cycles single layer stacks, achieving a maximum lifetime of 1.8 ms and J_0 of 146 fA/cm^2.

7.4.2 SPV

The CPD for a 5 cycles AlO_x with increasing anneal temperature is plotted in Figure 7.14. The initial values show a small, negative SPV value, and a negative CPD, larger than that of SiO_x or SiN_x. This indicates a positive charge and high D_{it} is present in the as-deposited AlO_x. The D_{it}-Q_f map for the as-deposited case is included in Appendix D and indicates a positive charge of $\sim 1\times10^{11}$ q/cm^2 and D_{it} of $\sim 1\times10^{12}$ cm^{-2}. Upon annealing, there are significant changes in the CPD. Between 300 and 450 °C the CPD values become positive and the polarity of SPV swaps



(a) (b)

Figure 7.13: Lifetime of ALD AlO_x with a hotplate anneal. Lines are a guide to the eye, with each line representing a separate sample

to a positive value. Both these effects indicate an increase in negative charge. The D_{it}-Q_f plots shown in Figure 7.15, are generated for the 450 °C anneal. To generate the high positive SPV of 0.2 V, Δn must be increased from 5×10^{13} cm^{-2} to 1×10^{17} cm^{-2} (see Appendix D), meaning a well-passivated surface allows the injection at the surface to go to 1×10^{17} cm^{-2}. A negative charge concentration $>2\times10^{12}$ cm^{-2} is required to get such SPV value. A D_{it} $<10^{12}$ cm^{-2} is expected to contribute to the large SPV value.

7.4.3 Capacitance and Conductance Measurements

A high conductivity, independent of frequency was measured, so G-V analysis could be carried out. Figure 7.16 shows the conductance-voltage measurements for 5–20 cycles ALD AlO_x as-deposited and with Al contacts. The value of conductance used to indicate the flatband voltage is varied with respect to the AlO_x thickness. The G-V curves shift to the right as the number of cycles is reduced, indicating an increase of fixed charge in the dielectric. The fitted Q_f is indicated next to each $|Q_{abs}|$ curve. There is a high negative charge in the layers, with a Q_f of 1.5×10^{13} q/cm^2 required to fit the 5 cycles AlO_x. These results are discussed further in Section 7.6.1.

Capped capacitance-voltage measurements are performed on 5 and 10 cycles ALD AlO_x with and without the additional RCA2 oxide. The AlO_x was deposited then some samples underwent hotplate anneals at 450 or 550 °C. The PECVD SiO_x capping layer was deposited and all samples were annealed at 350 °C for 5 min in air, before Al contact deposition. Figure 7.17 shows the C-V curves with the theoretical fitting and Table 7.3 gives the extracted values of Q_f and D_{it} from the fits.

There are significant changes in the C-V curves for different AlO_x stacks and processing conditions. The negative charge in the dielectric layer increases with anneal temperature and with the addition of an RCA2 layer. The RCA2+10 cycles AlO_x has the highest Q_f of -3.2×10^{12} q/cm^2 after 550 °C anneal. The single layers have a lower charge and in the case of 5 cycles AlO_x, the charge remains positive even after annealing. The Q_f measured is lower than the RCA2 or PECVD oxide, so the positive charge in the oxide capping layer may be contributing to the charge seen. If this charge is removed a negative charge $\sim$-4×10^{11} q/cm^2 is seen. There is an increase in D_{it}

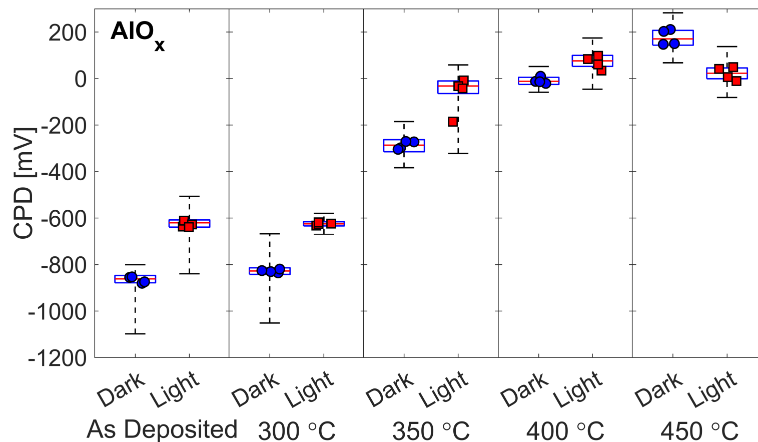


Figure 7.14: CPD of AlO_x as a function of anneal temperature in the dark and under illumination. The box plots are generated from the points on the 10×10 map, the points indicate the average CPD in each quadrant of the map.

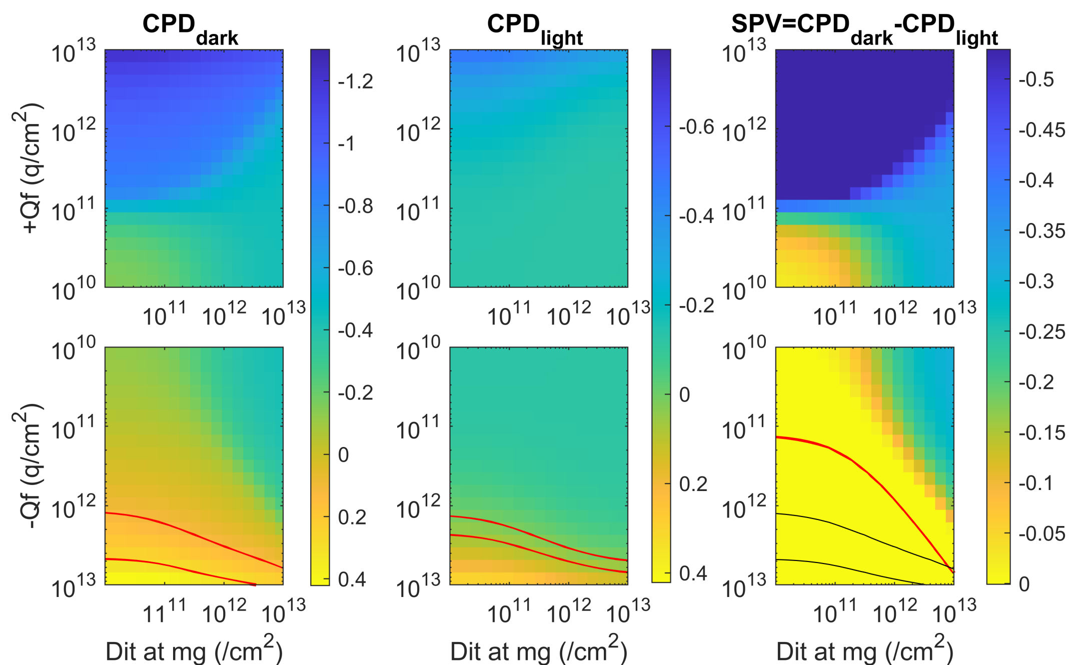


Figure 7.15: Estimated D_{it} and Q_f from SPV measurement of 5 cycles AlO_x after 450 °C anneal. Black lines show the CDP_{dark} values superimposed on the SPV graph.

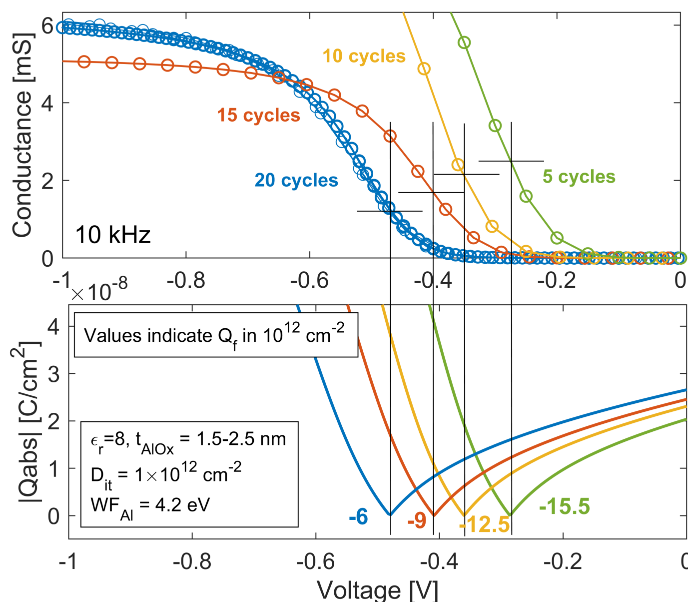


Figure 7.16: G-V of AlO_x for increasing deposition cycles. The value of conductance used to represent the onset of excessively high conductance is reduced as the thickness increases.

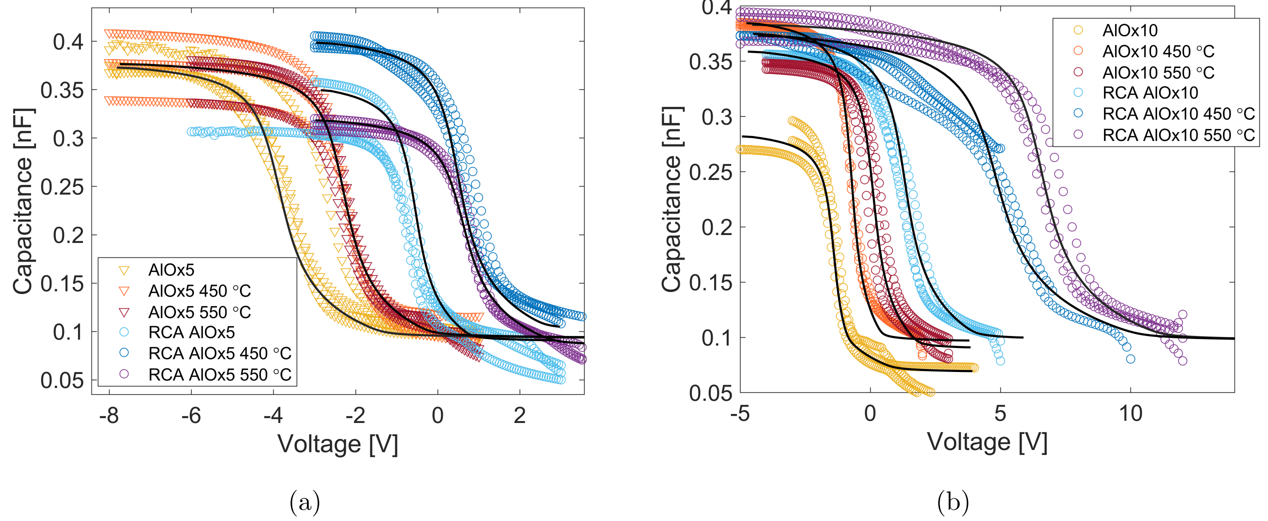


Figure 7.17: C-V measurements of AlO_x nanolayers using a PECVD SiO_x capping layer. Solid black lines give the theoretical fits.

Table 7.3: Fitted Q_f and D_{it} from C-V of AlO_x and RCA2+AlO_x stacks

Dielectric	**Q_f [$\times 10^{12}$ q/cm^2]**			**D_{it} [$\times 10^{12}$ cm^{-2}]**		
Anneal T [°C]	**350**	**450**	**550**	**350**	**450**	**550**
AlO_x 5 cycles	0.7	0.4	0.4	0.7	0.6	0.6
AlO_x 10 cycles	0.2	-0.1	-0.4	0.1	0.1	0.4
RCA2+AlO_x 5 cycles	-0.1	-0.6	-0.6	0.2	0.6	0.6
RCA2+AlO_x 10 cycles	-1	-2.7	-3.2	1	2.5	2

for the higher annealing temperatures. The improvement in effective lifetime seen in the single layers must be due to the increase in charge. The RCA+AlO_x stack has high Q_f suggesting the drop in lifetime is due to an increase in D_{it}, not any contribution from a positive charge in the RCA2 layer. The stack was annealed at 550 °C before SiO_x deposition, so hydrogen could effuse out of the interface. However, the PECVD SiO_x should resupply the interface with hydrogen and hence an increase in D_{it} would not be seen in the C-V measurements. Thermal shock is a plausible mechanism for the D_{it} increase and τ_{eff} decrease.

The higher negative charge in the RCA2 stacks could be related to the stoichiometry of the films discussed in Chapter 5, Section 5.3. The SiO_x surface condition enables a higher concentration of Al to be deposited in the initial deposition cycles. In addition, Hiller et al. [100] showed that the SiO_x interlayer is key to forming a high negative charge in ALD AlO_x. In the AlO_x single layer stacks an anneal >350 °C may allow the formation of the SiO_x interlayer and generate the charge.

7.4.4 Summary

The passivation properties of AlO_x have been studied via photoconductance decay, SPV, G-V and C-V measurements. J_0 values below 100 fA/cm^2 were achieved for the stacks with the RCA2 oxide interlayer. The additional analysis showed a clear increase in the negative charge with increasing anneal temperature. There is some inconsistency with quantifying of this negative charge, with

the SPV indicating 2–5×10^{12} and G-V giving >10^{13}. The C-V measures a slight positive charge, but this is reduced to -4×10^{11} if the PECVD SiO_x charge is compensated for. The cause of these discrepancies is discussed in Section 7.6.1.

7.5 Titanium Oxide Interface Nanolayers

TiO_x samples are prepared by collaborators at AIST with plasma (p), or thermal (t), ALD using the deposition parameters found in Table 3.3. Prior work carried out at AIST involved lifetime measurements of the TiO_x nanolayers and fabrication of full cells with a TiO_x hole selective contact. It was found that (i) tALD TiO_x has a negative charge, while pALD TiO_x has a positive charge (ii) hydrogen plasma treatment (HPT) and annealing the TiO_x layers improved the efficiency of TiO_x cells due to an increase in V_{OC} and FF [322] (iii) textured wafers had lower V_{OC} [322], and (iv) the samples were susceptible to degradation during light soaking at 1 Sun [322]. SPV and G-V analysis is used to develop a deeper understanding of the Si/TiO_x interface. The Si orientation, post-deposition treatments and UV light soaking have been shown to alter the properties of full cells, and by studying the Si/TiO_x interface the mechanisms behind these changes can be determined.

7.5.1 Lifetime

The lifetime of plasma and thermal ALD TiO_x are compared in Figure 7.18 for various post-deposition treatments. The samples were measured immediately after deposition at AIST and then remeasured upon receipt in Oxford (the samples are diced before transport, so each half is measured in Oxford, indicated by Sample 1 and Sample 2 in Figure 7.18). The measured lifetimes agree well with the initial measurements at AIST, indicating the samples have not degraded during transportation. Plasma ALD samples show poor lifetimes after all treatments, with a small improvement after the HPT and anneal treatment. The thermal ALD has significantly higher lifetimes. The 180 °C anneal improves the lifetime to over 1 ms. The HPT alone does not have an appreciable effect on the lifetime, but when combined with an anneal, effective lifetimes of several

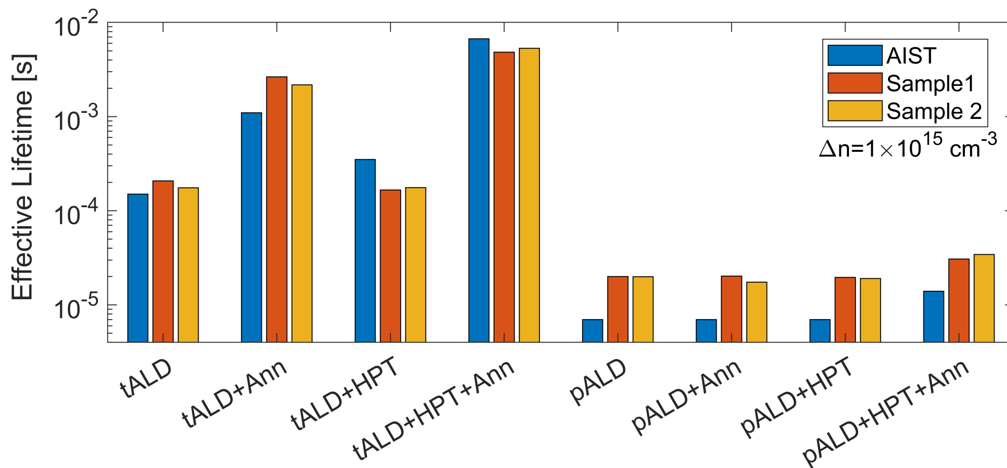


Figure 7.18: Effective Lifetime of plasma and thermal ALD TiO_x as-deposited and after various post-deposition processes. The samples underwent an anneal (Ann), a HPT or both. Measurements were carried out before (AIST) and after transportation (Sample 1 and 2).

milliseconds are measured with a J_0 of 5.5 fA/cm^2. The following sections focus on understanding the Si/TiO_x interface in more detail.

7.5.2 Plasma and Thermal ALD Titanium Oxide

Plasma and thermal ALD are compared in Figure 7.19. The plasma ALD has a large, negative SPV value, while the thermal ALD has a large positive SPV. This shows the pALD has a positive charge, while the thermal ALD has a negative one. For use in a hole selective DFPC the negative charge is highly beneficial, and thus further analysis focuses on the tALD TiO_x. Figure 7.20 shows the D_{it}-Q_f maps for the tALD TiO_x samples. The red contour lines indicate the values of CPD and SPV measured on the as-deposited sample. A negative charge is present of around 10^{11} q/cm^2 or higher. The SPV analysis is insensitive to D_{it} in this regime, so it is not possible to give a meaningful estimate of D_{it} for the TiO_x samples using this technique.

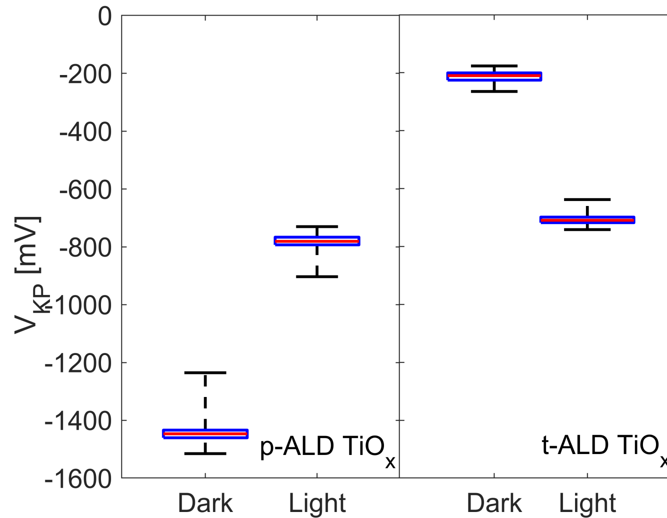


Figure 7.19: CPD measurements of plasma and thermal ALD TiO_x in the dark and under illumination.

7.5.3 Effect of Post-Deposition Processing

Figure 7.21 shows the SPV signal for TiO_x as deposited, after an anneal (180 °C in air), with HPT and with HPT+anneal. A large, positive SPV is seen in all cases. There is very little change in the SPV for the different processing conditions, with only a very slight increase in the values of CPD_{light} and SPV after post-deposition treatments. This change is minor compared to the variation across each sample, so there is limited meaningful analysis possible. As was shown in Figure 7.2(b), the conductance of a TiO_x sample is high and independent of measurement frequency. Thus, the TiO_x is suitable for analysis using the G-V technique. The measurements are taken at 10 kHz, with Al contacts. The insets of the figures indicate the fitting parameters used to determine the dielectric fixed charge. Figure 7.22 shows the conductance-voltage measurements for the as-deposited TiO_x and for samples with further annealing and HPT treatments. The sharp increase in the conductance occurs at a positive voltage, indicating a negative fixed charge in the TiO_x. The G-V curves, are

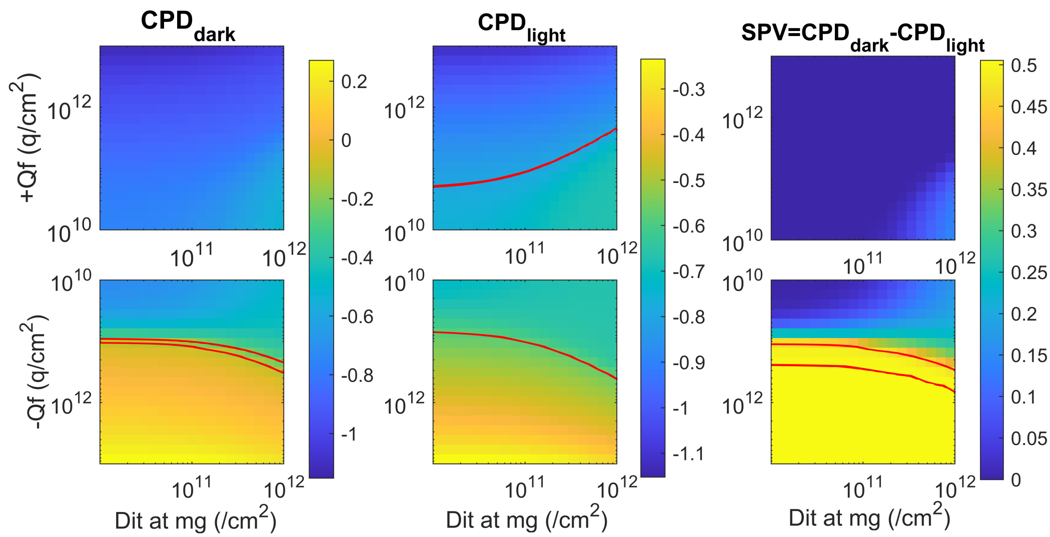


Figure 7.20: Estimated D_{it} and Q_f of tALD TiO_x from SPV.

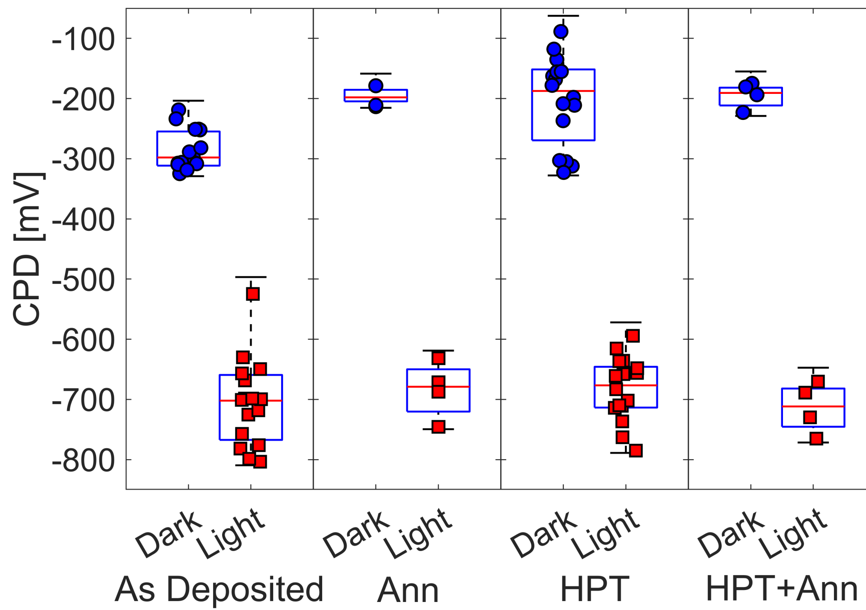


Figure 7.21: Dark and illuminated CPD measurements of thermal ALD TiO_x sample as-deposited, with an anneal, with HPT treatment and with an anneal and HPT treatment.

fitted to the minima of the $|Q_{abs}|$ at a conductance of 2 mS. All samples show a high negative charge in the 10^{12} q/cm^2 range. There is an increase in the negative charge of $\sim 10^{12}$ q/cm^2 after the additional processing. There is no significant difference between the samples with only HPT, only the anneal or both the HPT and anneal. The high negative charge agrees with the SPV results in Figure 7.21. The post-processing results in a slight increase in the SPV signal, but the technique sensitivity is insufficient to quantify the charge increase. The G-V analysis has a higher sensitivity to the dielectric fixed charge, so the changes in charge concentration during processing steps are distinguished.

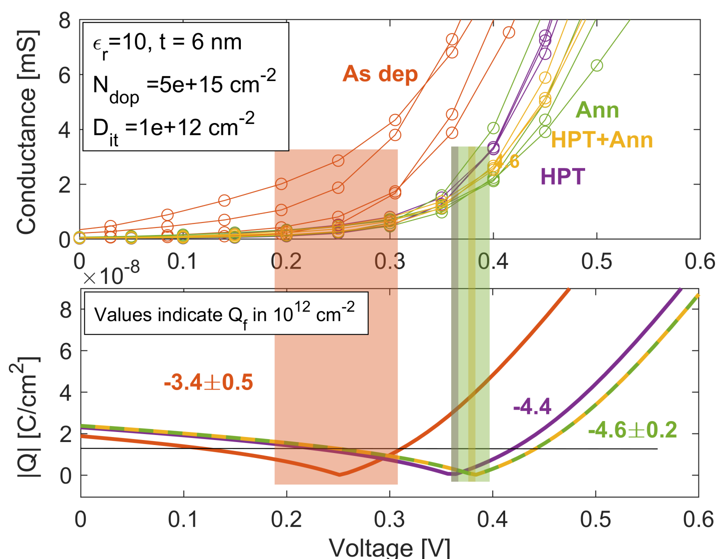


Figure 7.22: G-V analysis of a TiO_x sample as deposited, with HPT treatment, with an anneal and with HPT+anneal

7.5.4 Effect of Silicon Orientation

Full cells are fabricated with textured wafers to maximise the absorption of light. The V_{OC} of cells with TiO_x on textured wafers was significantly lower than on planar wafers [194]. Figure 7.24 compares the SPV signal from TiO_x on planar Si(100) to the TiO_x on textured and planar Si(111). There is a significant decrease in the SPV signal for both the textured and Si(111) samples, caused by an increase in the CPD_{light}. The difference in SPV for the textured and Si(111) showed the drop in V_{OC} is due to a change in the Si/TiO_x interface, not the higher surface area of textured Si. A smaller SPV signal is due to a reduction in charge or an increase in higher D_{it}. As the CPD_{dark} signal is unchanged, an increase in D_{it} is likely. This is explained by the higher atomic density of the Si(111) plane [68].

G-V analysis is used to confirm the mechanisms causing a reduction in the V_{OC} for textured wafers. Thermal evaporation of metal contacts onto textured wafers is not possible so the planar Si(111)/TiO_x samples are compared to Si(100). Figure 7.23 indicates a small reduction on the Si(111) surface compared to a Si(100) planar surface. The shift in the G-V curve is not explained by a higher D_{it}, as an increase in D_{it} would shift the curve to a higher voltage. Thus, the combination of SPV and G-V indicated the lower V_{OC} on textures Si is caused by a combination of lower Q_f and higher D_{it}.

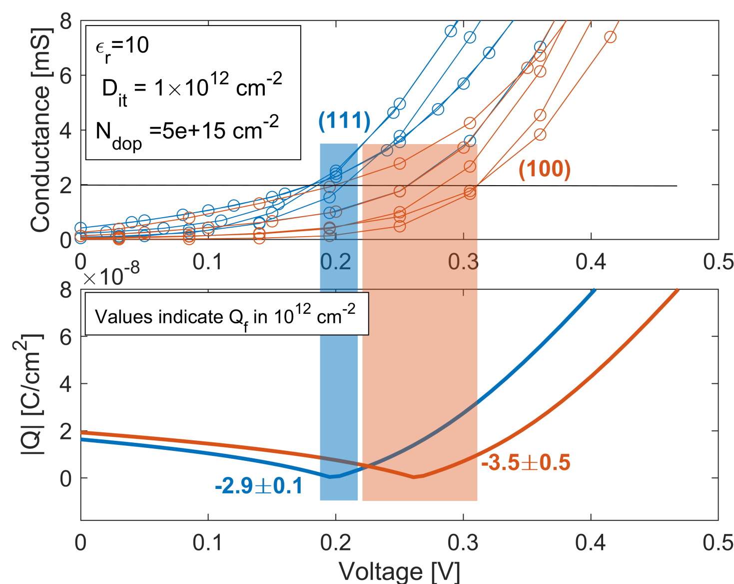


Figure 7.23: G-V analysis of TiO_x deposited on (100) and (111) wafers

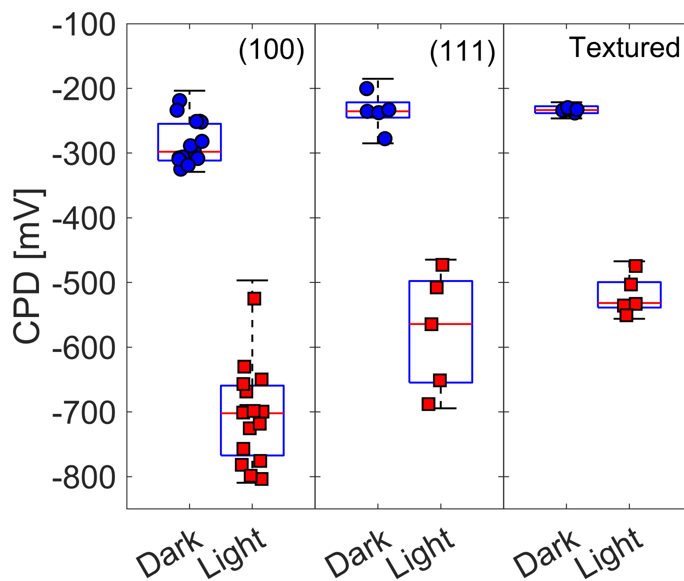


Figure 7.24: Dark and illuminated CPD measurements of thermal TiO_x deposited on (100) silicon, (111) silicon and textured silicon.

7.5.5 Effect of UV degradation

A drop in the performance of full cells is seen after light soaking for 100 hr under 1-Sun illumination. Light-induced degradation is carried out using UV lightbox at a total optical irradiance of ∼5 mW/cm^2 to observe the change in the SPV signal during the degradation process. Figure 7.25 shows the evolution of SPV signal during sample processing. TiO_x on (100) Si with an HPT anneal is used. During the first UV ageing treatment the sample underwent 100 hr of UV ageing. The degradation showed a significant drop in the CPD_{light} and SPV values, which indicated a decrease in the negative charge in the sample. The UV box has a higher intensity, so most of the degradation

occurred before the first measurement after 2 hrs. The sample was recovered by a 2 hr anneal at 180 °C, then exposed to UV for shorter time intervals. The SPV signal after the anneal matches that of the sample before UV exposure, indicating the sample is fully recovered. The shorter time intervals allow observation of the degradation timescale. It is seen that the effect of UV degradation is observed after just 5 mins of exposure, reducing CPD_{dark} by 150 mV and CPD_{light} by 300 mV. The measurements are relatively stable after this time, with a further reduction of CPD_{dark} of 150 mV and no change in CPD_{light} after 1 hr of UV exposure.

For the G-V analysis, an HPT sample underwent 100 hrs at 1 Sun. This is compared to the HPT and the as-deposited TiO_x in Figure 7.26. A reduction in the negative charge at the interface is seen after the illumination. The reduction in charge returns the charge in the TiO_x to the value of the as-deposited state. As with the change in Si orientation, if the light soaking caused an increase in D_{it}, the $|Q_{abs}|$ would shift to the right. Therefore the degradation seen after illumination is due to the reduction in charge.

7.5.6 Summary

The TiO_x samples were analysed and compared to the results from AIST. Lifetime measurements showed close agreement with the results from AIST, showing the samples were not degraded during shipping. The tALD is confirmed to have a significant negative charge, beneficial for hole-selective contacts. The SPV and G-V provided additional analysis of the TiO_x films. the effect of post-deposition processing, Si wafer orientation and UV degradation were studied. The changes in the performance measured in full cells are related to changes in the D_{it} and Q_f at the Si/TiO_x interface, with good agreement between the techniques. This analysis is crucial to finding the optimum conditions and structures for the TiO_x contacts to be implemented into efficient cells.

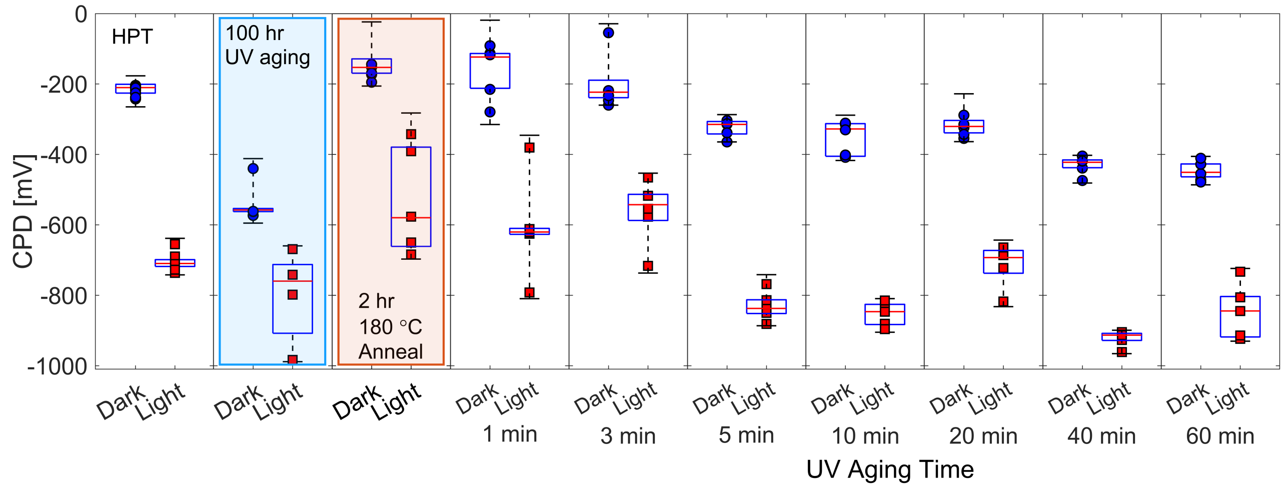


Figure 7.25: Dark and illuminated measurements of UV degraded of TiO_x with HPT treatment. The sample is initially degraded with 100 hr of UV, then it is recovered with a 2 hr anneal at 180 °C, before a second degradation.

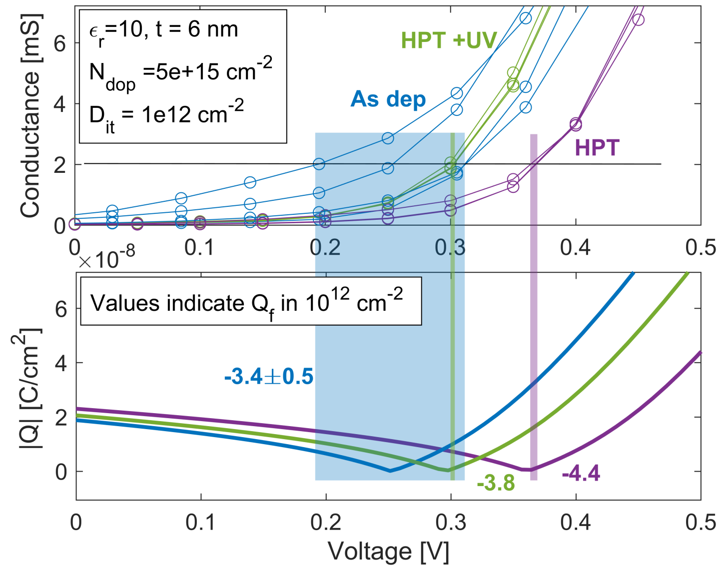


Figure 7.26: G-V analysis of TiO_x as deposited, after HPT and after 100 hr light soaking

7.6 Discussion

7.6.1 Comparison of Techniques

The issues with determining D_{it} and Q_f in nanolayer dielectrics are discussed in Sections 2.10 and 7.1. SPV analysis can be carried out for the thin dielectrics as the probe is not directly contacted, and hence no leakage current can occur. SPV can provide some information on the D_{it} and Q_f at the Si/dielectric interface when combined with analytical calculations. Though the influence of D_{it} and Q_f are linked, limiting the precision of the technique. Gad et al. [130] used SPV to study the D_{it} of various thin SiO_x layers. They used a biased SPV measurement to obtain the D_{it} as a function of energy to find the D_{it} over the Si band gap [323], [324]. It is unclear how the effect of interface charge on the photovoltage measurement is negated, but it may be that it is assumed to take a low, constant value for the SiO_x studied.

Two novel techniques are developed to obtain more information about the Si/dielectric interfaces for highly conductive nanolayers. G-V measurements used the highly conductive nature of the films to determine the position of V_{FB} and then fitted this to the minima in the $|Q_{abs}|$. This enabled a detailed study of the charge in the TiO_x films under various processing regimes. The technique was less effective in the SiN_x and AlO_x nanolayers. both gave unrealistically high values of Q_f. It is likely the films were not sufficiently conductive to use the technique, causing an overestimation of V_{FB}. The extremely thin nature of the films means a large charge is required to shift the $|Q_{abs}|$ curve on the voltage axis. This means a small error in the voltage value taken as the onset of high conductivity leads to a large error in the Q_f. This is in addition to known dipole effects created at metal interfaces [325]. The technique best compares the charge concentration during different processing treatments, where the thickness remains constant. The study on TiO_x highlights the ability of the G-V analysis to resolve differences in the charge concentration for different processing conditions. The small influence of D_{it} on the position of Q_f can also lead to some errors. For a negative charge on an n-type Si wafer, an increase in D_{it} shifts the $|Q_{abs}|$ curve in the direction

of a higher charge. The G-V can be compared to the lifetime or V_{OC} to determine whether the passivation quality increases or decreases. An increase in passivation could be attributed to an increased FEP, i.e. a higher charge. Poorer passivation would suggest the shift is caused by lower chemical passivation i.e. a higher D_{it}.

The capped C-V analysis has some advantages over the G-V analysis. The PECVD SiO_x is shown to provide a sufficient insulating layer to enable good-quality C-V measurements. The fitting of these measurements is well understood and the D_{it} and Q_f affect the measurement independently, enabling the extraction of both parameters to high precision. The limitations of the technique are the additional processing and the SiO_x layer, which could influence the Si/dielectric interface. The high concentration of hydrogen in the PECVD SiO_x can provide additional chemical passivation of the interface. Additional hydrogen is not necessarily a problem, as any full contact structure will undergo a hydrogenation step. In fact, hydrogenation of the interfaces could be intentionally added with optimisation of the SiO_x anneal, this would give an idea of the minimum D_{it} possible. The results from the capped C-V show good agreement with the estimated values of D_{it} and Q_f from SPV and the overall passivation quality from the lifetime, indicating the technique is valid, with D_{it} and Q_f obtained to high accuracy and precision.

The techniques discussed here provide methods for extracting D_{it} and Q_f from Si/dielectric interfaces with high leakage currents. The limitation of both techniques is that they cannot characterise the dielectric interface in full poly-Si contacts, after the poly-Si deposition and high-temperature anneal. The high-temperature anneal can significantly alter the dielectric layer's interface properties. It has been shown that the anneal can reduce the D_{it} in some SiO_x contacts, but in others, it causes a break-up of the oxide and results in a significant increase in the D_{it} [145], [216]. In AlO_x and SiN_x contacts studied here, it has been shown that the charge in the dielectric can vary significantly with anneals up to 550 °C. The anneals and in-diffusion of boron can alter the FEP in the complete poly-Si contact structure, intended for the full exploitation of these nanolayers.

7.6.2 Comparison of Nanolayer Dielectric Interfaces

Extensive characterisation of the nanolayer dielectrics has determined the charge and interface state density for each of the dielectrics. Figure 7.27 compares the effective lifetime, SPV and C-V measurements for the SiO_x, SiN_x, and AlO_x. The TiO_x is not included here as it was deposited on different Si wafers and hence a direct comparison cannot be made. Figure 7.27(a) shows the effective lifetime as a function of injection density. The highest lifetimes for each structure are compared. It is seen that the AlO_x lifetime is far superior to the SiN_x or SiO_x fabricated in this work. The low lifetime of SiO_x is explained by the low charge and the lack of any hydrogenation process. Hydrogenation is crucial for lowering the D_{it} and obtaining high lifetimes in nanolayer SiO_x [119], [130]. The SiN_x lifetime is also low, though an improvement is seen with the addition of an RCA2 interlayer. The non-stoichiometry, discussed in Chapter 5, may contribute to the low lifetime. A low J_0 of 40 fA/cm^2 has been reported for an LPCVD SiN_x nanolayer [177], so with the optimised processing conditions, there is scope to improve the passivation quality of the SiN_x. 10 cycles AlO_x achieved the highest lifetimes. The highest lifetime of single layer AlO_x was 1.9 ms, with the addition of negative corona charge, corresponding to a J_0 of 130 fA/cm^2. The RCA2+AlO_x stack achieved a lifetime of 1.3 ms from annealing and a lifetime of 2.4 ms with negative corona,

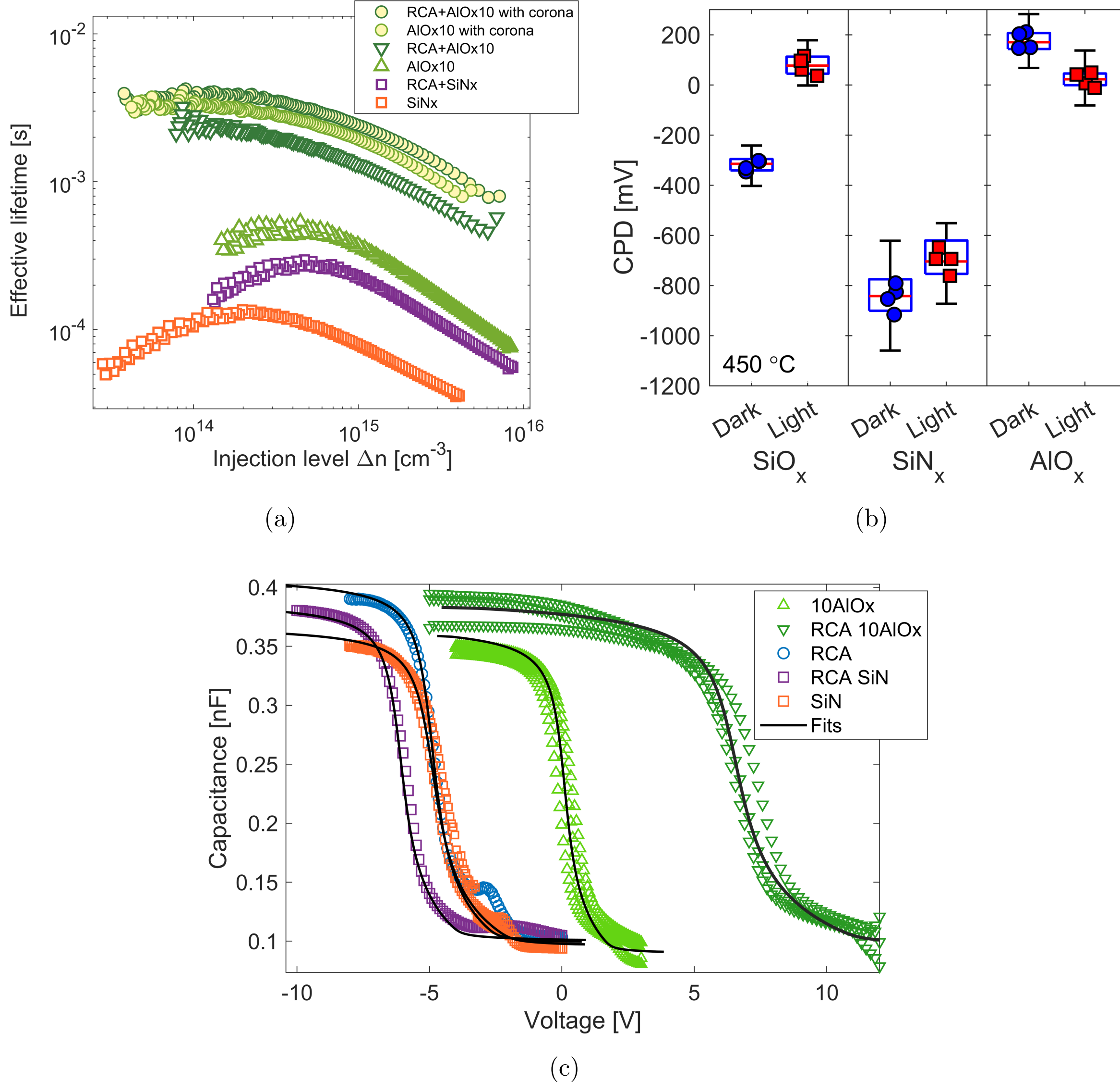


Figure 7.27: Comparison of a) τ_{eff} on N30-60 wafers, b) SPV on P1-10 wafers and c) capped CV measurements on P1-10 wafers and after 350 °C anneal for Si/dielectric interfaces

this gives J_0 of 130 and 94 fA/cm^2, respectively. Single AlO_x nanolayers have reached SRV of 23 cm/s with 5 cycles [185] and J_0 of 40 fA/cm^2 for AlO_x deposited on SiO_x [207]. The passivation quality of the AlO_x nanolayers fabricated here is approaching the highest reported values in the literature for nanolayer stacks. The layers have not had any hydrogenation, which could boost the lifetime of all samples significantly [94], [205], [317]. The nanolayers are hydrogenated after poly-Si deposition in Chapter 8 and discussed to work on AlO_x and SiN_x poly-Si contacts, as well as the state of the art SiO_x/poly-Si contacts.

Figures 7.27(b) and 7.27(c) compare the SPV and capped C-V measurements for SiO_x, SiN_x, and AlO_x. The results show good agreement, with the SiO_x having a low positive charge, the SiN_x having a slightly larger positive charge, and the AlO_x having a significant negative charge. The benefit of a high negative charge in passivating contact structures was discussed in detail in Chapter

4. The AlO_x showed an increase in charge with increasing annealing temperature and with the addition of a SiO_x interlayer. This was also found in other work on thin films [176], [185]. Charges of 3×10^{12}–7×10^{12} q/cm^2 in <2 nm AlO_x have been measure using corona-based methods [176], [185], [211]. Corona charge can be neutralised by leakage through the nanolayers so the charge measured represents an upper-limit to Q_f. The capped C-V and G-V methods both use an applied bias, so do not suffer from the variability as a result of this charge.

The D_{it} calculated with C-V showed an increase, or no significant decrease, with increased annealing temperature. The D_{it} typically decreases at annealing temperatures <600 °C [178], [185]. Thermal stresses during cooling may lead to an increased D_{it}, so a slower cooling rate could reduce these stresses and lower D_{it}. For the RCA2+AlO_x stacks, if the low D_{it} can be maintained and combined with the high charge, further improvements in the lifetime could be achieved. The SPV analysis was insensitive to D_{it} in the regimes so could not provide additional information on the D_{it} changes with temperature.

7.7 Summary

The passivation quality of the nanolayers has been studied in detail. Due to the difficulties with measuring the interface properties of nanolayer dielectrics using conventional techniques, two novel techniques were developed to analyse Si/dielectric interfaces. The G-V and capped C-V measurements were carried out on various dielectric passivation layers. The trends in D_{it} and Q_f were consistent across the techniques.

The passivation quality of SiO_x, SiN_x, and AlO_x were compared. The AlO_x achieved the best passivation, partly due to a high concentration of negative charge. J_0 of <100 fA/cm^2. The SiN_x films have not achieved high lifetimes, but further analysis showed a moderate D_{it} $\sim10^{12}$ cm^{-2}. Other work has obtained a low J_0 of 40 fA/cm^2 for SiN_x nanolayers, so with optimised processing an improvement in the passivation of SiN_x is expected. The lifetime of the SiO_x was low, but it is known that thermal SiO_x can achieve some of the highest lifetimes in literature via subsequent high-temperature processing. The passivation of all the nanolayers may be affected after poly-Si deposition, annealing and hydrogenation. The anneal at temperatures >800 °C results in the re-ordering of bonds at the Si/dielectric interface. This can either reduce the D_{it} or cause the break-up of the nanolayers, resulting in highly recombinative regions where the Si directly contacts the poly-Si. The anneal also causes an in-diffusion of boron, which gives a doping profile across the interface and can add FEP. The hydrogenation step can reduce the D_{it}, improving the chemical passivation. The device implementation of the nanolayers is carried out in Chapter 8.

Chapter 8

Poly-Si on Oxide and Nitride Nanolayer Contacts

Using the knowledge gained from the previous chapters on nanolayers and Si/nanolayer interfaces, poly-Si contacts are fabricated incorporating the SiN_x and AlO_x layers synthesised. The poly-Si deposition and subsequent processing steps are carried out by collaborators at the École Polytechnique Fédérale de Lausanne (EPFL), as the required deposition tools are not available in Oxford. EPFL has an established process for obtaining high-quality SiO_x/p^+poly-Si contacts. Passivating contacts with iVoc of 720 mV, and contact resistivity of 10 mΩ·cm^2 have been fabricated in EPFL [318], [326]. Slight differences between each batch of samples can occur, therefore the novel dielectrics are processed along with a UV-O_3 SiO_x that acts as a control. The process flow for each batch of samples is shown in Figure 8.1. Details of each of these steps can be found in Chapter 3. The poly-Si anneal is carried out in an Ar atmosphere with a heating rate of 10 °C/min to the set point, immediately followed by a 2 °C/min cooling. The PECVD SiN_x layer in Batch 2 provides hydrogenation of the Si/dielectric interfaces and is removed for ECV and J-V measurements.

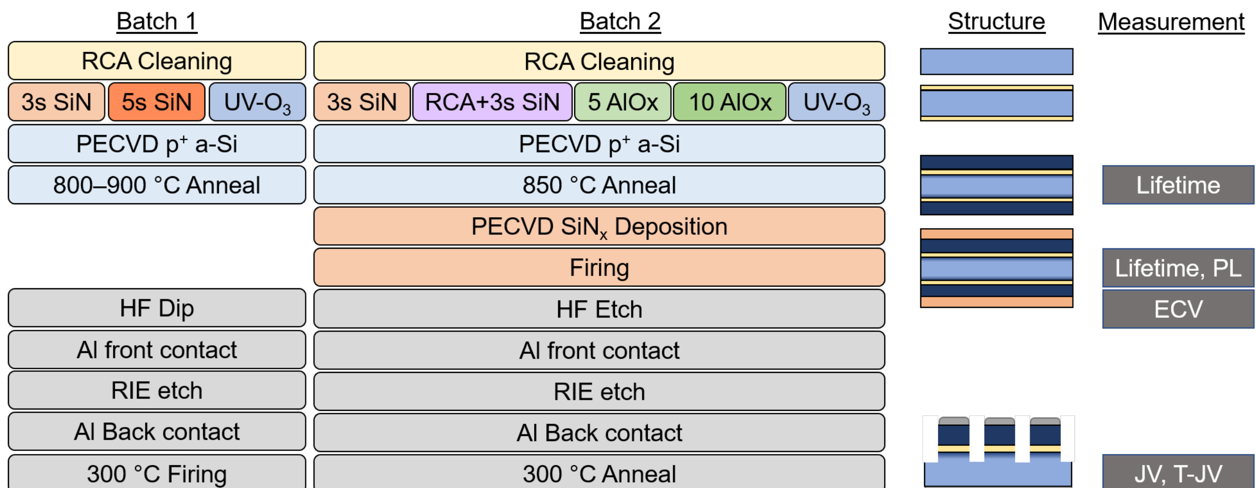


Figure 8.1: Process flow for poly-Si contacts.

8.1 Resistivity of Poly-Si Contacts

The J-V measurements are carried out via a straight-through J-V measurement as described in Section 3.4. The structure is formed via the processing steps in Figure 8.1 with the final structure shown in Figure 3.3(b). The contact resistivity (ρ_c) is obtained by removing the theoretical spreading resistance from the total resistance. The RIE etch isolates the contact stacks to prevent lateral conduction through the poly-Si or in-diffused region. The HF dip before front contact deposition and the 300 °C firing of the contacts are crucial to ensure the resistivity at the poly-Si/metal contact is minimised. The effect of these steps is explored in Appendix E.

8.1.1 Effect of Anneal Temperature

The first batch of samples studies the effect of the annealing temperature. The poly-Si anneal temperature is varied between 800–900 °C in steps of 50 °C. The resistivity of 3 s SiN_x, 5 s SiN_x and UV-O_3 control samples are shown in Figure 8.2. An optimum anneal temperature of 850 °C is found for all dielectrics. The SiN_x ρ_c is equal to, or slightly lower than the SiO_x control sample with ρ_c of 50 mΩ·cm^2. The 900 °C anneal was expected to produce a lower contact resistivity with a higher N_{pin} forming in the dielectric. Incomplete removal of the native oxide during the HF dip could cause an increase in ρ_c, however, the increase is seen across all dielectrics, so this is unlikely. The Ar atmosphere for the poly-Si anneal could have a low concentration of oxygen that diffuses to the nanolayer dielectric, causing a thickening.

Temperature-dependent J-V (T-JV) measurements are performed to study the conduction mechanisms in the samples. Figure 8.3 shows the temperature dependence for the 3 s SiN_x poly-Si samples at each annealing temperature. The parameters used for fitting are shown in the insets next to the relevant curve. ϕ_b is zero in all cases as the semiconductor-insulator-semiconductor (SIS) contact does not form a Schottky barrier. At 800 °C the resistivity increases with decreasing temperature and is fitted with no influence from pinholes. The samples annealed at 850 °C and

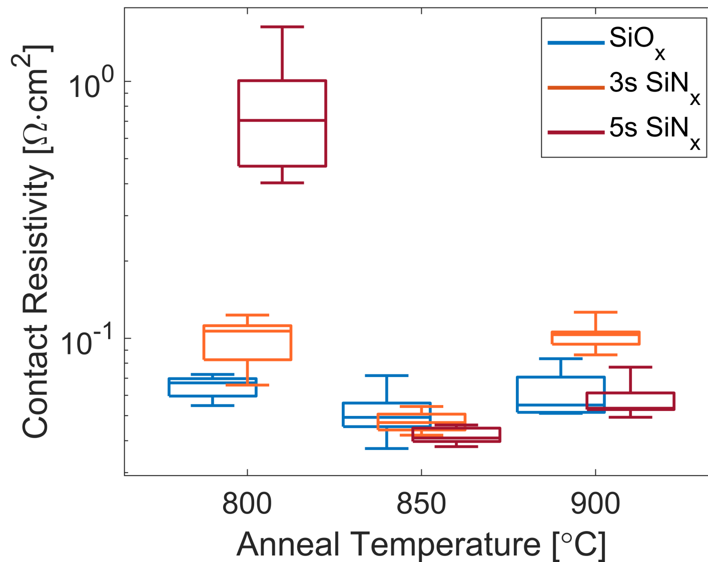


Figure 8.2: Contact resistivity of Dielectric/poly-Si structures for poly-Si anneal temperature between 800–900 °C.

900 °C show the opposite trend, with a decrease in resistivity at low temperatures. The theoretical fits show some thickness reduction in the SiN_x film and a high density of pinholes is formed, showing the structure of the SiN_x nanolayer changes at temperatures ≥850 °C. The 900 °C shows a slightly higher resistivity, which fits with Figure 8.2. The fit suggests the increase in resistivity is due to a reduction of pinholes, though the mechanism for this is unclear.

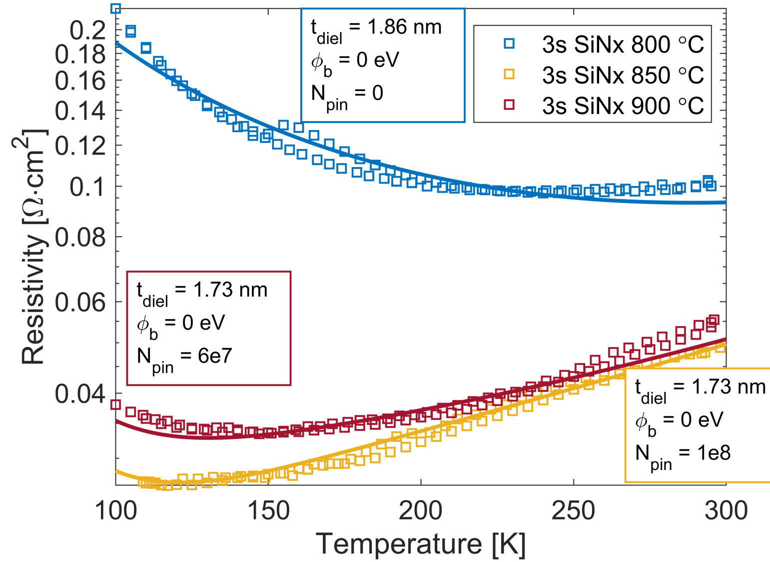
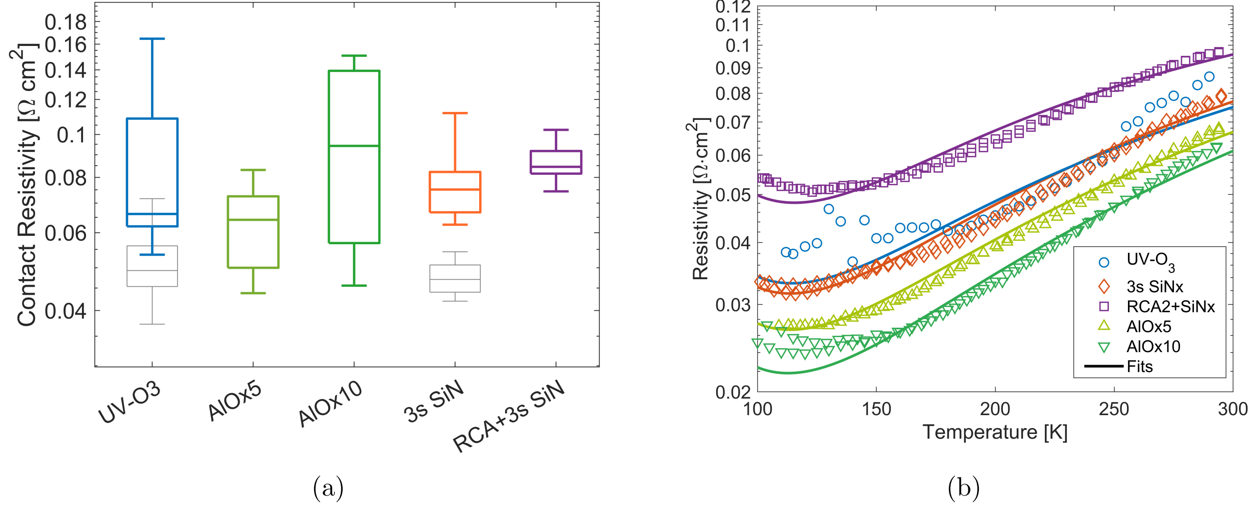


Figure 8.3: Temperature dependent Contact resistivity of 3 s SiN_x/poly-Si structures for poly-Si anneal temperature between 800–900 °C.

8.1.2 Comparison of Dielectrics

A second batch of poly-Si samples was fabricated. This batch included 5 cycles and 10 cycles AlO_x and an RCA/3 s SiN_x stack. All samples were annealed at the optimum anneal temperature of 850 °C. Figure 8.4(a) compares the contact resistivity of all dielectrics. The UV-O3 oxide and SiN_x are compared to the resistivity of the first batch. An increase in the resistivity is observed compared to Batch 1, but median ρ_c remains below 100 mΩ·cm^2 for all dielectrics. There is also greater variation in the resistivity for Batch 2. The reason for this is expected to be due to the SiN_x deposition and removal before the J-V measurements (Figure 8.1). Any contamination on the sample surface prevents the complete removal of native oxide in these regions, which causes poorer contact. The contact resistivity is lowest for the 5 cycles of AlO_x with a mean value of 60 mΩ·cm^2. The mean contact resistivity for 10 cycles AlO_x is 100 mΩ·cm^2, though some contacts measure a resistivity as low as the 5 cycles. The 3 s SiN_x samples have a contact resistivity of 80 mΩ·cm^2. The addition of an RCA2 oxide results in a 10 mΩ·cm^2 increase in ρ_c, but it remains below the 100 mΩ·cm^2 benchmark.

Temperature-dependent J-V is again used to determine the dominant conduction mechanisms through the dielectric layers. Figure 8.4(b) shows the temperature dependence of the resistivity for each dielectric with the fitting parameters given in Table 8.1. In all cases, there is a significant contribution from pinholes. The pinhole density is 10^8 cm^{-2} for the single-layer dielectrics. N_{pin} for the 3 s SiN_x layer matches Batch 1 (Figure 8.3), which fits with the ρ_c increase in Batch 2



(a) (b)

Figure 8.4: a) Contact resistivity of Dielectric/poly-Si structures. The grey boxplots show ρ_c for UV-O_3 SiO_x and 3 s SiN_x from Batch 1. b) Temperature-dependent Contact resistivity of Dielectric/poly-Si structures

being caused by a poor quality poly-Si/metal contact. The RCA/SiN_x stack has a lower density of pinholes of 3×10^7 cm^{-2}. Pinhole densities of this magnitude are likely to reduce the passivation quality of the contacts since the area fraction of the direct Si/poly-Si interfaces is high [215].

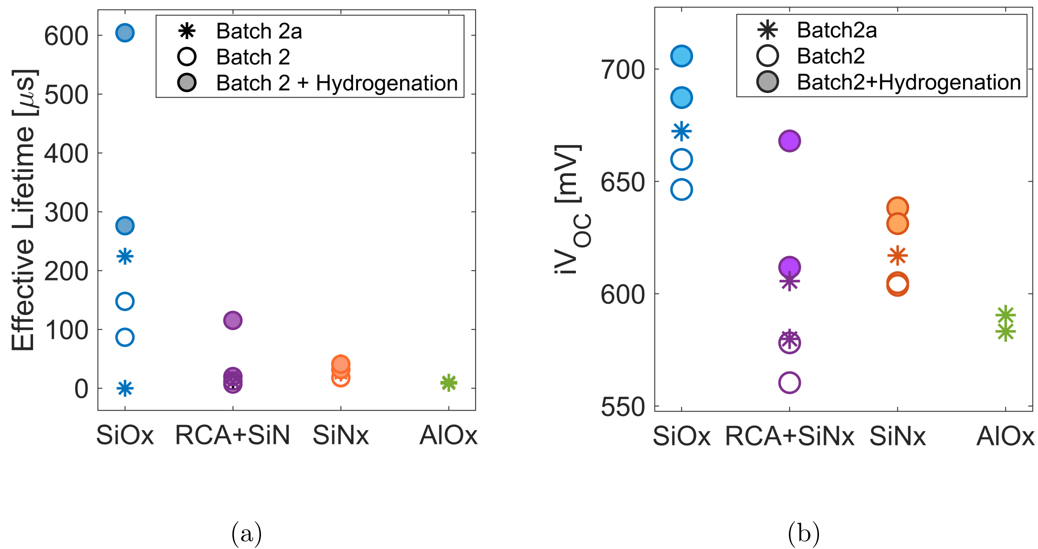
Table 8.1: Fitted t_{diel}, ϕ_b and N_{pin} for poly-Si contact structures

Dielectric	t_{diel} **[nm]**	ϕ_b **[eV]**	N_{pin} $\times10^8$ [cm^{-2}]
UV-O_3 SiO_x	1.2	0	1
3 s SiN_x	1.9	0	1
RCA2+3 s SiN_x	1.92	0	0.6
5 cycles AlO_x	1.32	0	1.4
10 cycles AlO_x	1.32	0	2

8.2 Passivation of Poly-Si Structures

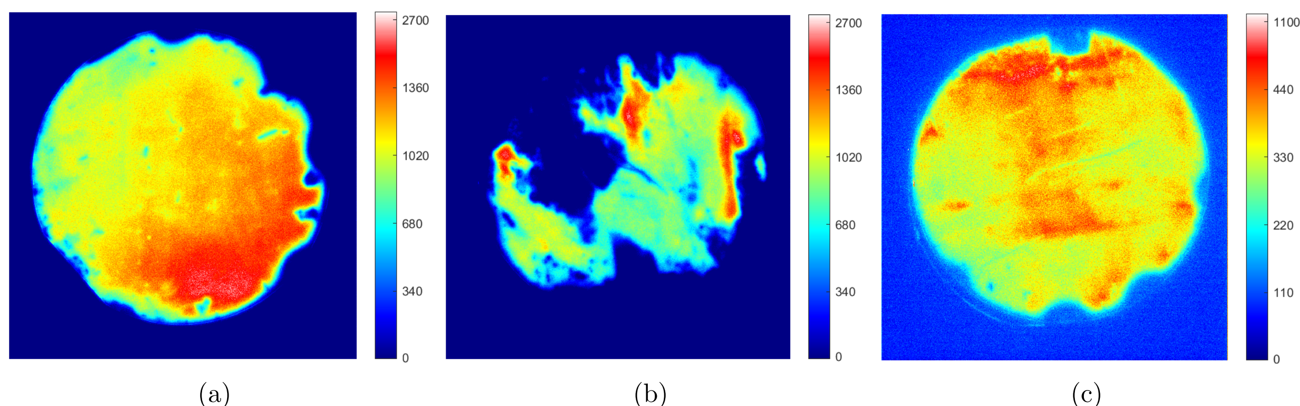
The passivation quality of the poly-Si contacts is measured by collaborators at EPFL. The effective lifetime is measured after the high-temperature anneal and after hydrogenation. Figure 8.5(a) shows the effective lifetime for Batch 2. The iV_{OC} at 1-sun is extracted from the effective lifetime and shown in Figure 8.5(b). The UV-O_3 SiO_x has the highest lifetime before and after the hydrogenation. The RCA2+SiN_x has the lowest lifetime after the poly-Si anneal, but a large improvement is measured with hydrogenation. All dielectrics show a lower iV_{OC} compared to Batch 2a, which was measured after the anneal but not hydrogenated. This indicates some variation in the poly-Si process between batches. Thus, the comparison to the UV-O_3 control is a key metric for the passivation quality of the AlO_x and SiN_x films. The lifetime curves from the hydrogenated SiO_x and best RCA2+SiN_x samples were analysed to extract the surface recombination current [239]. The fitted curves are included in Appendix D. J_0 values of 43 fA/cm^2 and 98 fA/cm^2 were obtained for the two SiO_x samples and 140 fA/cm^2 for the best RCA+SiN_x stack.

Photo-luminescence (PL) images determine the uniformity of passivation in a sample. PL uses a laser to generate electron-hole pairs in the sample. Radiative recombination of the electron-hole pairs is measured in a photodetector, with a high signal intensity indicating areas of good passivation. The PL images in Figure 8.6 were taken by collaborators at EPFL. Further details on the technique are given in Appendix B. Figure 8.6 compares SiN_x and RCA+SiN_x to the UV-O_3 SiO_x. The SiO_x and SiN_x have similar levels of passivation uniformity, though the overall signal in the SiN_x is low (note the adjusted scale bar in Figure 8.6(c)). The slight non-uniformity across the samples indicates there is some spatial variation in the quality of poly-Si deposition. The RCA+SiN_x sample exhibits considerable non-uniformity, leaving large areas unpassivated. The areas with the best passivation match the best that of the SiO_x reference. The in-homogeneity is likely caused by handling during the RCA2 and PECVD deposition and damage during transportation. If the sample processing is improved the lifetime of the RCA+SiN_x could be significantly increased.



(a) (b)

Figure 8.5: a) τ_{eff} and b) iV_{OC} of the dielectric/p$^+$poly-Si structures. Batch 2a samples were measured after the high-temperature anneal but were not hydrogenated.



(a) (b) (c)

Figure 8.6: PL images of 4” wafers with poly-Si structures after hydrogenation. a) UV-O_3 SiO_x, b) RCA+SiN_x and c) SiN_x

8.3 Boron In-diffusion in Poly-Si structures

The high temperature anneal after deposition of the p^+poly-Si causes in-diffusion of boron across the dielectric and into the Si wafer. As was shown in Chapter 4, the doping profile can have a significant influence on both the contact resistivity and recombination at the Si/dielectric interface. The dielectric, anneal time, and temperature will all influence the shape of the doping profile. The SiO_x boron profile is discussed in Section 2.9, where it is noted that a deep diffusion of boron is detrimental to the contact passivation. Electrochemical Capacitance Voltage (ECV) is a technique to measure the doping concentration as a function of depth. Collaborators at EPFL performed ECV on the poly-Si contact structures. A description of the methodology can be found in Appendix B, and the active boron concentration as a function of depth is shown in Figure 8.7. The SiN_x and AlO_x diffusion profiles are compared to the SiO_x. A measurement of SiO_x and SiN_x from Batch 1 gives good agreement. The SiN_x single layer and RCA+SiN_x stack both show boron blocking. The AlO_x samples behave similar to the SiO_x layer, with no appreciable difference in boron diffusion. Lu et al. [179] also found a high diffusivity of boron across AlO_x nanolayers.

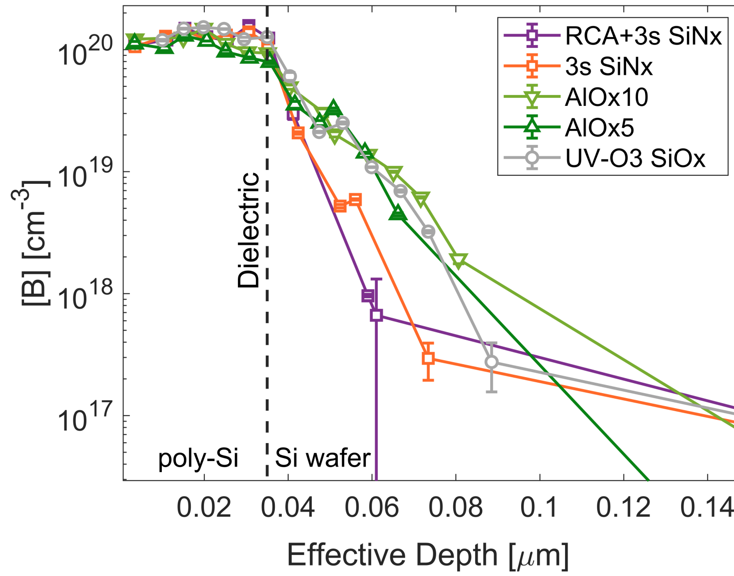


Figure 8.7: Active boron concentration as a function of depth for the dielectric/poly-Si structures.

8.4 Discussion

PECVD SiN_x and ALD AlO_x nanolayers have been incorporated into a p^+ poly-Si contact structure. A contact resistivity of 50 mΩ·cm^2 was obtained for the single layer and 90 mΩ·cm^2 was measured for the RCA+SiN_x stack. It is likely that a lower ρ_c could be obtained in the RCA stack if the contacts were deposited without the addition and removal of the SiN_x hydrogenation layer. These values are amongst the lowest reported on hole-selective SiN_x layers [4], [170], [187] and crucially below the target of 100 mΩ·cm^2. The AlO_x layers also measured low ρ_c <100 mΩ·cm^2. As with the RCA+SiN_x stack, it is likely these films suffer from a slight ρ_c increase due to contamination on the surface, preventing the complete native oxide removal prior to contact formation. Reichel [170] and Kaur [317] both reported ρ_c of >200 mΩ·cm^2 for ALD AlO_x contacts, though Reichel et al. measured a value of 70 mΩ·cm^2 for an SiO_x/AlO_x stack, comparable to the results presented here.

The T-JV measurements indicate a high density of pinholes in all the dielectrics after poly-Si deposition and annealing. The pinholes contributed to the low contact resistivity, however, the simulations in Chapter 4 showed that pinholes are not necessary for the SiN_x and AlO_x contacts to achieve low ρ_c. Indeed, in Chapter 6 the T-JV measurements confirmed that the nanolayers can form low-resistivity tunnelling contacts. This is believed to be the first report of the conduction mechanisms through SiN_x or AlO_x poly-Si contacts, so it is unknown if high pinhole densities were present in the prior work. The poly-Si deposition and annealing process used was developed for optimal SiO_x/poly-Si contacts. A poly-Si recipe tuned for the SiN_x or AlO_x could enable the formation of low-resistivity contacts with a reduced number of pinholes, which may improve the passivation of the films.

An iV_{OC} of 670 mV has been achieved in the RCA+3 s SiN_x stacks, which corresponded to a J_0 of 140 fA/cm^2. Feldmann [129] obtained a similar iV_{OC} of 675 mV for a SiO_x layer exposed to nitrogen plasma, and Reichel [170] reached 690 mV for the SiO_x/SiN_x stack. There were clear issues with the processing highlighted by PL images. The regions with the highest passivation

were comparable to the UV-O_3 control, indicating that, with better control in sample handling a significant improvement in the lifetime of the RCA/SiN_x stacks could be achieved.

The AlO_x nanolayers measured high lifetimes in Chapter 7, but the same level of passivation is not seen in the poly-Si contacts. The low lifetime could be caused by the break-up of the AlO_x during the high-temperature poly-Si process, or a reduction in the AlO_x negative Q_f after these processes. The break-up of the AlO_x film would also contribute to the deep diffusion seen in the ECV measurements. Kaur et al. [178] found that, for AlO_x contacts, annealing the poly-Si at lower temperatures of 450 °C gave superior passivation quality compared to an 800 °C anneal. Kaur measured J_0 of 15 fA/cm^2 for the low-temperature anneal, while a minimum J_0 of 50 fA/cm^2 was seen for an 800 °C anneal. Reichel [170] measured an iV_{OC} of 695 mV with the presence of an SiO_x interlayer, a gain of 60 mV compared to a single AlO_x layer after the same processing. The results in Chapter 7 show the RCA2+AlO_x stack can achieve a higher charge, and the compositional analysis in Chapter 5 indicated an increase in Al concentration with the SiO_x interlayer, which may improve the stability of the AlO_x during the high-temperature processing steps. The RCA2 interlayer, combined with optimised poly-Si processing to reduce the pinhole density, could enable the retention of the high-quality Si/AlO_x interface in poly-Si structures.

The presence of any fixed charge at the Si/dielectric interface of poly-Si contacts could not be determined using the techniques set out in Chapter 7. G-V is not possible due to the in-diffusion of boron during the poly-Si anneal. The in-diffusion forms a region of high conductivity at the Si/dielectric interface, as well as the already conductive dielectric/poly-Si interface. This means there is always a high concentration of carriers at both dielectric/silicon interfaces and a high conductivity is measured at all voltages. An example G-V curve is shown in Appendix E. The adapted C-V method is also not applicable, as the Si-dielectric layer is buried under the conductive poly-Si. Potential methods to measure the fixed charge in poly-Si structures are discussed in the Further Work in Chapter 9.

Combining the ρ_c and J_0 can be used to calculate the Selectivity of the contacts and the potential maximum efficiency. Figure 8.8 shows a J_0-ρ_c map with the best results obtained in this work, compared to hole contacts from the literature. The black dashed lines indicate the Selectivity. The novel dielectrics in this work compare with some of the best poly-Si and DFPC contact structures using alternative dielectrics [178], [187], [327], [328] with Selectivities of 12-13. However, poly-Si contacts using SiO_x currently outperform the novel nanolayer dielectrics [156], [318], [329]. A significant increase in Selectivity is seen when a p-type poly-Si is deposited on n-type Si, reaching a Selectivity of >16. SiO_x contacts have been studied far more extensively enabling thorough optimisation of the contacts. The results presented here show the promise of these nanolayers and with further optimisation, there is scope for significant improvements.

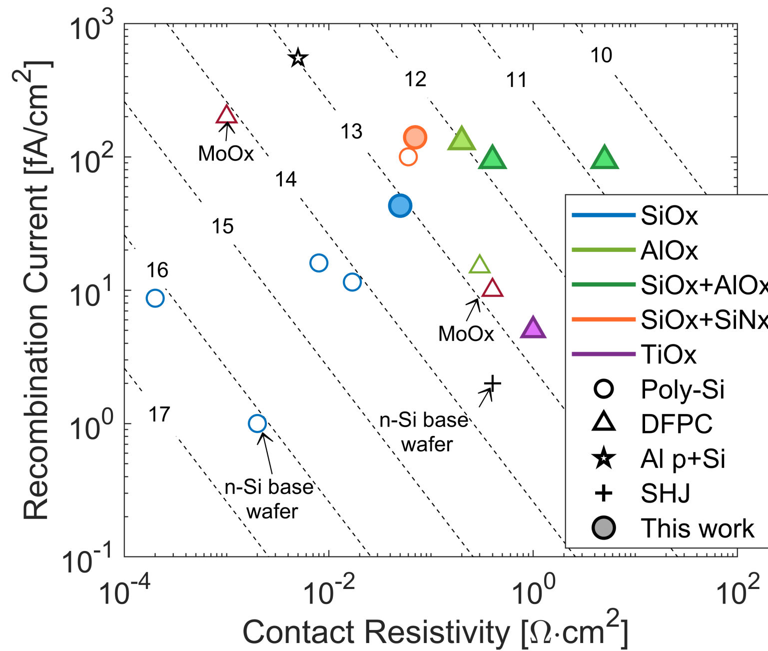


Figure 8.8: J_0 and ρ_c of the best contacts fabricated in this work and selected work from literature. Black dashed lines indicate the Selectivity. Results from this work are represented by shaded symbols and results from literature are shown as open symbols [156], [178], [187], [214], [318], [327]–[330].

8.5 Summary

SiN_x and AlO_x poly-Si contacts have been fabricated with low contact resistivity. A high pinhole density is observed, which may contribute to the low passivation in the AlO_x and SiN_x single layers. The RCA2+SiN_x stack achieved higher levels of passivation but is currently limited by substantial non-uniformity. Improved reliability of the nanolayer deposition, and the development of dielectric-specific poly-Si processing, will maximise the benefits of each dielectric, improving the passivation quality obtained. With optimisation, there is potential to fabricate contacts with ρ_c and iV_{OC} matching or outperforming the UV-O_3 control.

Chapter 9

Summary and Further Work

PV technologies are currently the fastest-growing source of electricity installations [24]. Obtaining higher power conversion efficiencies is crucial for reducing the cost of solar energy and maintaining this high growth rate. The silicon-metal contacts are a major source of recombination losses in current Si solar cells, so passivating contacts have been developed to reduce these losses. In poly-Si contacts, SiO_x is the standard dielectric used for both electron- and hole-selective contacts. SiO_x hole contacts are less effective than the equivalent electron contacts due to the high boron diffusivity and large valence band offset discussed in Section 2.9. In this work SiN_x, AlO_x and TiO_x were investigated as hole-selective passivating contacts in either dopant-free passivating contact (DFPC) or poly-Si contact structures. Simulations and multiple characterisation techniques were implemented to gain a detailed understanding of the nanolayers and the Si/nanolayer interface.

Sentaurus TCAD simulations studied the impact of dielectric fixed charge and doping profiles in passivating contact structures with alternative dielectrics. The simulations highlighted the benefits of a high negative charge in the dielectric for both the transport and passivation properties of the contact. It was also shown that the optimum doping profile is dependent on the dielectric charge. Lower doping in the poly-Si maximises the benefit of a high negative charge, while dielectrics with a low charge of either polarity benefit from high doping in the poly-Si as is already the case in SiO_x. The high negative charge in AlO_x and TiO_x, combined with low doping (such as in DFPCs) could form contacts that outperform SiO_x. The simulations show a reduction of two orders of magnitude in the dark saturation current (J_0) compared to a standard SiO_x contact, provided the chemical passivation is matched. The lower valence band offsets of SiN_x and AlO_x enable low resistivity hole contacts to be formed without pinholes. This is not the case for a hole selective SiO_x contact. A low contact resistivity (ρ_c) from a purely tunnelling current allows more control of the poly-Si processing conditions to optimise passivation.

Nanolayer AlO_x and SiN_x were fabricated to implement the benefits shown by simulations. Processes have been developed to deposit layers <2 nm with high uniformity, the first report of such uniformity for nanolayer PECVD SiN_x. The thickness control enabled the transport properties of the films to be shown as a function of thickness. Tunnelling contacts with ρ_c <100 m$\Omega\cdot$cm^2 were presented in Chapter 6 and ρ_c of 50-80 m$\Omega\cdot$cm^2 was measured in poly-Si structures. The conduction mechanisms in the nanolayer dielectrics were determined using temperature-dependent current-voltage measurements. This analysis has not been carried out for other work on SiN_x and AlO_x films. The layers show low, or no, pinholes with low-temperature processing but are

susceptible to pinhole formation at moderate anneal temperatures. The alternative nanolayers interact differently to SiO_x during the poly-Si processing, hence, tailoring the poly-Si for each dielectric is required to optimise the contacts.

The passivation of AlO_x and SiN_x layers was investigated both with and without poly-Si layers. The addition of an ultra-thin SiO_x can significantly improve the passivation of SiN_x and AlO_x contacts. This could be related to a lower D_{it} and, in the case of AlO_x, the change in Si surface chemistry, enhancing the ALD deposition in the initial stages. RCA+SiN_x/poly-Si stacks achieved J_0 of 140 fA/cm^2. AlO_x layers achieved better passivation (J_0 <100 fA/cm^2) without the poly-Si layer. Quantitative measurements of dielectric fixed charge showed a positive charge of $1{\times}10^{12}$ q/cm^2 in RCA+SiN_x nanolayers and a negative charge of $-3{\times}10^{12}$ q/cm^2 for RCA2+AlO_x. The Selectivity of the contacts is currently 12 for RCA2+AlO_x and 12.5 for RCA2+SiN_x. The PL images show areas with passivation matching that of the SiO_x, though processing issues currently limit the performance. Improving the sample handling, combined with an optimised poly-Si process to prevent excessive pinhole formation provides a route to fabricate hole contacts that outperform SiO_x. The high charge in AlO_x lends it to a DFPC structure, where the benefits of the charge can be maximised. So far, the AlO_x has not undergone any hydrogenation steps. If, with optimised hydrogenation, the AlO_x stacks can achieve similar chemical passivation to SiO_x, a DFPC using AlO_x could result in an efficiency gain of $\sim$1%$_{abs}$ and a maximum efficiency potential of over 28%.

The accurate extraction of charge in the contact structures required new methods to extract the interface properties of the highly conductive nanolayer dielectric structures. Two methods were developed and implemented on AlO_x, SiN_x and TiO_x nanolayers. The full benefits of the analysis were exploited for the TiO_x layers. The charge density was determined for multiple structures, processing conditions and ageing tests. Variations in the charge density were associated with performance changes in full cells, improving the understanding of the films and facilitating the novel contacts' optimisation. Highly-conductive and passivating contacts are becoming an increasingly important aspect of many electronic devices [331]. Characterising these interfaces effectively will lead to an improved understanding of the devices and facilitate efficiency enhancements. The techniques could be readily applied to interfaces in other PV systems, such as perovskites and tandems, and in a broader range of electronic devices, such as interfaces with 2D materials in nanoelectronics. Further to this, energy storage devices including batteries and fuel cells have multiple functional interfaces required for an effective design [332]. The knowledge gained from applying the methods for interface characterisation presented here could assist the future development of all these devices.

9.1 Future work

The nanolayer dielectrics fabricated in this work have shown promise in passivating contact structures. The properties of the nanolayers and the Si/dielectric interface were investigated. There are some alterations to the fabrication and processing to improve the layers further.

- XPS analysis showed that the SiN_x and AlO_x nanolayers were highly non-stoichiometric. Through optimisation of the sample surface chemistry and deposition parameters nanolayers with more stoichiometric compositions can be fabricated. This may improve the passivation quality of the nanolayers.

- The results in this thesis show a drop in the lifetime of RCA+AlO_x samples after moderate anneal temperatures. The cause of the poorer lifetime is suspected to be due to thermal shock. This can be checked by carrying out the anneal in a furnace and varying the cooling rate.
- The ellipsometry measurements show an increase in AlO_x thickness above 300 °C, while higher temperatures provide the optimum passivation quality. A study of the resistivity as a function of anneal temperature will determine if high temperatures cause a significant increase in the resistivity. If a significant increase is seen, the anneal may need to be carried out in an inert atmosphere.
- TEM images can be used to give a direct measurement of the films. This will enable a distinction of the dielectric and interfacial SiO_x layer thickness. TEM could also be applied to the nanolayers after the poly-Si deposition, or, after deposition on textured Si surfaces.
- Further study into the source of the negative charges in TiO_x and AlO_x could aid the deposition of highly charged layers. It could also provide a mechanism for the degradation seen in TiO_x under UV illumination.
- The TiO_x shows promise, but the efficiency suffers due to the reduction in V_{OC} on the textured wafers. Further optimisation of the hydrogenation steps could improve the chemical passivation, reducing the influence of the (111) surface plane.

The nanolayer/poly-Si contacts currently do not match the performance of the SiO_x control. From the initial results, there are some clear reasons for this and a number of routes to improve the alternative poly-Si hole contacts and deepen the understanding of the interactions of the nanolayers with the poly-Si.

- The nanolayer dielectrics are deposited in Oxford, then shipped to EPFL for the poly-Si deposition. The samples are packaged in a vacuum and desiccated atmosphere. However, the degradation of the films seen in Chapter 5 may not be entirely prevented. Ideally, the nanolayers should be deposited immediately before poly-Si deposition.
- The SiO_x and AlO_x show a deep diffusion but the boron diffusion in a Si/p^+poly-Si structure is not known. Measuring the doping profiles of a reference poly-Si contact without a dielectric will show the diffusion rate with no blocking layer. If the diffusion profile for a dielectric structure matches the reference, this shows no blocking has occurred and it may indicate the high-temperature anneal has caused a substantial break-up of the film.
- The PL images showed substantial in-homogeneity in the RCA2+SiN_x passivation. Improvement in sample handling, processing and transportation is necessary to achieve higher lifetimes.
- Sentaurus simulations of full cells with the experimental boron profiles. The experimental resistivity and J_0 can simulate the efficiency of a cell with the nanolayers fabricated in this work. The potential efficiency can be determined for a given improvement in ρ_c or J_0.
- Thicker dielectric layers or stacks and alterations in the poly-Si processing could prevent pinhole formation and improve passivation.

The capped C-V and G-V methods were developed to characterise conductive dielectrics. The techniques have enabled quantitative analysis of passivating contact structures. There are several areas that could be explored in more detail.

- Methods to study the interface properties of nanolayer dielectrics have been developed. However, it would be preferable to study the interface properties after the poly-Si deposition and high-temperature anneal. The easiest adaption would be to anneal the stack with the PECVD SiO_x at the high temperatures used. The interface would behave differently with a PECVD SiO_x instead of the a-Si capping layer, as the highly recombinative pinholes would not form. There is also no boron doping in this case. Another option would be to use a boron-doped SiO_x. This would enable an analysis of the dielectric interface after boron in diffusion, but it would still not form pinholes. A final option would be to carry out the poly-Si deposition and anneal, then selectively etch the poly-Si to leave the nanolayer dielectric. This could then be analysed using the method developed here. This enables the true interface to be studied, but etching the poly-Si without removing the dielectric would be experimentally challenging.
- The TiO_x can also be measured using the capped C-V method. As the TiO_x is not a tunnelling layer, some consideration is required to determine how this might affect the measurement.
- In addition to further investigation of the dielectrics studied here, many other materials for silicon passivating contacts could be analysed using these techniques. The techniques could also be adapted to allow the characterisation of non-silicon structures, such as perovskites.

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Appendix A: Derivation of Direct Tunnelling Current

In classical mechanics, when an electron approaches a barrier with a potential energy greater than its kinetic energy it will never be able to overcome the energy barrier and therefore the electron would be confined to one side of the barrier. However, in quantum mechanics, it is possible for the electron to be transmitted through the barrier. This is a result of wave-particle duality, where a particle of momentum, p, can be treated as a wavepacket with a wavelength of $\lambda = $ h/p. The MIS system discussed previously is an example where this phenomenon is crucial. Figure A1 shows the general case where a particle with a de Broglie wavelength λ and energy E is approaching a potential barrier of energy U and thickness t_d. To understand how the wave behaves in each region, the 1D time independent Schrödinger equation, shown in Equation 1, can be solved.

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} + U(x)\psi(x) = E\psi(x) \tag{1}$$

Where $\psi(x)$ is a wave function that varies with position x. The general solution to this equation is:

$$\psi(x) = Ae^{-\frac{ip}{\hbar}x} + Be^{+\frac{ip}{\hbar}x} \qquad \text{where,} \qquad p(x) = \sqrt{2m(E - U(x))} \tag{2}$$

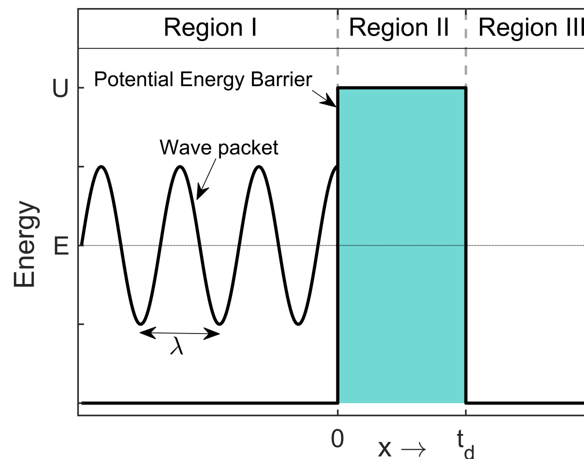


Figure A1: Free electron wave approaching a potential barrier

In Regions I and III,E>U so p(x) is real and equation 2 is in the form of a free wave that will propagate at a constant amplitude and momentum. In Region II, E<U so p(x) is imaginary and the exponential terms in Equation 2 are real. To avoid a nonphysical, exponential increase in the amplitude of the wavepacket the constant B must equal zero. With B=0 the wavefunction will undergo an exponential decay in Region II. The WKD (Wentzel Kramers Brillouin) approximation can be used to obtain quantitative values for the constants. First the Schrödinger equation is rearranged,

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} = \frac{p(x)^2}{\hbar^2}\psi(x). \tag{3}$$

Let,

$$\psi = A(x)e^{i\phi(x)}. \tag{4}$$

This can be differentiated twice (remembering A and ϕ are both functions of x) to give

$$\frac{d^2\psi}{dx^2} = [A'' + 2iA'\phi' + iA\phi'' - A(\phi')^2]e^{i\phi} = -\frac{p^2}{\hbar^2}Ae^{i\phi}. \tag{5}$$

Now the real and imaginary parts can be split. First taking the imaginary parts,

$$0 = 2A'\phi' + A\phi'' = (A^2\phi')', \tag{6}$$

$$C^2 = \int (A^2\phi')', \tag{7}$$

$$A = \frac{C}{\sqrt{\phi'}}. \tag{8}$$

Where C is a real constant. Now the real parts,

$$A'' - A(\phi')^2 = -\frac{p^2}{\hbar^2}A. \tag{9}$$

The WKD approximation can now be used, which states that the potential is varying slowly in comparison with the wavelength when E>U and slowly with $1/(\frac{ip}{\hbar})$ for regions where E<U. Thus A'' is negligible and can be assumed to equal 0. Equation 9 becomes:

$$(\phi')^2 A = -\frac{p^2}{\hbar^2}A, \tag{10}$$

$$\frac{d\phi}{dx} = \pm\frac{p}{\hbar}, \tag{11}$$

$$\phi = \frac{1}{\hbar}\int p(x)dx. \tag{12}$$

The wave function defined in Equation 4 can be expressed in terms of the momentum, p(x):

$$\psi = \frac{C}{\sqrt{p(x)}}e^{i\frac{1}{\hbar}\int p(x)dx}. \tag{13}$$

$\sqrt{\hbar}$ is absorbed into the constant C. Figure A2 depicts the qualitative solution to the wave function

for an electron tunnelling through a barrier. The probability of the particle tunnelling through the barrier, P_{tun}, is determined by the ratio of the amplitude of the incident wave and the transmitted wave,

$$P_{tun} = \frac{|\psi_{incident}|^2}{|\psi_{exiting}|^2}. \tag{14}$$

The magnitude of the incident wave is found by solving for region I and the magnitude of the exciting wave is found by integrating between 0 and t_d in Equation 13.

Application to a Silicon/Dielectric/Silicon Structure

Now Equation 13 is applied to the Si/Dielectric/Metal or Si/Dielectric/Si structures to determine the tunnelling probability and tunnelling current. The potential barrier is assumed to be square so E−U is constant and equal to the silicon/insulator band offset, ΔE (conduction band offset (CBO) for electrons and valence band offset (VBO) for holes).

$$P_{tun} = \frac{|\psi_{incident}|^2}{|\psi_{exiting}|^2}. \tag{15}$$

$$P_{tun} = \frac{C^2/p}{C^2/p{\cdot}e^{2/\hbar \int p(x)dx}} \tag{16}$$

$$P_{tun} = \exp\left(-\frac{2}{\hbar}\int_0^{t_diel} \sqrt{2m^*{\cdot}q\Delta E}\right) \tag{17}$$

$$P_{tun} = \exp\left(-\frac{2}{\hbar}{\cdot}t_{diel}\sqrt{2m^*{\cdot}q{\cdot}\Delta E}\right) \tag{18}$$

To convert from a tunnelling probability to a tunnelling current, the tunnelling probability can be combined with the thermionic emission current over a MS Schottky barrier. The thermionic emission current is derived from the number of electrons with sufficient energy to overcome the

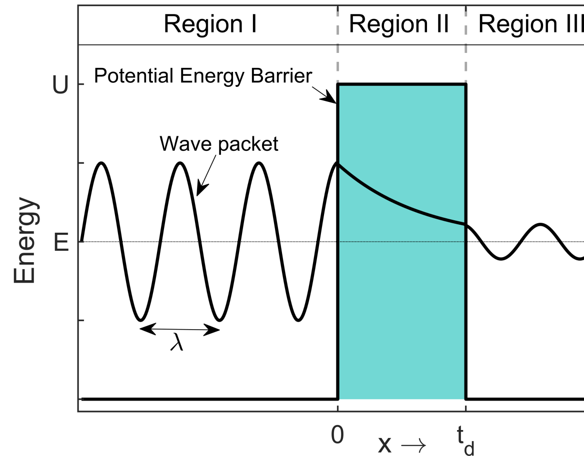


Figure A2: Qualitative solution to the potential barrier problem.

potential barrier. The current from the interface from the semiconductor to the metal is:

$$\mathrm{J}_{s\rightarrow m} = \int_{E_{Fn}+q\phi_{Bn}}^{\infty} q\nu_x N(E)F(E)dE \tag{19}$$

$$\mathrm{J}_{s\rightarrow m} = A^{*}T^{2}\cdot\exp\left(\frac{-q\phi_b}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \tag{20}$$

$$\tag{21}$$

Where ν_x is the average velocity of electrons in the x direction, N(E) is the density of states as a function of energy and F(E) is the Fermi-Dirac distribution, which gives the probability of a certain energy state being filled by a carrier. Equation 21 gives the solution of the integral. It is dependent on the temperature, T, applied voltage, V and the Schottky barrier height. q is the electron charge, k is the Boltzmann's constant, n is the ideallity factor and A^* is the Richardson constant. The physical quantity is given by:

$$A^{*} = \frac{4\pi q m^{*} k^{2}}{h^{3}}. \tag{22}$$

The value of m* is dependent on the semiconductor band alignment so it can vary with the semiconductor alignment and doping type (electrons vs holes). A^* is 250 for n-type [100] Si and 80 for p-type Si [46].

The total thermionic emission current, J_{TE} will be the sum of the current flowing from the semiconductor to the metal and the current flowing from the metal to the semiconductor. $\mathrm{J}_{m\rightarrow s}$ is identical to $\mathrm{J}_{s\rightarrow m}$ except the carrier concentration at the interface is independent of the applied voltage therefore the voltage dependent exponential term is not present.

$$\mathrm{J}_{TE} = \mathrm{J}_{s\rightarrow m} - \mathrm{J}_{m\rightarrow s} \tag{23}$$

$$\mathrm{J}_{TE} = A^{*}T^{2}\cdot\exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{24}$$

The direct tunnelling current is now obtained from $\mathrm{J}_{TE}\cdot P_t$, Equation 25,

$$\mathrm{J}_{tun} = A^{*}T^{2}\cdot P_t\cdot\exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right) - 1\right]. \tag{25}$$

The ϕ_b of the MIS system is likely to be lower then that of a MS as the dielectric interfacial layer reduces the D_{it} at the silicon surface (section 2.1.3).

Appendix B: Additional Methods

Cleaning

Before processing, each sample is cleaned using the standard RCA cleaning procedure to remove organic and inorganic contaminants from the surface of the samples [333]. RCA1 solution consists of ammonia (NH_3), hydrogen peroxide (H_2O_2) and de-ionised (de-I) water in a ratio of 1:1:5. It is heated to 80 °C using a hotplate and the sample is submerged in the RCA1 solution for 10 min, rinsed using de-I water for 5 min, and then dipped in 10% hydrofluoric acid (HF) for 1 min. The RCA1 process grows a thin oxide layer into the Si that slowly etches the Si and removes organic contaminants from the Si surface. Thorough rinsing ensures the RCA1 solution (now containing any organic contaminants) is fully removed from the sample surface. The HF dip removes the oxide to leave a bare Si surface. RCA2 solution is hydrogen peroxide, 40 wt% hydrochloric acid and de-I water at a ratio of 1:1:6. Again, the solution is heated to 80 °C and the sample is submerged for 10 min then rinsed for 5 min. The RCA2 solution also forms a thin oxide and slowly etches the Si, but removes inorganic contaminants from the Si surface. The oxide is removed with a final HF dip immediately before further processing.

Photoluminescence Imaging, PL

Photoluminescence imaging provides a spatially resolved map of the passivation quality across a sample. A flash of illumination is incident onto the sample and a photodetector collects the photons emitted as a result of radiative recombination in the sample. The signal detected will be highest in the regions with the best passivation. Regions with poor surface passivation or some bulk contamination will have a lower signal due to high levels of recombination via SRH of surface defects. The PL signal is given by [334],

$$A_i \cdot I_{PL} = B(N_D + \Delta n)\Delta n \tag{26}$$

Where A_i is the calibration factor, I_{PL} is the PL intensity and B is the radiative recombination coefficient. With appropriate calibration, the effective lifetime in a particular region of the sample can be extracted as a function of PL intensity.

The PL images are taken by collaborators at EPEL with an in-house built setup. The photocarriers are generated using an 808 nm wavelength laser and a PIXIS camera from Princeton Instruments is used for the imaging.

Electrochemical Capacitance–Voltage, ECV

ECV is a destructive technique used to measure the doping concentration in silicon as a function of depth. A capacitance-voltage curve is measured and N_{dop} is extracted from the slope of $1/C^2$ in the depletion region (Equation 3.24). The front contact is an electrolyte solution, with the area determined by a rubber seal. The technique is very sensitive to the measurement area to determine the absolute doping concentration, so any leaks or bubbles in the contact can result in errors in the doping concentration measured. Electrochemical etching of the silicon between measurements is used to obtain depth profiling [335].

The ECV measurements in this Thesis are performed by collaborators at EPFL using an ECV CVP21 tool from WEP. The electrolyte used is a 0.1 mol/L NH_4F solution. The technique is used to measure the doping profiles of Si/dielectric/poly-Si samples after the high-temperature anneal. A 4-point probe measurement of the poly-Si conductivity gave a sheet resistance of 90 $\Omega/\square$. Assuming the conduction is solely in the 40 nm poly-Si gives an upper limit to the [B] of 5×10^{20} cm^{-3}. A lower limit is obtained by assuming an equal contribution to the conductivity from the in-diffused region. A boron concentration of 9×10^{19} cm^{-3} is obtained from an effective thickness of 150 nm. N_{dop} measured by ECV gave $[B]_{poly-Si}$ to be 10^{20} cm^{-3}, in agreement with the 4-point probe measurement.

Appendix C: Simulations

MIS Structures

The metal-insulator-semiconductor contacts in dopant free passivating contacts (DFPCs) structures have a different band structure to the poly-Si contacts. A Schottky barrier is present at the silicon surface, which increases the resistivity of the contact. The width and height of the barrier are dependent on the substrate doping, the silicon/dielectric interface and the metal contact. The simulated DFPC structure is shown in A3 a gold contact is used for the resistivity contact, with a ϕ_b of 0.16 eV. The Schottky barrier height was determined in the T-J-V measurements in Chapter 6. The parameters for the poly-Si structure are found in Table 4.3.

Figure A4 compares the ρ_c and J_0 for a DFPC and a poly-Si contact. From inspection of Figures 4.7 and 4.9, it can be seen that the DFPC structure behaves in a similar manner to a poly-Si structure with low doping. Thus the conclusions for lightly-doped poly-Si contacts can be applied to DFPC structures.

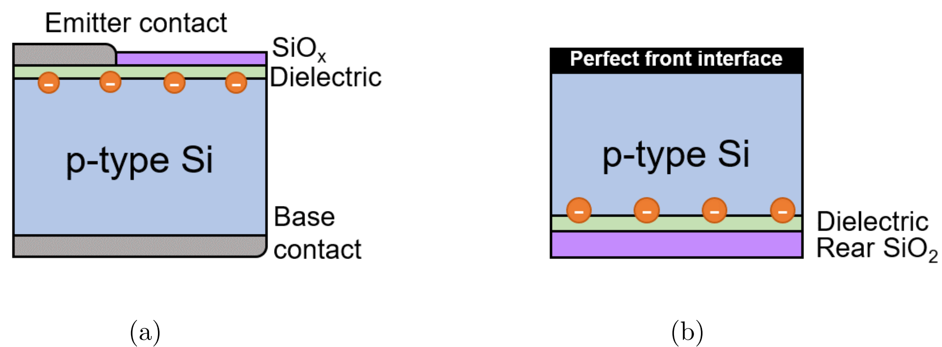
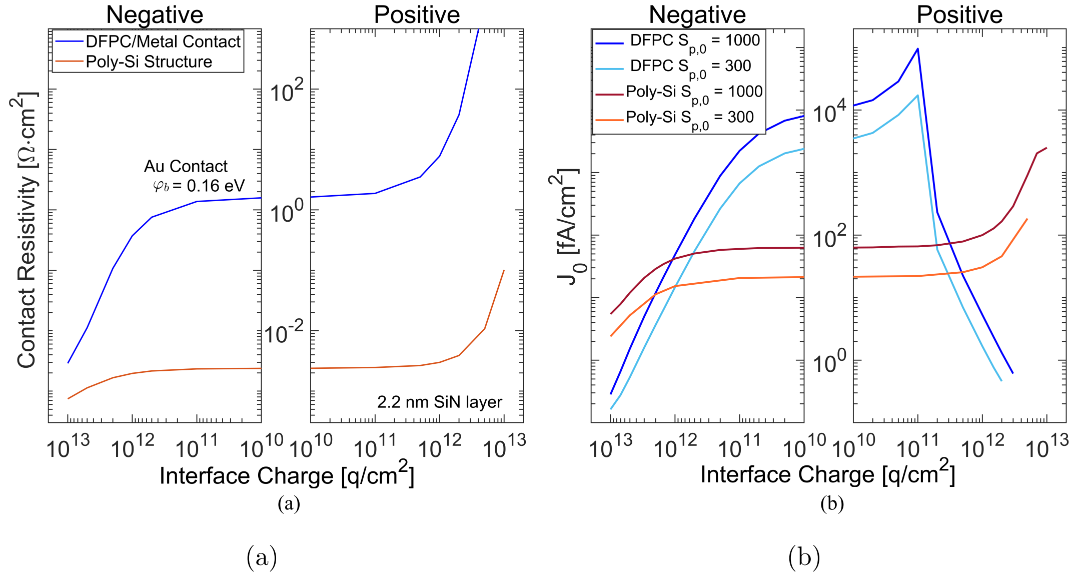


Figure A3: Schematics of simulated structures. a) poly-Si structure for contact resistivity simulations, b) DFPC structure for contact resistivity simulations c) poly-Si structure for J_0 Simulation.



(a) (b)

Figure A4: Simulations of a) ρ_c and b) J_0 for a DFPC structure and a poly-Si structure with the parameters from Table 4.3.

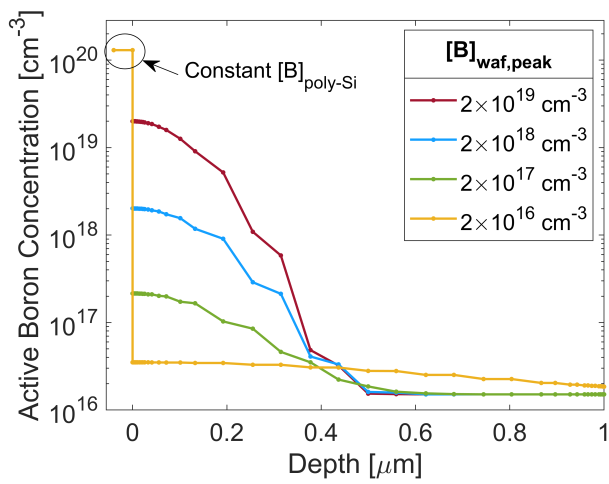
Doping profiles

In Figure A5(a), the $[B]_{\text{poly-Si}}$ is kept constant and the peak in-diffusion varied. As the in-diffusion is reduced, the difference between $[B]_{\text{poly-Si}}$ and $[B]_{\text{waf,peak}}$ increases, resulting in a larger built-in voltage across the junction. The low doping concentrations (yellow lines in Figure 4.4) are similar to the structures in DFPCs. An accurate simulation of DFPC uses a Schottky barrier contact model. This is included in Appendix 9.1.

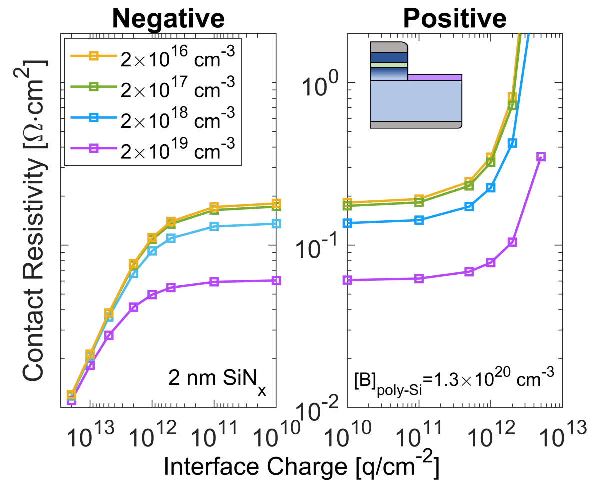
In Figure A5(b), the poly-Si concentration is set to 1.3×10^{20} cm^{-3} and $[B]_{\text{waf,peak}}$ was reduced from of 2×10^{19} down to 2×10^{16}, simulating a case where the in-diffusion is almost entirely blocked by the dielectric. Again, at a neutral charge a higher [B] results in lower resistivity. This shows that despite the constant high doping concentration in the poly-Si layer, the diffusion into the Si wafer is beneficial for minimising the contact resistivity. However, the effect of $[B]_{\text{waf,peak}}$ has a significantly smaller influence on ρ_c than the combined effect with the poly-Si doping shown in Figure 4.7. Again the lighter doping results in a stronger effect of charge. At high negative Q_f, the ρ_c of the lightest in-diffusion (yellow curve in Figure A5(b)) converges on the ρ_c of the highly doped in-diffused region.

Figure A5(c) investigates the effect on J_0. A large difference between the doping level in the poly-Si and Si wafer results in more FEP across the interface. The weaker in-diffusion gives lower J_0 values at almost all values of charge at the Si/Dielectric interface. Again the effect of charge is stronger for lower doping concentrations. The lower J_0 for lower $[B]_{\text{waf,peak}}$ is due to the combination of a higher field across the dielectric and a reduction in the Auger recombination. The increase in J_0 for positively charged interfaces is again minor below 10^{12} q/cm^2. In a real device, a doping profile with a low $[B]_{\text{waf,peak}}$ is formed when the dielectric provides an effective barrier to boron diffusion, such as in the SiN_x-poly-Si contacts in Chapter 8.

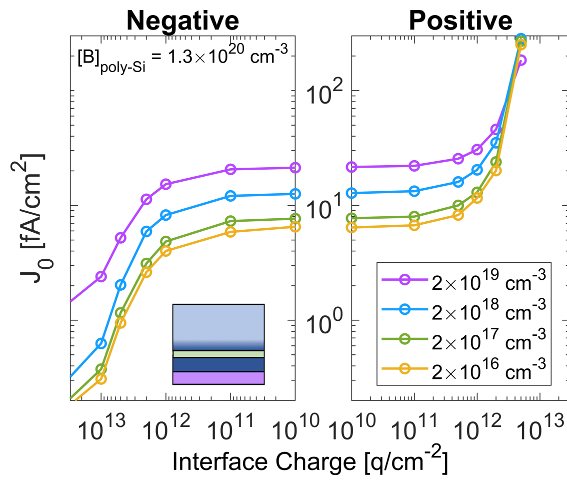
Figure A5(d) is obtained from Figures A5(b) and A5(c) using Equation 4.2. Compared to



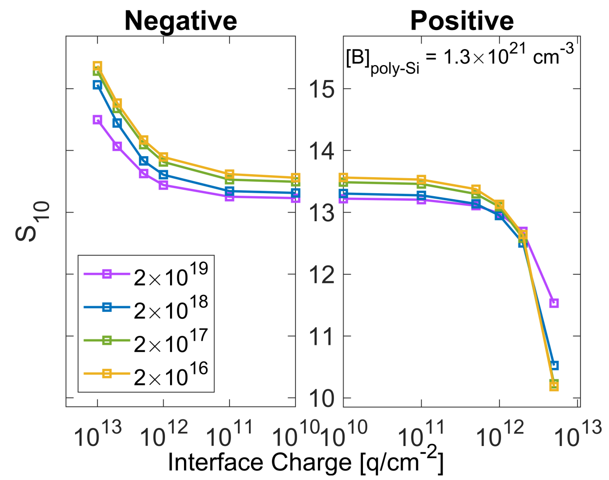
(a)



(b)



(c)



(d)

Figure A5: a) Doping profiles for varying peak in-diffusion, $[B]_{\text{poly-Si}} = 1.3\times10^{20}$ cm^{-3}. b) Resistivity c) J_0 and d) Selectivity of a 2 nm SiN_x/poly-Si contacts as a function of dielectric charge.

Figure 4.12, there is a smaller range in the Selectivity values. This is due to the competing effects of ρ_c and J_0. The lighter in-diffusion at the Si/dielectric interface enables a higher Selectivity for neutral and negative Q_f. The higher Selectivity shows that the benefit of a low J_0, due to lower Auger recombination and high FEP, outweighs the slightly higher resistivity.

Appendix D: Fitting inputs

SPV inputs and analysis

The Δn determination by matching the generated light vs Q curve. And note the other input parameters in the table.

Table A1: Standard Modelling Parameters for SPV Fitting.

Parameter	Value
Au WF	5.1 eV
Δn	5×10^{13} cm^{-3} (unless specified)
Doping Concentration	1.5×10^{15} cm^{-3}
Bulk lifetime	100 µs
Charge centroid, x_c	1 nm
$D_{it,tail}$	10^{15} cm^{-2}
Dielectric Permittivity	SiO_x 3.9, SiN_x 7.5, AlO_x 8, TiO_x 10
Capture Cross sections, σ_n,σ_p	10^{-15},10^{-15}

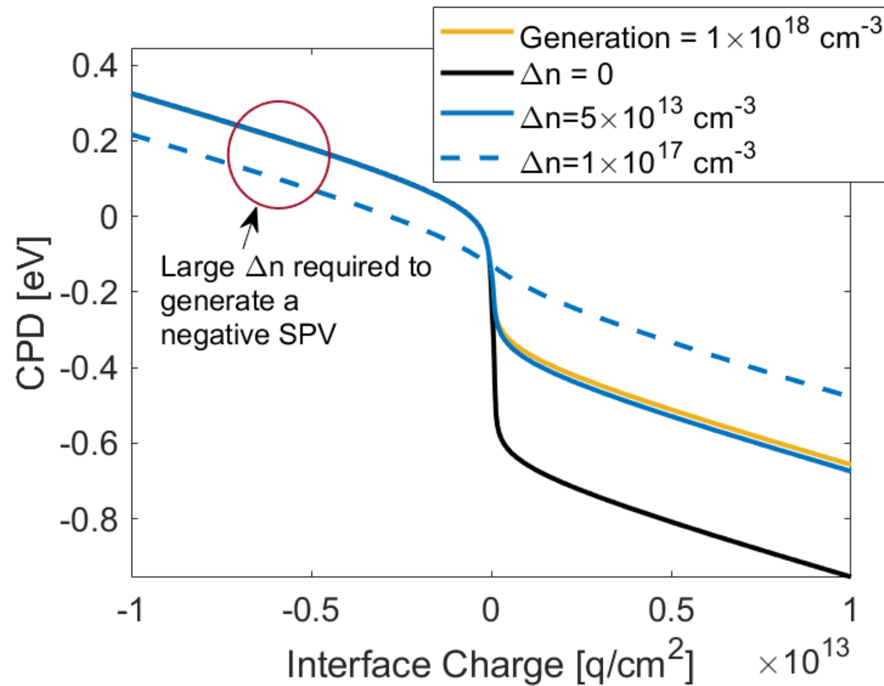


Figure A6: CPD signal as a function charge for determination of the carrier density during KP measurements. The black line indicates a measurement in the dark, the yellow line is generated by a carrier generation of 1×10^{18} cm^{-3} at the silicon surface, the blue line shows the equivalent carrier density of 5×10^{13} cm^{-3} to match the generation profile, and the dashed blue line show the high carrier density required to obtain a negative SPV on a p-type substrate, as seen in the AlO_x nanolayers.

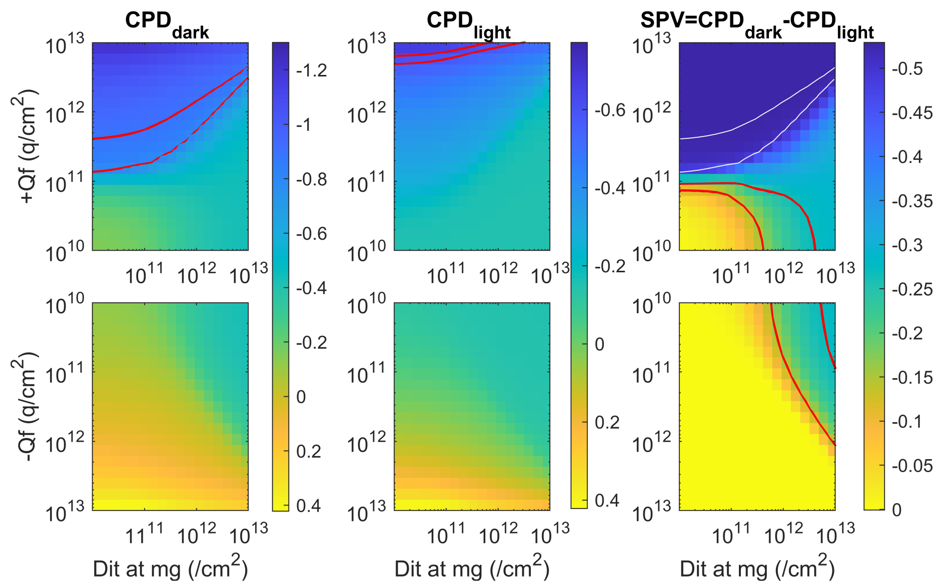


Figure A7: Estimated D_{it} and Q_f from as deposited SPV. Black lines show the CDP_{dark} values superimposed on the SPV graph.

Extraction of J0 from Lifetime

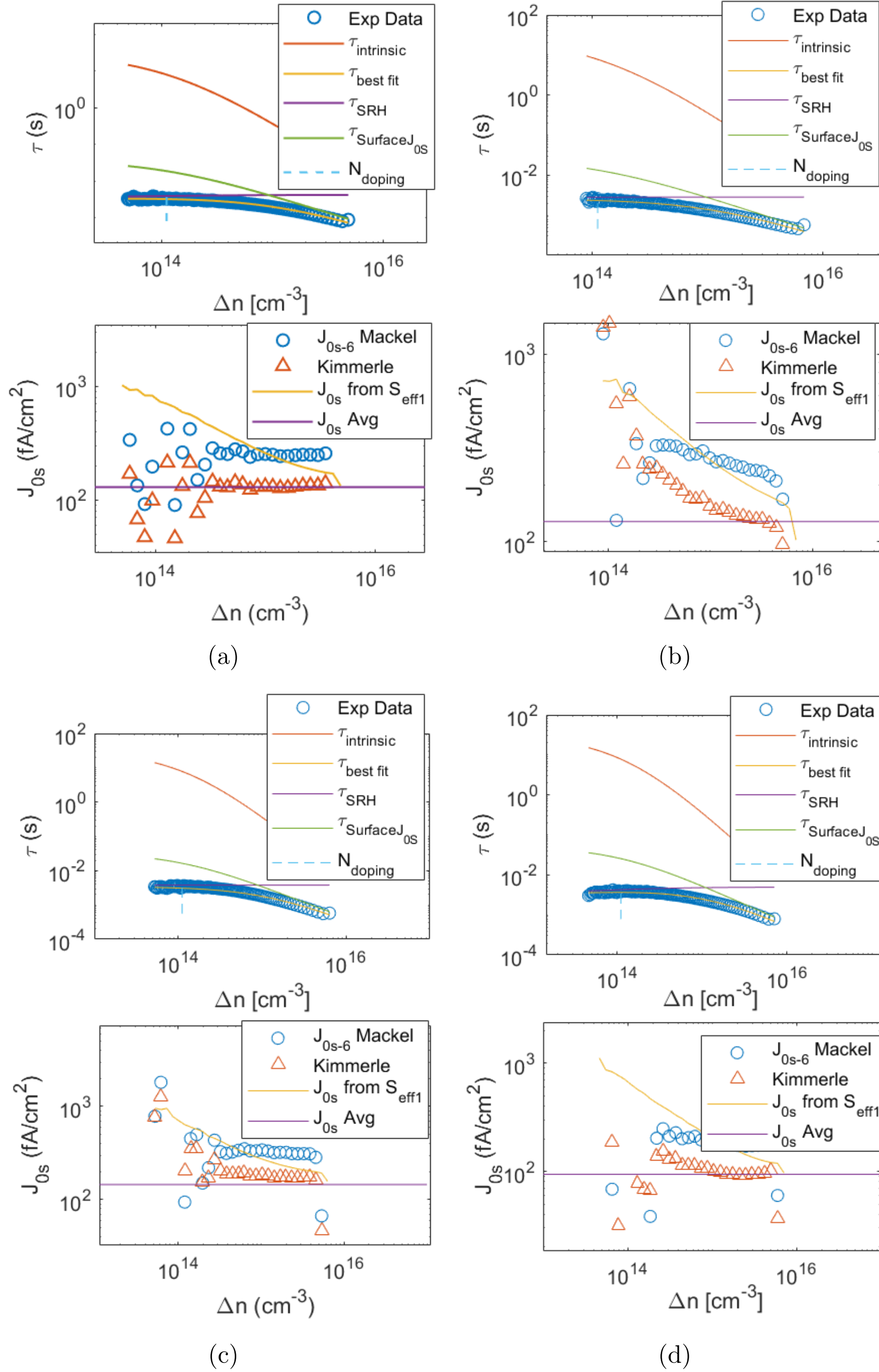
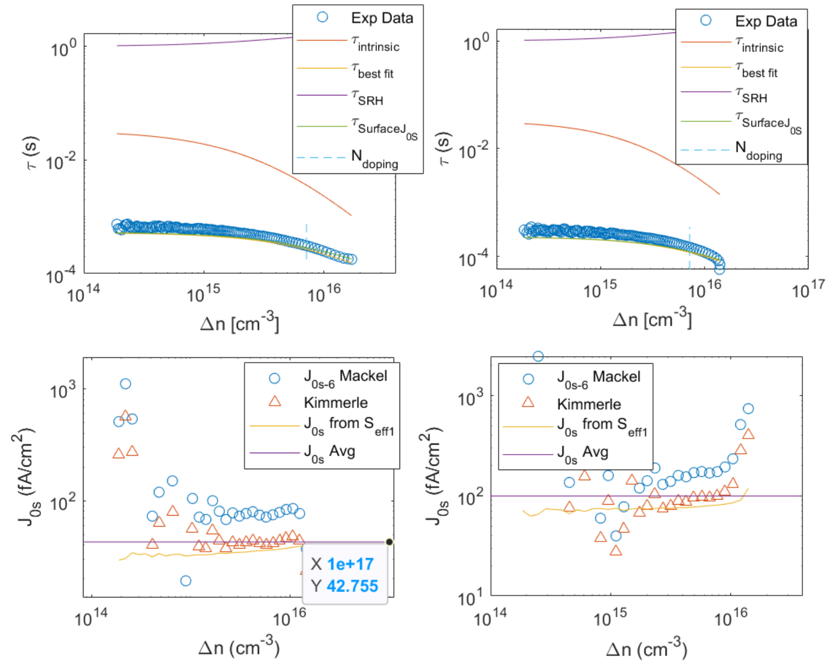
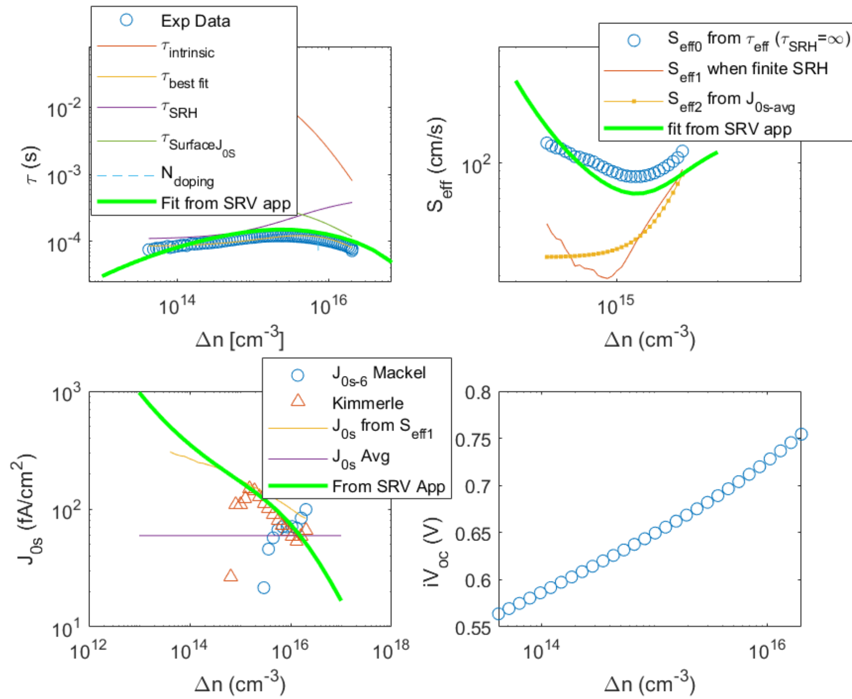


Figure A8: Extraction of J_0 values from fitting of τ_{eff} curves for a) a)10 cycles AlO_x, b) RCA+10AlO_x c) RCA+5AlO_x with negative corona d) RCA2+10AlO_x with negative corona.



(a)



(b)

Figure A9: Extraction of J_0 values from fitting of τ_{eff} curves for a) UV-O3 SiO_x/poly-Si b) RCA2+SiN_x/poly-Si. The automatic fitting of τ_{eff} for the RCA+SiNx gave an unrealistic value of J_0 so manual fitting of the τ_{eff} was carried out. The manual fitting shows good agreement for the τ_{eff}, S_{eff} and J_0. The J_0 value quoted is taken at $2{\times}10^{15}$ cm^{-3}, the minimum point on the S_{eff} curve.

Appendix E: Poly-Si

Effect of HF dip and Al firing on the Contact Resistivity of Poly-Si structures

Figure A10 shows the change in the resistivity for each processing step. The results for each anneal temperature follow the same trend. The HF dip removes any native oxide formed during the poly-Si anneal and transportation. Removal of this oxide results in a drop in the resistivity. Then the contact firing reduces the resistivity further by improving the contact between the poly-Si and the aluminium. Carrying out these steps ensures the contact resistivity at the poly-Si/Aluminium interface is minimised, so an accurate value for the dielectric resistivity can be obtained.

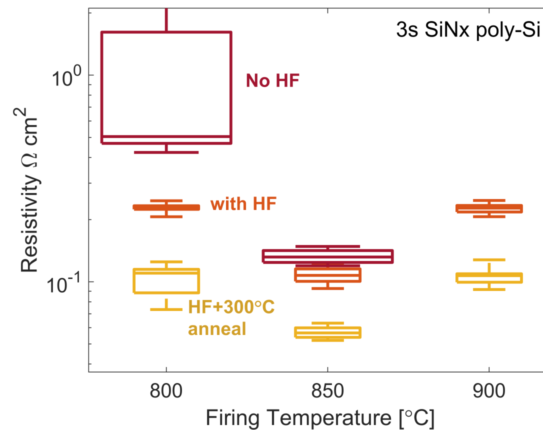


Figure A10: Contact resistivity of Dielectric/poly-Si structures with and without an HF dip to remove native oxide from the poly-Si and with contact firing.

Conducatance-Voltage Measurements of Poly-Si Structures

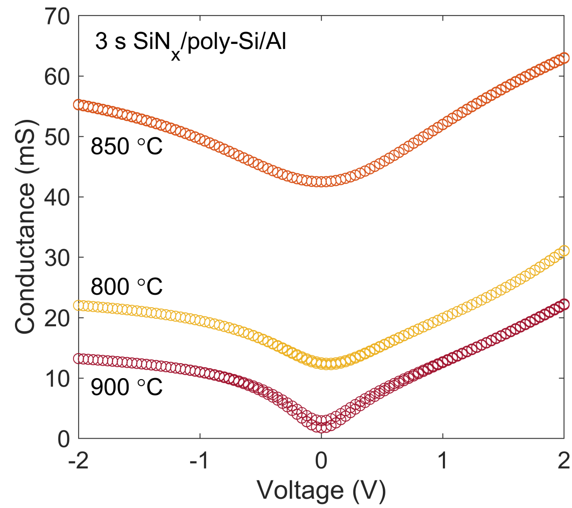
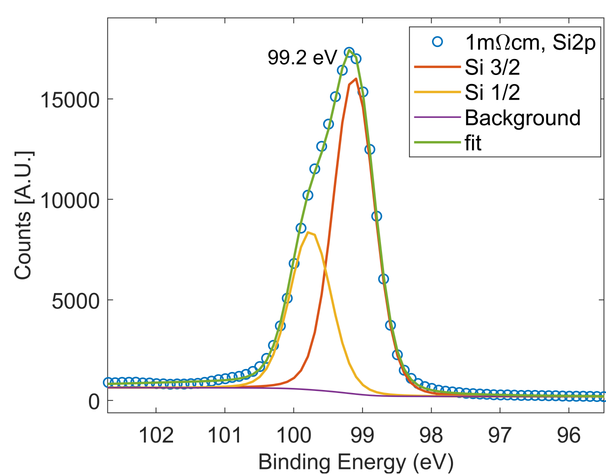
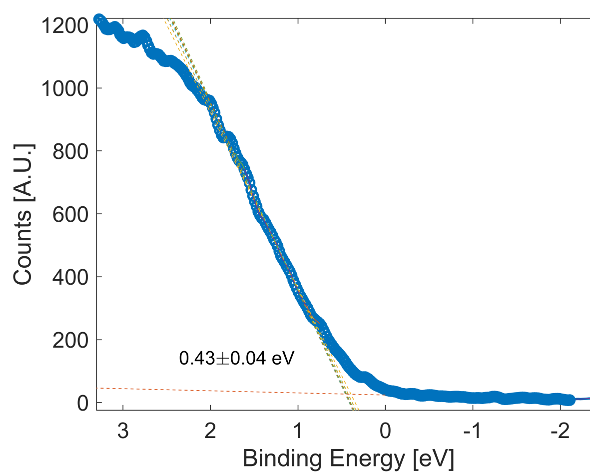


Figure A11: G-V measurement of 3 s SiN_x poly-Si structure. A high conductance is seen in at all voltages due to the high density of holes at both the Si/dielectric and dielectric/poly-Si interfaces.

Appendix F: XPS Peak fitting

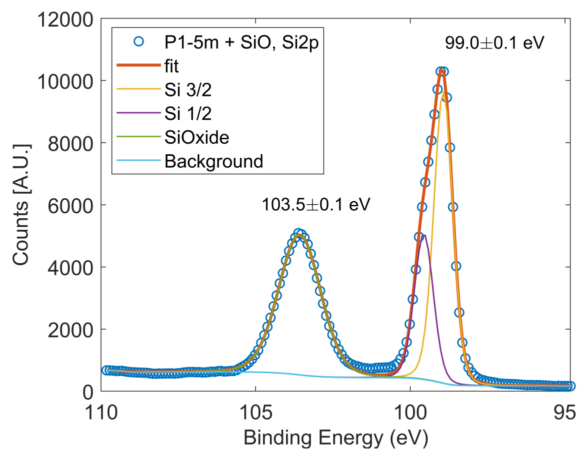


(a)

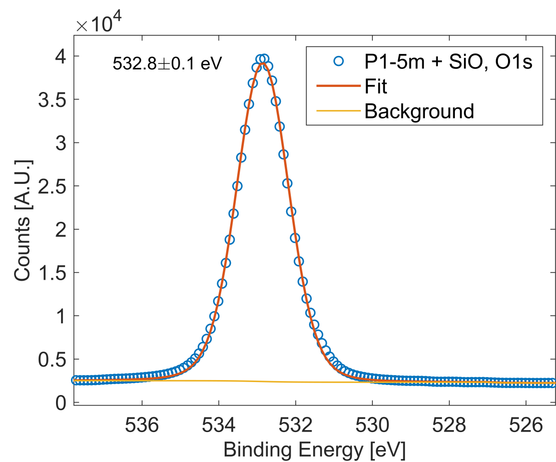


(b)

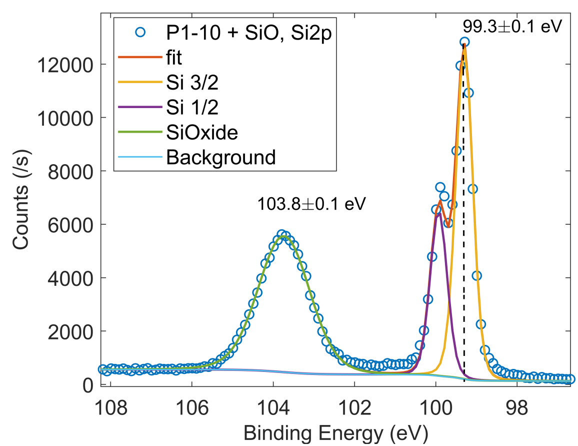
Figure A12: XPS data for P1-5m a) Si2p peak b) VBO



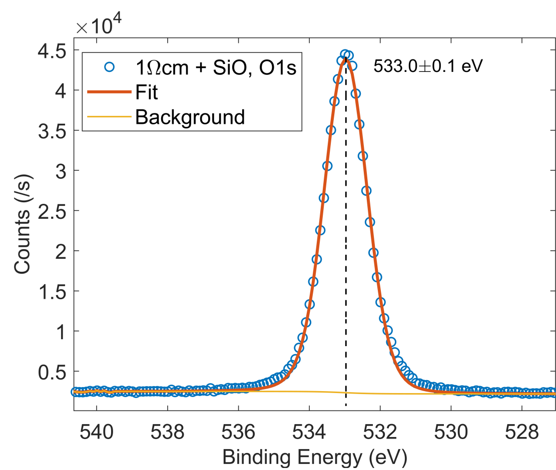
(a)



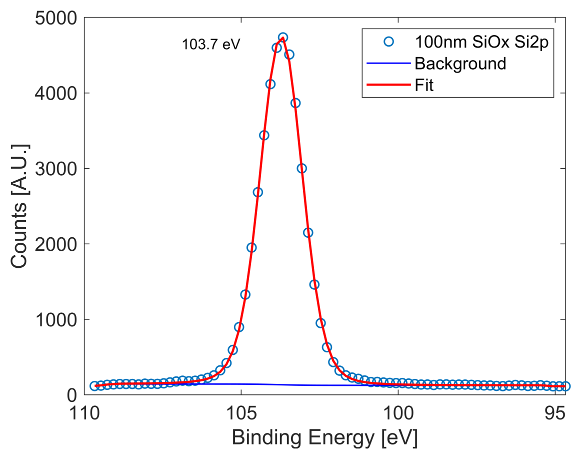
(b)



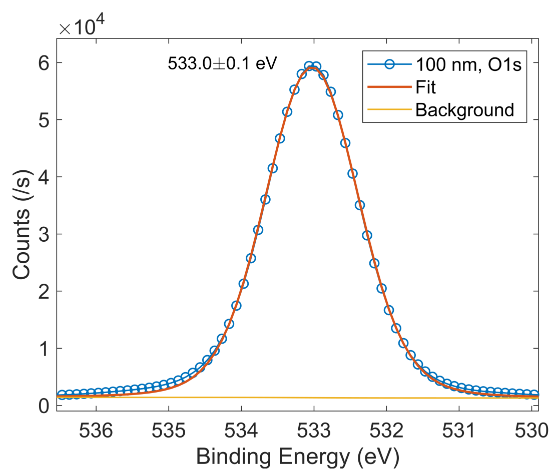
(c)



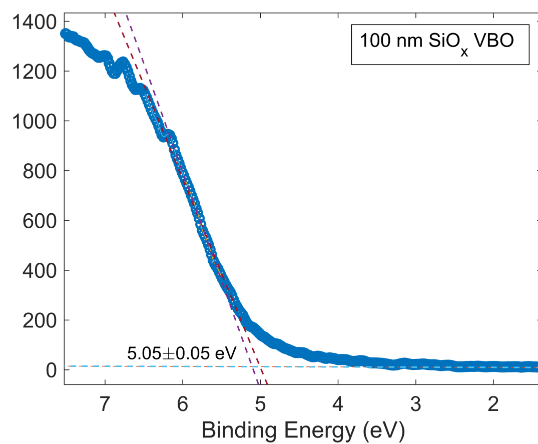
(d)



(e)

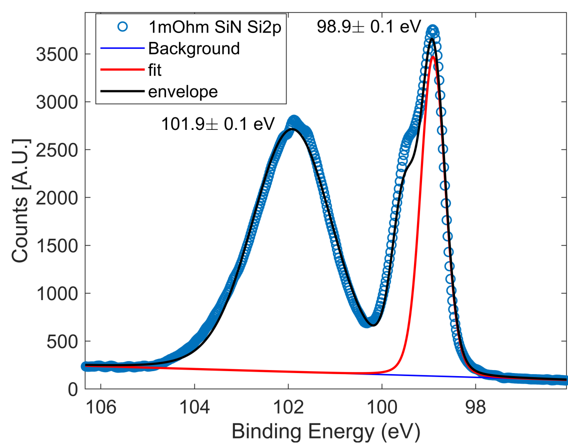


(f)

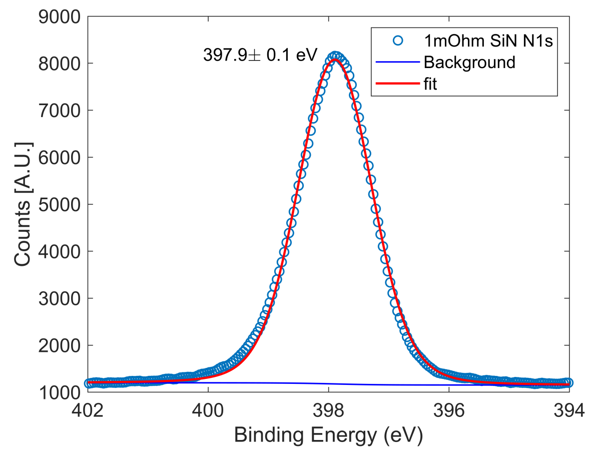


(g)

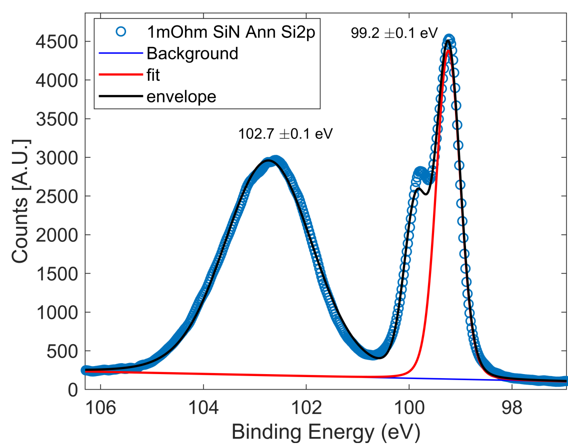
Figure A12: XPS data for SiO_x a) P1-5m Si2p peak b) P1-5m O1s peak c) 10 s RTO SiO_x Si2p peak d) 10 s RTO SiO_x O1s e) 100 nm SiO_x Si2p f) 100 nm SiO_x O1s peak g) 100 nm SiO_x VBO.



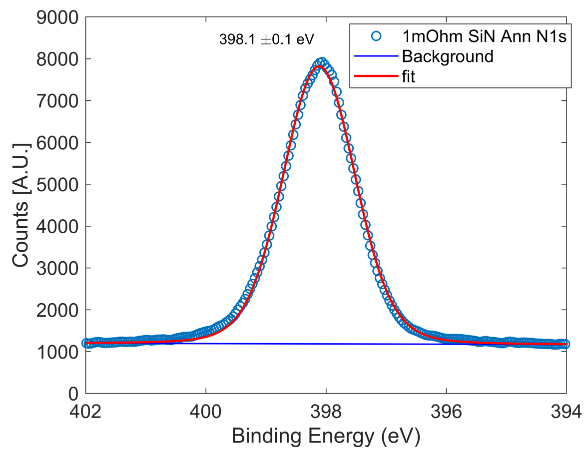
(a)



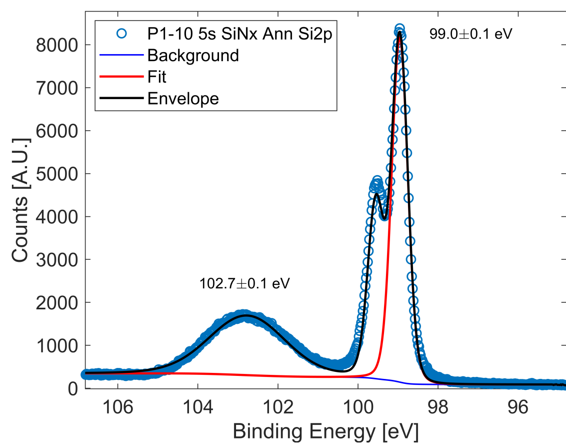
(b)



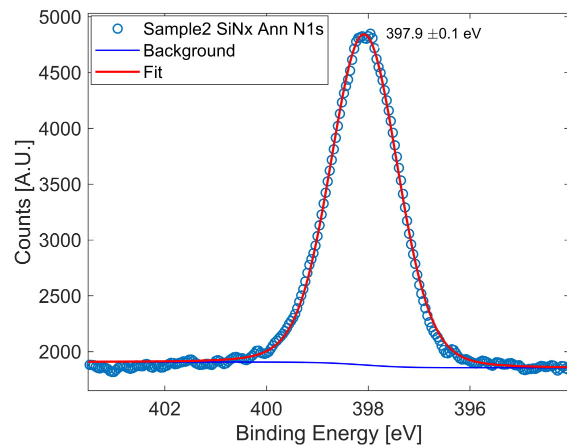
(c)



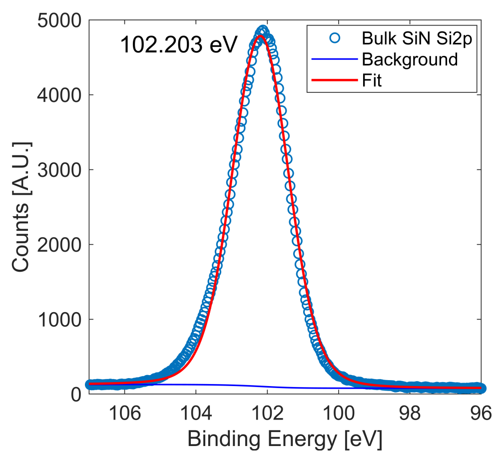
(d)



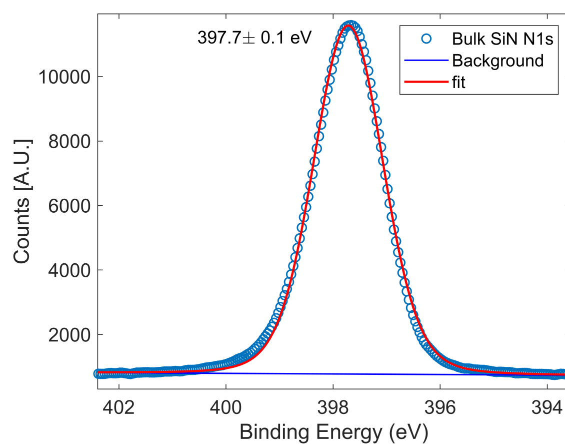
(e)



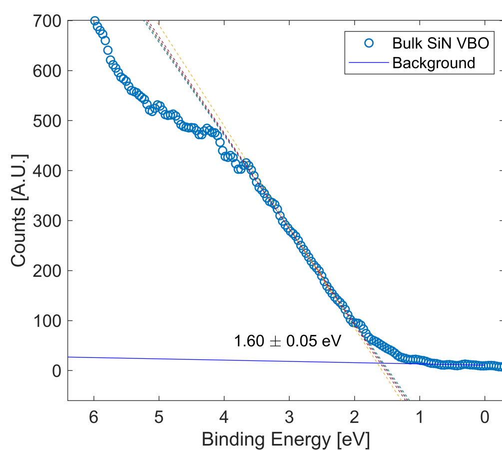
(f)



(g)

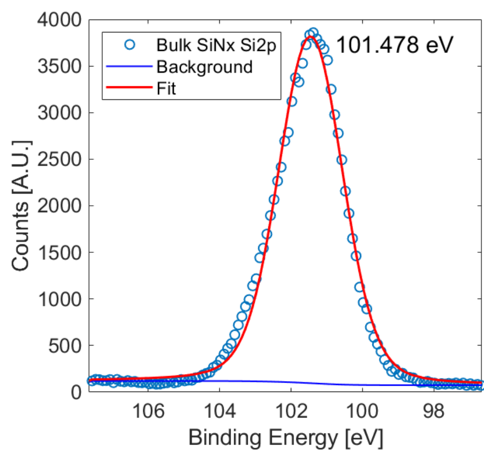


(h)

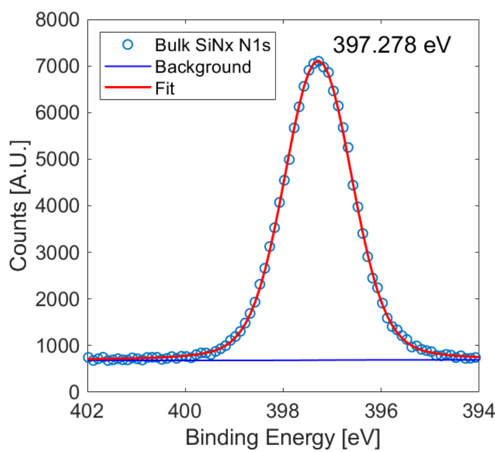


(i)

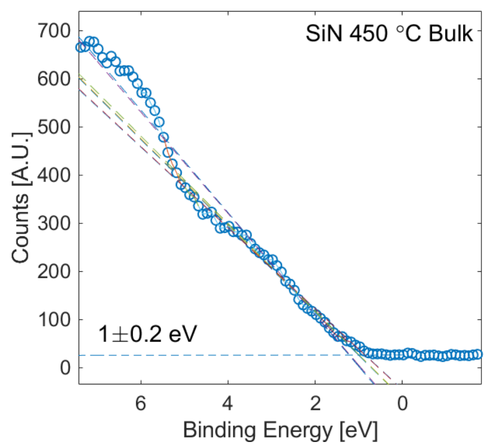
Figure A12: TSK XPS data for SiN_x a) P1-5m Si2p peak b) P1-5m N1s peak c) P1-5m annealed Si2p peak d) P1-5m annealed N1s peak e) P1-10 5s SiN_x annealed Si2p peak f) P1-10 5s SiN_x annealed N1s peak g) Bulk SiN_x Si2p peak h) Bulk SiN_x N1s i) Bulk SiN_x VBO



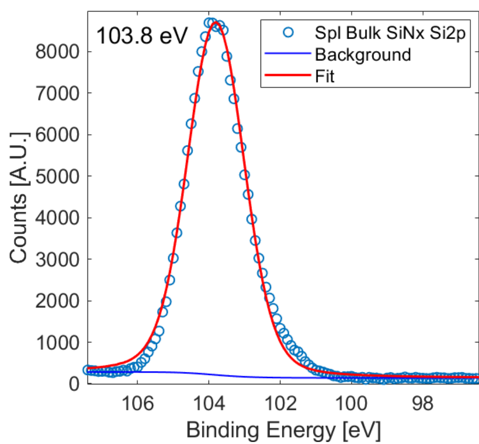
(a)



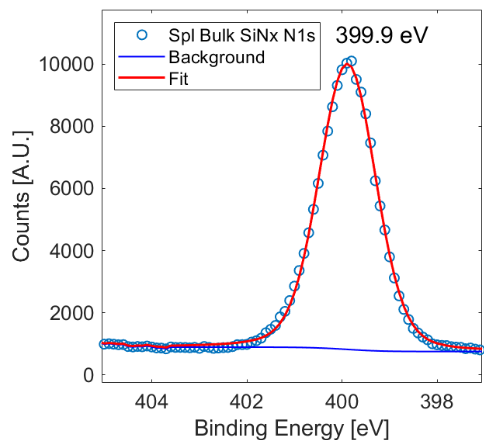
(b)



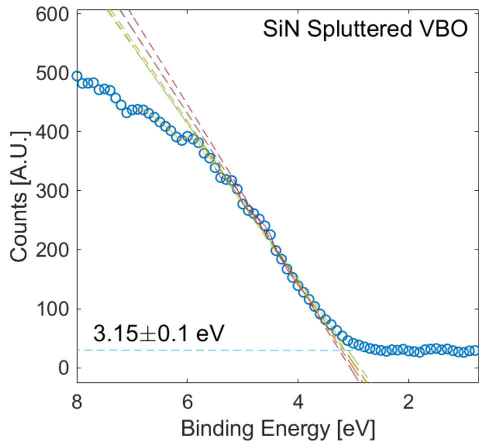
(c)



(d)

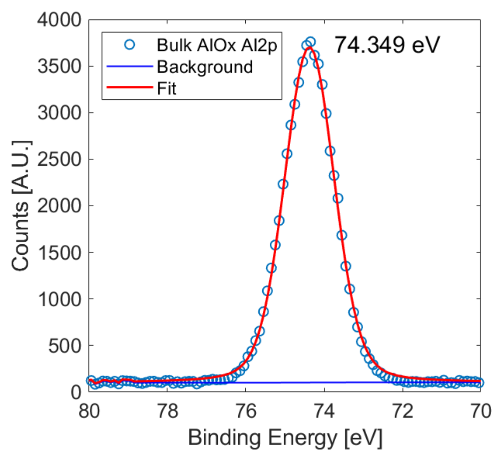


(e)

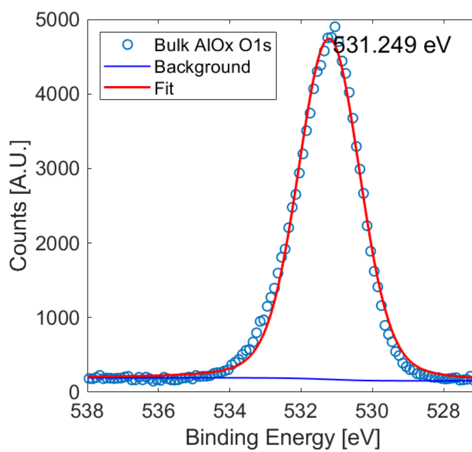


(f)

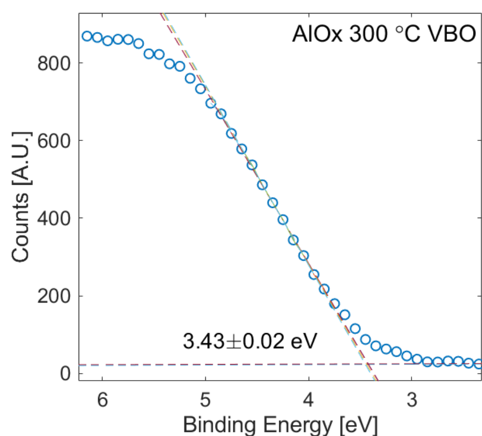
Figure A13: PhiV XPS data for a),b),c) bulk SiN_x and d),e),f) spluttered bulk SiN_x



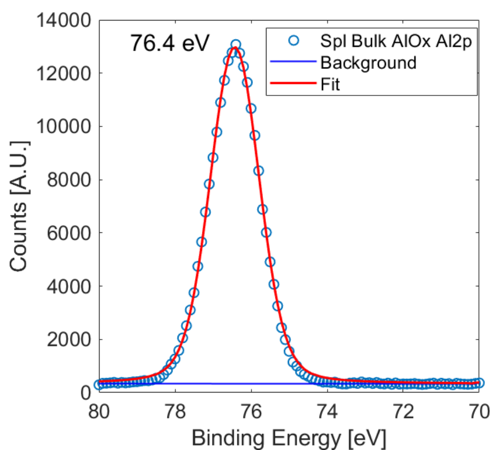
(a)



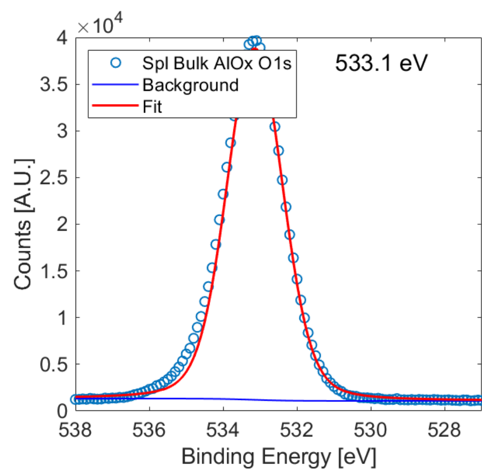
(b)



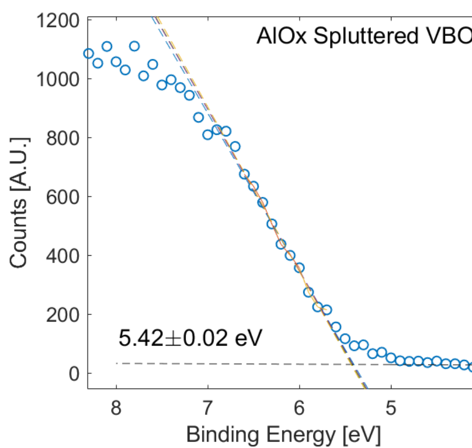
(c)



(d)

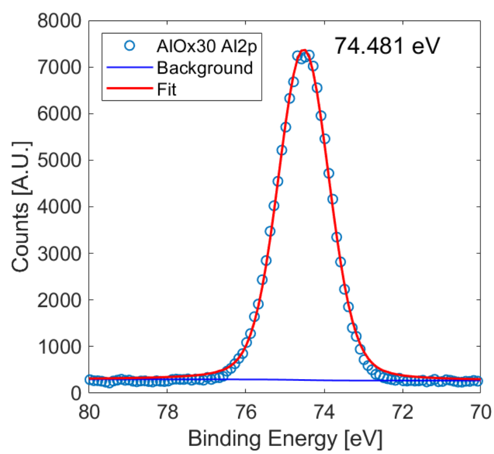


(e)

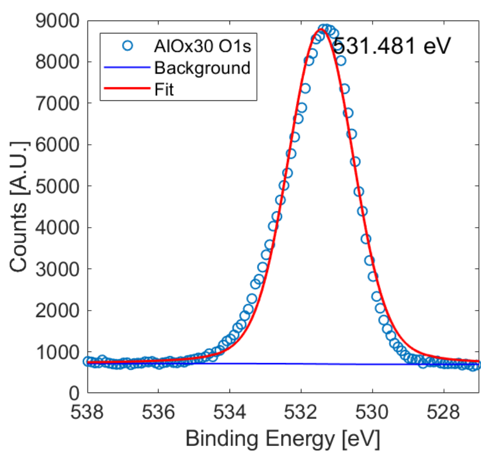


(f)

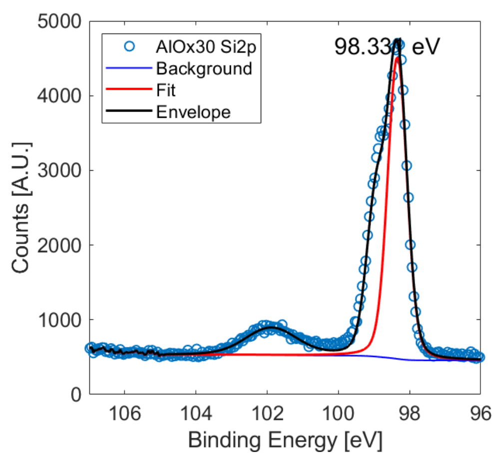
Figure A14: XPS data for a),b),c) bulk AlO_x and d),e),f) spluttered bulk AlO_x



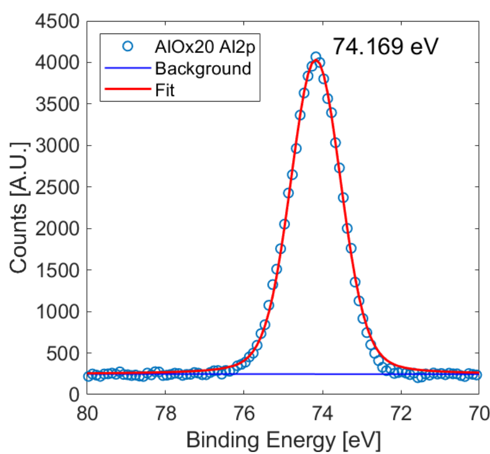
(a)



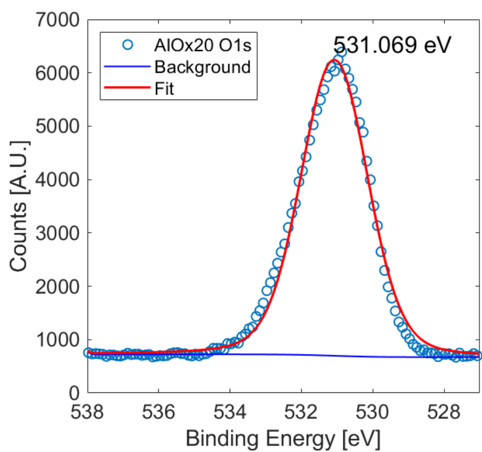
(b)



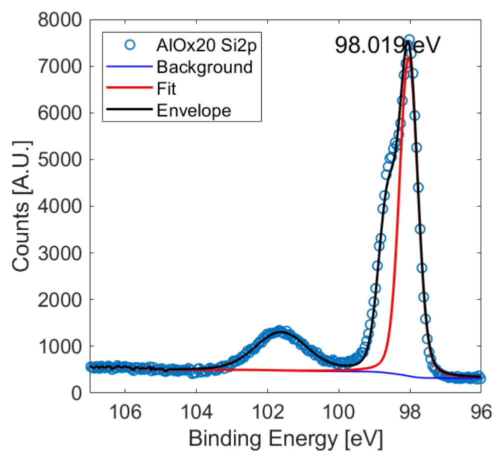
(c)



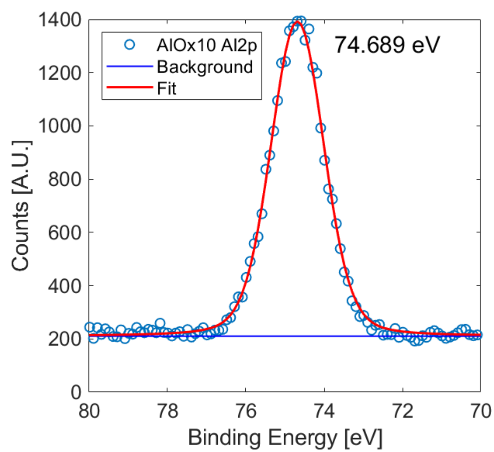
(d)



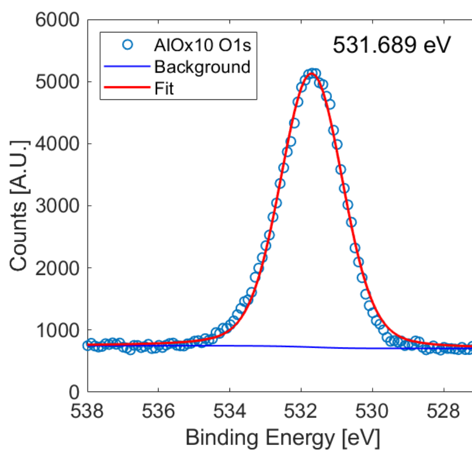
(e)



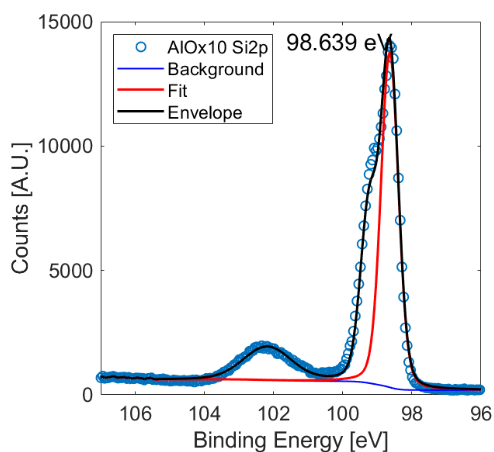
(f)



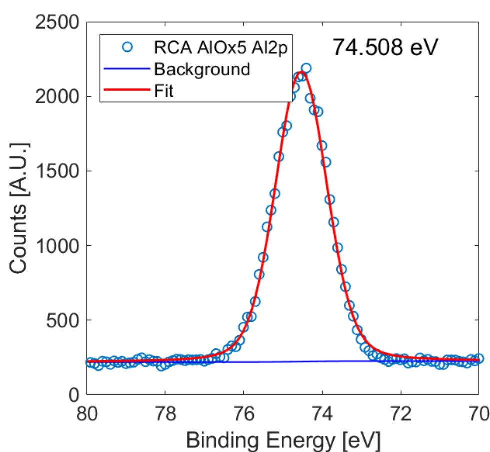
(g)



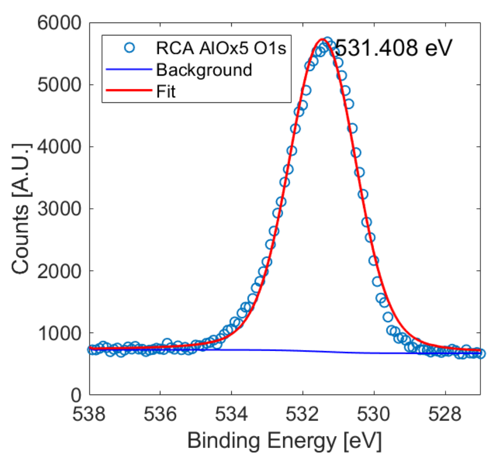
(h)



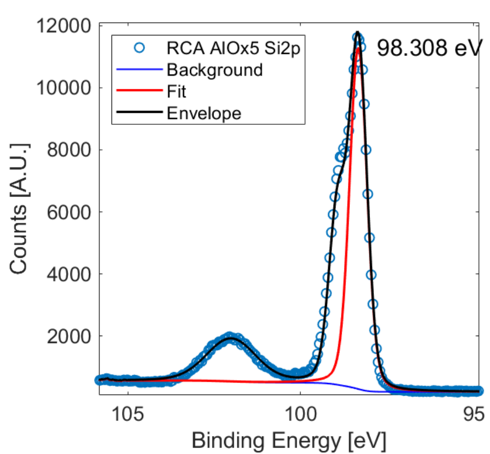
(i)



(j)

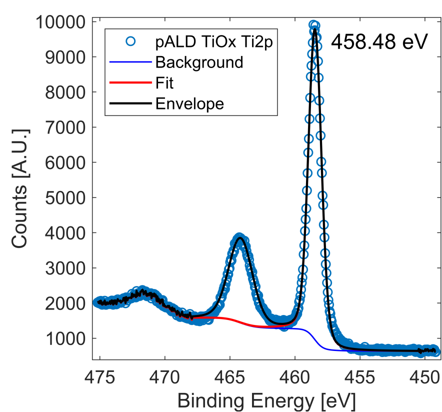


(k)

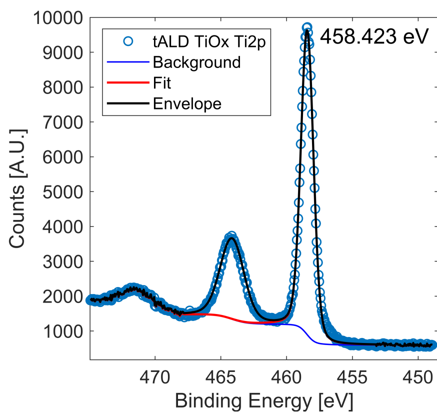


(l)

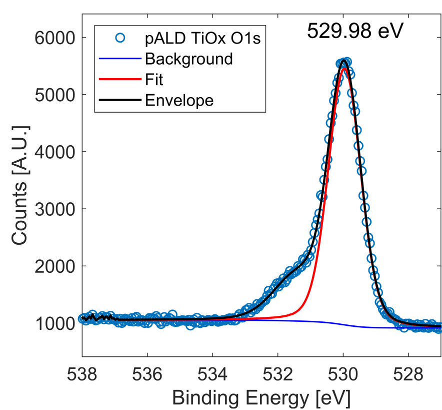
Figure A14: XPS data for thin AlO_x films on P1-10. a)-c) 30 cycles, d)-f) 20 cycles g)-i)10 cycles j)-l) RCA2+5 cycles



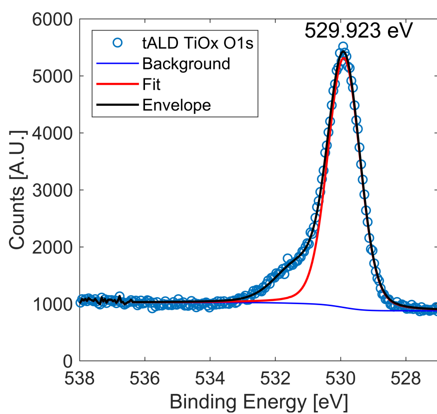
(a)



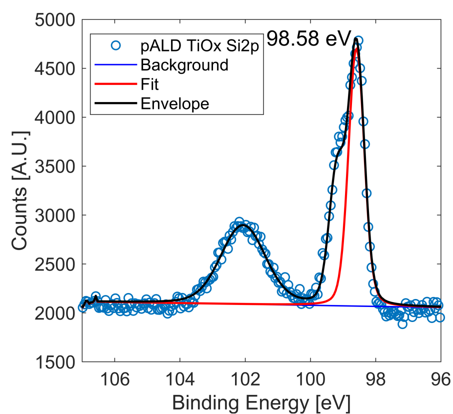
(b)



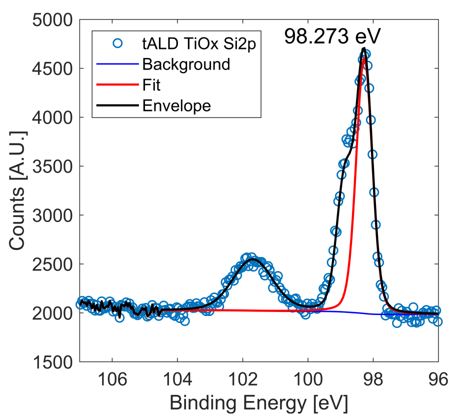
(c)



(d)



(e)



(f)

Figure A15: XPS peaks for TiO_x a) pALD Ti2p peak b) tALD Ti2p peak c) pALD O1s peak d) tALD O1s peak e)pALD Si2p peak f) tALD Si2p peak