Battery management systems with active loading and decentralised control

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To my family at home, my family who helped make me feel at home, and my new family members.

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Abstract

This thesis presents novel battery pack designs and control methods to be used with battery packs enhanced with power electronics. There are two areas of focus: 1) intelligent battery packs that are constructed out of many hot swappable modules and 2) smart cells that form the foundation of a completely decentralised battery management system (BMS). In both areas, the concept of active loading/charging is introduced. Active loading/charging balances the cells in a battery pack by loading each cell in proportion to its capacity. In this way, the state of charge of all cells in a series string remain synchronized at all times and all of the energy storage potential from every cell is utilized, despite any differences in capacity there may be. Experimental results from the intelligent battery show how the capacity of a pack of variably degraded cells can be increased by 46% from 97 Wh to 142 Wh using active loading/charging.

Engineering design challenges of building a practical intelligent battery pack are addressed. Start up and shut down procedures, and their respective circuits, were carefully designed to ensure zero current draw from the battery cells in the off state, yet also provide a simple mechanism for turning on. Intra-pack communication was designed to provide adequate information flow and precise control. Thus, two intra-pack networks were designed: a real time communication network, and a data communication network.

The decentralised control algorithms of the smart cell use a small filtering inductor as a multi-purpose sensor. By analysing the voltage across this filtering inductor, the

switching actions of a string of smart cells can be optimised. Experimental results show that the optimised switching actions reduce the output voltage ripple by 83% and they synchronize the terminal voltages of the smart cells, and by extension, their states of charge. This forms the basis of a decentralised BMS that does not require any communication between cells or with a centralised controller, but can still achieve cell balancing through active loading/charging.

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Nomenclature

There are a few symbols with multiple meanings, such as the letter "D". It is used to label diodes and it is used to represent duty cycle. In these situations, the definition should be clear based on the context in which the symbol is used.

Abbreviations

AB	Active Balancing
ac	Alternating Current
ADC	Analogue to digital converter
BMS	Battery Management System
CAN	Controller Area Network
CCCV	Constant Current, Constant Voltage
CCpCV	Constant Current, Pseudo Constant Voltage
dc	Direct Current
DIN	Deutsches Institut für Normung (German Institute for Standardization)
EES	Electrical Energy Storage
EV	Electric Vehicle
FPU	Floating Point Unit
GaN	Gallium Nitride

HEV	Hybrid Electric Vehicle
HVDC	High Voltage Direct Current
Li-ion	Lithium-ion
Mbps	Mega Bits Per Second
MCU	micro-controller
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PB	Passively Balanced
PE	Power Electronics
PWM	Pulse Width Modulator
SiC	Silicon Carbide
SOC	State of Charge
SOH	State of Health
SPDT	Single Pole, Double Throw
VL	Variable Loading/charging
Wh	Watt-hours

Roman

B_k	battery of the k^{th} module or smart cell
C	C-rate [A/Ah]
C	capacitance [Farads]
C_k	capacity of the k^{th} module or smart cell [Ah]
$C(s)$	controller transfer function
$\hat{d}$	ac duty cycle

D	diode
D	duty cycle
E	energy [J] or [Wh]
f_s	switching frequency $[Hz]$
$G\,(s)$	control to output transfer function
I	current [A]
K	Kuramoto controller gain
K_p	proportional gain
K_i	integral gain
L	inductance [H]
$\mathbf{L}$	Hessian matrix
M	total number of modules or smart cells in a pack
n	counter
N	a total number of elements
Q	MOSFET
Q_H, Q_L	smart cell MOSFETs
$Q_{H,k}$, $Q_{L,k}$	MOSFETs of the k^{th} module
R	resistance [Ω]
RLY_k	k^{th} relay
s	Laplace variable
$S_{A,x}$	active switching state x
$S_{E\text{-}C,x}$	extraction switching state x during charge
$S_{E\text{-}D,x}$	extraction switching state x during discharge
$S_{I,x}$	insertion switching state x

t	time [s]
T_h	time [h]
T_s	switching period [s]
$T(s)$	loop gain
v_L	voltage across the smart cell inductor, L_{sc} [V]
V_{nom}	nominal battery cell voltage [V]
X_u	random number uniformly distributed between 0 and 1

Greek

δ	phase shift [radians]
γ	phase in rotated reference frame [radians]
ω	frequency [radians/s]
ϕ_k	phase shift of the k^{th} smart cell or module [s]
σ	standard deviation
θ	phase [radians]

Subscripts

B	balance
d	duty cycle
i, j	counters
i	current
IB	intelligent battery
k	used to specify a single module or smart cell
m	module

M number of series connected modules or cells

sc smart cell

v voltage

Superscripts

C capacitors

L inductors

S switches

T transformers

Chapter 1

Introduction

Power electronics is the workhorse of our energy-craved society, burdened with the loads of our machines. It is used everywhere - from the single watt converters found in cell phones [2], all the way up to the gigawatt converters used in High Voltage Direct Current (HVDC) transmission lines [3]. Power electronics is also playing a key role in the reduction of green house gas emissions through the integration of green energy technologies with the grid [4, 5].

As energy generation on the electricity grid becomes increasingly decentralized, there will be an even greater penetration of power electronics into our daily lives. It is estimated that by 2030, 80% of all grid power will use power electronics between its generation and consumption [6]. Therefore, power electronics engineers must develop efficient, reliable power converters to ensure the robustness of the electrical energy distribution system [7].

One area of increased power electronics penetration is electrical energy storage (EES) [8], where the market is growing very rapidly [9–11]. For example, the EES market in the United States of America is expected to grow from 231 MW in 2016 to 2.5 GW in 2017 [12]. This rapid adoption of grid-connected EES requires state of the art power electronic converters and energy management systems. Furthermore, since

the energy storage device (battery cells, for example) is the most expensive component [13], the power electronics should be designed to maximise their performance and lifetime whilst ensuring safety [14], [15].

The integration of power electronics into energy storage systems is the main topic of this thesis. The following chapters will explore how power electronics can be more tightly integrated with energy storage systems to yield improved system reliability and performance. The remainder of this chapter is dedicated to motivating research into this subject area and a review of the current state of the art.

1.1 Battery states

When discussing batteries or cells, the terms state of charge (SOC) and state of health (SOH) are frequently used, and it is important to define what they mean. For the remainder of this subsection, "batteries or cells" will be referred to as "cells". Throughout this thesis, the SOC of a cell will be defined as the percentage of the remaining energy for a given normalized current rate, or C-rate:

$$\text{SOC} = \frac{E_{R\text{-}C_x}}{E_{T\text{-}C_x}} \times 100\%, \tag{1.1}$$

where $E_{R\text{-}C_x}$ is the energy remaining in the cell at a C-rate of C_x and $E_{T\text{-}C_x}$ is the total amount of energy that the cell can store if discharged at a C-rate of C_x. The C-rate C_x is defined as:

$$C_x = \frac{I_x}{C_{Ah}}, \tag{1.2}$$

where I_x is the current through the cell and C_{Ah} is the rated capacity of the cell measured in Amp-hours. In applications where the C-rate varies with time, the total amount of remaining energy can be calculated as:

$$E_R(t) = E_T - \int_0^t v(t)\, i(t) - f_{\text{loss}}(v(t), i(t), T(t), SOC(t))\, dt, \tag{1.3}$$

where E_T is total, rated amount of energy that the cell can hold, $v(t)$ is the terminal voltage of the cell, $i(t)$ is the current through the cell, $T(t)$ is the temperature of the cell, $SOC(t)$ is the SOC of the cell, and $f_{\text{loss}}(\ldots)$ is a function which calculates the energy loss of the cell at time t and it is very difficult to determine. The energy remaining in a cell at a particular C-rate that has been subjected to an arbitrary cycle is:

$$E_{R\text{-}C_x}(t_0) = E_R(t_0) - \int_{t_0}^{t_{\text{end}}} f_{\text{loss}}(v(t), I_x, T(t), SOC(t))\, dt. \tag{1.4}$$

where t_{end} is the time at which the SOC would be 0%. The total amount of energy available in a cell at a particular C-rate is defined by (1.4) evaluated at $t_0 = 0$:

$$E_{T\text{-}C_x} = E_{R\text{-}C_x}(0) = E_R(0) - \int_0^{t_{\text{end}}} f_{\text{loss}}(v(t), I_x, T(t), SOC(t))\, dt, \tag{1.5}$$

The SOH of a cell will be defined as the ratio of the total amount of energy that can be delivered by a cell at a particular C-rate to the total amount of energy that could have been delivered by the same cell at the same C-rate when it was new:

$$\text{SOH} = \frac{E_{T\text{-}C_x}}{E^{\text{new}}_{T\text{-}C_x}} \times 100\%. \tag{1.6}$$

The definitions above for SOC and SOH are energy based definitions and there are many other ways to define them. The research area of accurate SOC and SOH estimation is very active, but outside the scope of this thesis.

1.2 The importance of battery management

Electrochemical energy storage systems release electrical energy as a consequence of chemical reactions that take place inside of cells. Unfortunately, individual battery cells have restrictive voltages which is a result of their chemical composition. For example, one of the most established chemistries, lithium manganese cobalt oxide cells, commonly known as NMC, cycles between 2.5 V and 4.2 V [16]. In [17], they report on a lithium vanadium fluorophosphate cell which was cycled between 3.0 V and 4.5 V. A lead acid cell will cycle between 1.75 V and 2.1 V [18]. As it stands, electrochemical cells will be low voltage devices. Furthermore, these cells are limited in their capacity due to their physical size. The most popular cylindrical cell on the market today is the lithium-ion 18650 cell, a cylindrical cell with a diameter of 18 mm, and a length of 65 mm. They now have capacities greater than 3 Ah. In order to truly overcome the voltage and capacity limitations of small electrochemical cells, most applications will connect several cells in series and in parallel to create a battery pack of sufficient capacity with the appropriate voltage and current ratings. Battery cells of the same chemistry and impedance connected in parallel will easily share the load current and maximize the amount of energy delivered to the load from the available energy stored in the cells [19]. However, this is only possible because the cell voltages of battery cells of the same chemistry are theoretically identical. It is impossible to connect cells of different chemistries in parallel and achieve the best performance from all cells because each battery chemistry will have its own unique output voltage for a given capacity, temperature, and current value. Battery cells connected in series are limited by the weakest cell [20], thus a single cell in a series string of cells can become fully charged before the rest of the pack and continuing to charge the pack will result in overcharging of one or more cells, which can lead to a catastrophic failure of the entire

(a) Going... (b) Going... (c) Gone.

Fig. 1.1: Battery management failure of a RoboSimian droid at the Jet Propulsion Laboratory [21].

pack. Fig. 1.1 shows the consequences of charging a lithium-ion battery pack without proper management. It was later discovered that the power management systems were not properly enabled, leading to an overcharged failure mode of the robot's lithium-ion battery. In order to avoid failures and prolong battery pack lifetime, battery packs have integrated systems which are designed to continuously monitor the pack and ensure that the electrochemical energy storage devices are operated safely. The systems that monitor electrochemical cells and battery packs are called battery management systems (BMS's).

Battery management systems come in many different forms, with many different features. In the most general sense, a BMS should be able ensure that every cell in a battery pack is kept within its safe operating area to avoid catastrophic failure. However, this is only possible with global information about the system, which means accurate knowledge of temperature, voltage, current, and other future measurements such as pressure that may yield necessary information, throughout the entire battery pack. Furthermore, the fundamental chemical reactions that take place in commercial cells can vary over the lifetime of a battery pack due to manufacturing differences and external factors. In many situations it is impractical or too costly to install sensors everywhere to measure all of the required quantities, thus a BMS with reduced functionality is realized.

There are many different battery chemistries available on the market today and many others are the subject of intense research. In this thesis, the focus will be on the lithium-ion (Li-ion) chemistry, one of the most popular battery chemistries due to its high energy density [22], low weight [22], increasingly low cost [23], and long life [24]. Despite these many benefits, Li-ion batteries are a "Goldilocks chemistry". Temperature extremes will accelerate degradation [25], along with high currents [25] and high voltages [25]. During storage, Li-ion batteries should be kept at a reduced state of charge (SOC), to reduce the ageing effects known as "calendar ageing" [25]. Over discharging a Li-ion battery may cause the growth of dendrites which can puncture the separator between the positive and negative electrode [26], causing an internal short circuit within the cell, which can lead to thermal runaway and catastrophic cell failure. Overcharging a Li-ion battery increases the rate at which the active material is lost, in this case cyclable lithium, thus accelerating capacity fade [25]. Overcharging (Fig. 1.1) can also cause the electrolyte to oxidise at the cathode producing several types of gases which increase the internal pressure of the cell [27] and can lead to cell rupture [22, 28], another catastrophic failure mode. In summary, in order to safely extract the full energy storage potential out of a pack of Li-ion cells, they must be carefully managed with a BMS.

1.3 Parallel cell balancing

As mentioned previously, parallel connected cells of the same chemistry will self balance [22, 29]. In most applications, large packs are constructed out of series connections of parallel modules to yield the largest pack capacity [30] and the parallel modules are considered to be balanced. Although this is sufficient from the short term (a single charge/discharge cycle) point of view of a BMS, recent research has highlighted the increased degradation rates of parallel connected cells.

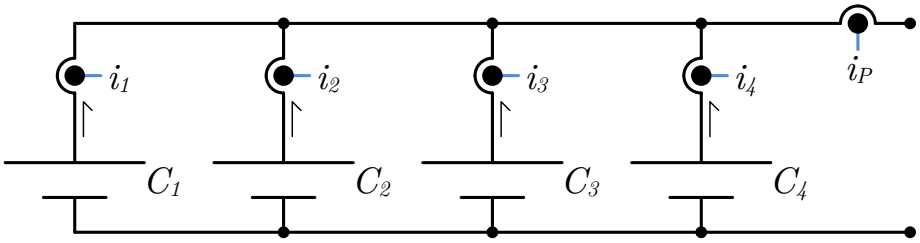


Fig. 1.2: Four cell parallel pack that was studied in [1].

Table 1.1: Charge throughput of variably aged cells from [1].

Cell	**Charge Throughput (%)**		**Relative Capacity (%)**	**1 C Discharge Capacity (Ah)**
	HEV	**BEV**		
C_1	28.6	26.3	26.2	2.94
C_2	25.1	25.6	25.5	2.86
C_3	25.5	24.8	24.7	2.77
C_4	21.9	23.3	23.6	2.65

All of the studied accelerated degradation pathways of parallel connected cells are a result of a mismatch between the impedances of those cells. Mismatches in cell impedance will detrimentally effect the ageing characteristics of a group of parallel cells [31, 32]. Therefore, any ageing mechanism which will further mismatch cell impedances will accelerate the ageing of parallel cells. For example, differences in cell temperatures linearly increase the rate of capacity loss [33] and larger C-rates will accelerate ageing of parallel connected cells [1]. The mismatch of cell impedances is amplified in chemistries that have a very "flat" SOC vs. voltage curve, such as lithium iron phosphate.

In order to illustrate the effect of C-rates on cells connected in parallel, the data from [1] will be analysed. In this study, four identical cells from the same manufacturer were variably aged and connected together to form a 4 cell parallel pack, as shown in Fig. 1.2. The capacities of the cells from the study are shown in Table 1.1, along with their calculated relative capacity. The calculated relative capacity was determined using (1.7):

$$\text{Relative Capacity of } C_x = \frac{C_x}{\sum_{i=1}^{4} C_i} \times 100\%. \tag{1.7}$$

The parallel pack was then subjected to a cycling profile from a hybrid electric vehicle (HEV) and a cycling profile from a battery electric vehicle (BEV). The HEV cycling profile had a higher C-rate on average than the BEV. During these experiments, the current from each cell was recorded and each cell's relative throughput could be calculated using (1.8):

$$\text{Relative Throughput of } C_x = \frac{\int_{\text{cycle}} |i_x|\, dt}{\int_{\text{cycle}} |i_P|\, dt} \times 100\%. \tag{1.8}$$

As shown in Table 1.1, the batteries more equally shared the load current in proportion to their capacities during the BEV cycling profile, which on average had lower C-rates, than in the HEV cycling profile. This shows that under low C-rates, variably aged cells connected in parallel will discharge and charge in proportion to their respective capacities.

1.4 Serial cell balancing

Due to the weakest cell problem, one method to prolong the life of a battery pack is to implement cell balancing in series connected cells. In [34], a summary of the current state of the art battery balancing technologies is presented. Figure 1.3 is a modified reproduction of the graphical summary presented in [34], with the additional technologies presented in this thesis highlighted.

As shown in Figure 1.3, battery cell balancing circuits can be broken down into two general categories: active and passive. Passive cell balancing circuits use a passive device, such as a switched resistor, to dissipate surplus energy in charged cells, in order to fully charge every cell in a battery pack [35, 36]. An example is shown in

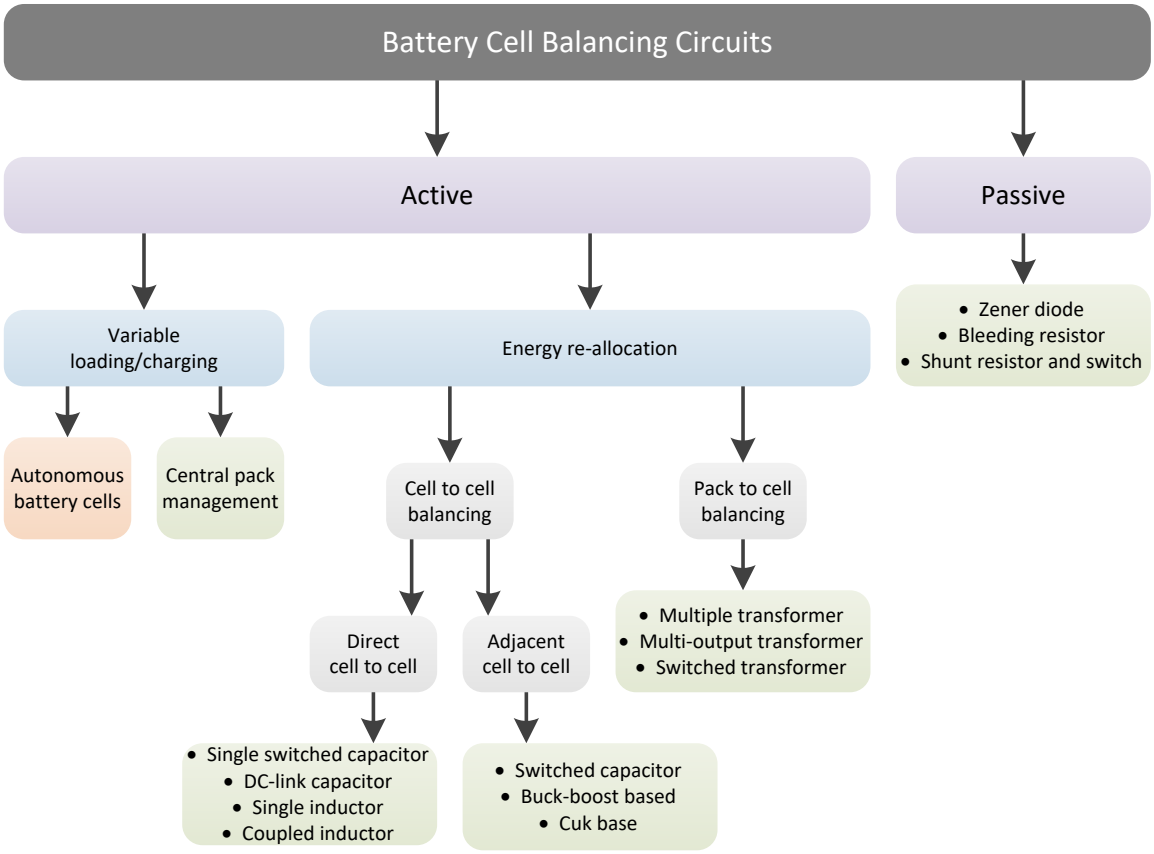
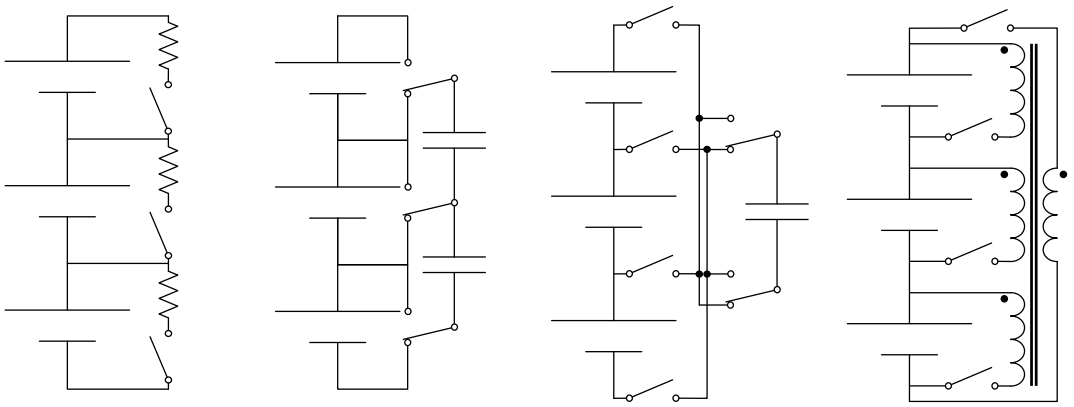


Fig. 1.3: Summary of cell balancing technologies based on the graphical summary originally presented in [34]. The area highlighted in orange (Autonomous battery cells) is a new technology presented in this thesis. The areas highlighted in blue are new categories added to the original diagram.

Figure 1.4(a). Passive cell balancing is a popular balancing technique because it is very cheap and easy to implement, and therefore, it is very scalable. However, passive cell balancing can only occur during charging, energy is wasted which is undesirable in applications where the energy source is limited, and passive heat dissipation may cause unwanted battery heating [37].

Active cell balancing circuits instead employ power electronic circuits to balance the energy between cells.



(a) Passive balancing. (b) Adjacent cell to cell balancing. (c) Direct cell to cell balancing. (d) Pack to cell balancing.

Fig. 1.4: Simplified examples of balancing circuit topologies from the literature.

1.4.1 Active battery cell balancing

Active cell balancing circuits fall within two main categories as redefined in this thesis: energy re-allocation and variable loading/charging. The most basic active cell balancing topology re-allocates energy between adjacent cells using a switched capacitor system [38, 35, 39, 40], an example of which is shown in Figure 1.4(b), the most scalable active balancing topology of those shown in Fig. 1.4. This topology has been improved with the addition of a second tier of switched capacitors [41], a central voltage source [42], and a chain structure of capacitors [43] to dramatically decrease the balancing time. Soft switching [44] and quasi-resonant switching [45] was introduced to increase the efficiency of the system. Individual voltage sensing is not required for any of these topologies, making them immune to sensor variations [43] and more easily scalable to large packs.. Even so, the balancing time is still quite considerable since it relies on voltage differences between cells to drive the balancing currents and is subject to temperature gradients across the battery pack [46].

Cell balancing time can be reduced using direct cell to cell balancing [47]. An example of this is the flying capacitor topology as shown in Figure 1.4(c). Using

a bidirectional, isolated converter for each cell, direct cell to cell balancing can be achieved by connecting the outputs of all the converters together to form a common dc bus, as demonstrated in [48]. A reduction of magnetic components can be achieved by using a buck-boost type architecture [49] and can even be reduced to a single inductor [50, 51] using many switching components.

Pack to cell balancing is also much quicker than switched capacitor balancing circuits [47]. The multi-winding flyback topology is a good example of pack to cell balancing [52, 53], where every cell has a switch and winding, and the entire pack is connected to the input of the flyback, as shown in Fig. 1.4(d). However, Fig. 1.4(d) is the least scalable of the topologies shown in Fig. 1.4 due to the need for a coupled transformer between all of the series connections, a switch for each series connected cell, and a single high voltage switch for the pack winding. Both the transformer and high voltage switch will have to scale in voltage isolation rating and kVA, respectively, as the number of cells in the series string increases. The number of transformer windings can be reduced by introducing more switching components [54–56], or the winding outputs can be implemented as simple rectifiers for more simple control [57]. In [58] a multi-winding flyback converter with added switching components is able to completely isolate a failed cell and prolong the life of the entire battery pack.

All of the topologies discussed thus far re-allocate energy within the battery pack - essentially discharging one battery to charge another. This introduces charge/discharge losses and has a maximum efficiency limited by the energy efficiency of the chemistry used. A more direct approach to cell balancing variably loads and variably charges each individual cell in a series string of batteries. This can be accomplished using a central controller to manage a large array of switches to ensure all cells are discharged at the same rate [59, 60]. A reduction in the complexity and control requirements leads to placing a small buck-boost converter on each cell and connecting all of their outputs

in series [61, 62] or parallel [63–65]. In [53], a current equalization circuit was employed to balance cells. The largest drawback of variably loaded balancing topologies, is that the power electronics must process all of the power flowing through the battery cell. Conversely, energy re-allocation topologies need only to process a fraction of the power.

In all active balancing topologies, the power electronic devices must be low cost, highly efficient, and easily integrated into a large battery pack. Recent advancements in wide band gap switching devices, whose cost is expected to decrease over time, will increase conversion efficiencies (and reduce power losses) and reduce overall system costs through higher power density [66–68] and decreased cooling requirements [69]. There are two types of wide band gap devices currently available on the market today: 1) silicon carbide (SiC), and 2) gallium nitride (GaN). The SiC devices are primarily designed for high voltage applications (650 V to 1700 V blocking voltage) and are unsuitable for most balancing circuit switches, with the exception of topologies which require a high voltage switch such as the one shown in Fig. 1.4(d). GaN devices show some promise for low voltage switching as there are GaN MOSFETs with drain to source breakdown voltages as low as 15 V currently available. However, the cost of GaN devices are still prohibitively expensive with a 30 V, 60 A device costing six times more than an equivalent silicon MOSFET of the same rating and equivalent drain to source on resistance. Therefore, for low voltage power electronic switches, silicon devices will be the primary device of choice in the near future.

1.5 Scalability of serial cell balancing

Throughout the literature, and indeed during this review, balancing circuits are commonly evaluated on the "speed" at which they balance series connected cells. However, this approach is slightly misguided for real world battery packs. Although directly related, balancing circuits should be evaluated based on the normalized current,

or C-rate, at which they can balance a string of cells. The C-rate of a given cell is defined as the current flowing through the cell in amps divided by its capacity in amp-hours. Define the maximum balancing C-rate as C_B:

$$C_B = \frac{I_{B,\max}}{C_{\text{avg}}} \tag{1.9}$$

where $I_{B,\max}$ is the maximum balancing current in amps and C_{avg} is the average capacity of the series connected cells in amp-hours. Evaluating balancing circuits with a C_B, allows a designer to better estimate the spread in cell capacities that the balancing circuit can handle and thus, the estimated lifetime of a battery pack.

Table 1.2 calculates the C_B rates for some of the balancing circuits found in literature. Note that when calculating C_B rates for switched capacitor circuits, their maximum current as reported in each study was taken. In reality, this maximum current can only be achieved with a minimum voltage difference between cells, thus they will appear more favourable in Table 1.2. In addition, the peak balancing current was taken for $I_{B,\max}$, despite restrictions on some topologies where this current is only achieved between two cells at a time, thus the rest of the pack is not able to balance while energy is being transferred.

As shown in Table 1.2, the balancing rate varied dramatically across the literature demonstrating that different C_B rates are required for different situations. However, in order to compare the balancing circuits on equal terms, the scalability of each circuit was also analysed. Scalability is an important metric as larger battery packs are being built and commissioned. The scalability of each balancing topology was calculated by normalising the component ratings of each circuit to their maximum balancing current. By doing this, all of the balancing circuits were normalised to the same balancing performance. In this thesis, there are two metrics to define scalability: 1) a normalized kVA rating, and 2) a normalized passives energy rating. Both of these quantities are

Table 1.2: Review of cell balancing currents found in the literature.

Description	**Type**	**Balancing Current (A)**	**Balancing Rate (C_B)**	**Scalability** $\lvert\mathbf{kVA}\rvert_M$	**Type** $\lvert\mathbf{J}\rvert_M$	**Ref.**
Balancing circuit used as an assisting converter	AB[‡]	2.78	NR[*]	B	II[L]	[70]
Cell to cell balancing with reduced number of switches	AB	2.13	0.14	A	III[L]	[34]
Compact, low cost, high efficiency balancer	AB	1.50	0.03	B	I	[57]
Converter per cell	AB	1.50	0.02	B	I[L]	[53]
Coupled switched capacitor	AB	0.56	0.51	A	IV	[71]
Flyback cell to pack balancer	AB	3.00	0.05	B	I	[52]
Isolated cell to cell	AB	0.21	0.05	B	II	[72]
Low cost high current balancer	AB	7.00	0.80	A	III	[73]
Modified half bridge balancer	AB	1.25	0.10	A	III	[74]
Modular balancing system	AB	0.55	0.08	B	III	[40]
Modular balancing system	AB	2.00	0.03	B	III	[75]
Multi-winding flyback transformer	AB	0.76	0.29	B	II	[76]
Multi-winding transformer	AB	1.00	0.04	B	III	[77]
Quasi-resonant zero-current-switching bidirectional converter	AB	1.00	0.10	A	III	[45]
Reconfigurable battery	AB	0.29	0.04	B	II	[78]
Resonant circuit	AB	0.49	0.11	B	IV	[79]
Shared dc-dc converter	AB	2.00	0.13	A	I[L]	[80]
ZVS switched capacitor circuit	AB	0.14	0.23	A	III	[44]
Cascaded H-bridge	VL[†]	1.80	0.82	A	I	[81]
Self-X battery	VL	20.00	1.00	A	I	[82]

[‡] Active Balancing
[†] Variable Loading/Charging
[*] Not Reported
[L] Magnetizing inductance value not reported

related to the costs of the respective components; increasing the ratings increases the costs. The normalized kVA rating for a string of M battery cells is defined as:

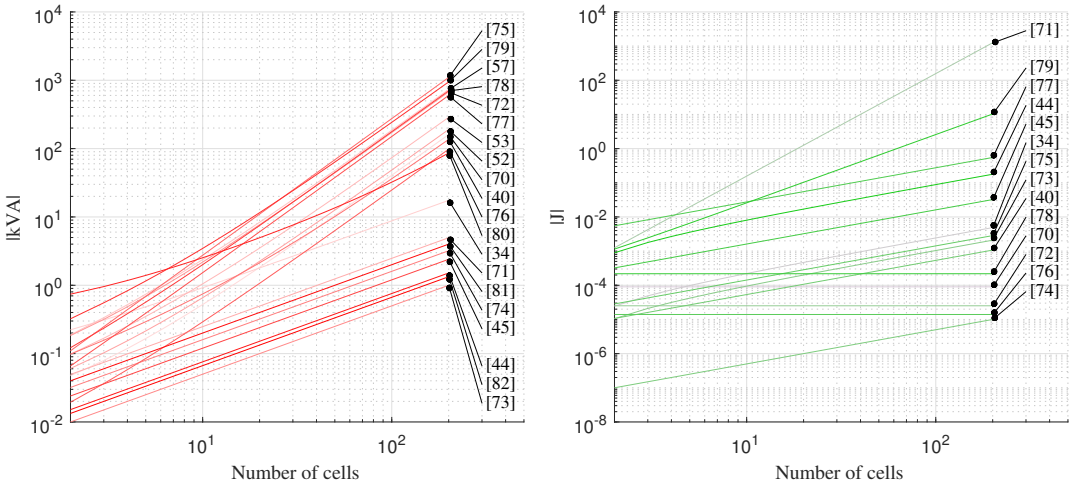
$$|\text{kVA}|_M = \frac{\text{kVA}_M^{S,T}}{I_{B,\max}}, \tag{1.10}$$

where $\text{kVA}_M^{S,T}$ is the total kVA rating of all of the switches and transformers in a balancing circuit with M series connected battery cells. In determining the current rating for each component, the root-mean-square current for every component was determined from each study, estimating this value from oscilloscope screen shots when necessary. The voltage rating of each component was determined by assigning each cell in a balancing circuit a voltage of 5 V and calculating the minimum blocking voltage required by each switch. The normalized passives energy rating was calculated with:

$$|\text{J}|_M = \frac{\text{J}_M^{C,L}}{I_{B,\max}}, \tag{1.11}$$

where $\text{J}_M^{C,L}$ is the total energy rating of all of the capacitors and inductors, including the magnetizing inductances, in a balancing circuit with M series connected battery cells.

The ratings for packs of various sizes were calculated and the results are summarized in Fig. 1.5. In Fig. 1.5(a), there appears to be 2 distinct groups of balancing circuits. In the first group, name them Type A, their kVA ratings increase the least with an increasing number of cells: [34], [71], [73], [74], [45], [80], [44], [81], [82]. The second group, name them Type B, scales worse (their kVA ratings increase the most) with the number of cells: [70], [57], [53], [52], [72], [40], [75], [76], [77], [78], [79]. The reason for these two groups lies in the use of transformers. Almost every single circuit in the second group, Type B, uses a transformer, with the exception of the topologies of [78] and [79] which use many switching components. Likewise, almost every circuit in the Type A group does not have a transformer, except for [34], [74], [80], which use single



(a) Normalized kVA of switches and transformers.

(b) Normalized energy in inductors and capacitors.

Fig. 1.5: Normalized total kVA and total energy in passives versus the number of series cells in a pack.

transformers for small groups of cells. The $|\text{kVA}|_M$ scalability type for each study is listed in Table 1.2. In conclusion, by looking at Fig. 1.5(a) alone, the most scalable balancing topologies are the ones that do not use transformers.

Fig. 1.5(b) shows the scalability of the circuits based on the energy ratings of the passives required for each of them, and should be considered in conjunction with Fig. 1.5(a). In Fig. 1.5(b) there are four distinct groups. The first group, name them Type I, are the topologies that do not require any passives: [57], [53], [52], [80], [81], [82][57], [53], [52], [80], [81], [82]. The second group, name them Type II, do not scale at all with an increase in the number of cells because the energy carrier between cells is a single passive component: [76], [72], [70], [78]. The third group, name them Type III, scales slightly with the number of cells because there is a passive component for every cell: [74], [40], [73], [75], [34], [45], [44], [77]. The fourth group, name them Type IV, is formed of topologies that do not scale well with the number of cells because their passives scale with voltage: [71], [79]. The $|\text{J}|_M$ scalability type for each study is listed in Table 1.2.

In conclusion, using the normalizations of (1.10) and (1.11) the most scalable topologies are those that are Type A and Type I: [80], [81], [82]. However, it should be noted that their are other factors that were not included in this analysis that will also effect the scalability of these circuits. For example, the intra-pack communication, sensing, and control requirements.

The next section will investigate how limited balancing current limits the amount of energy that can be extracted out of a battery pack with cells of varying capacities.

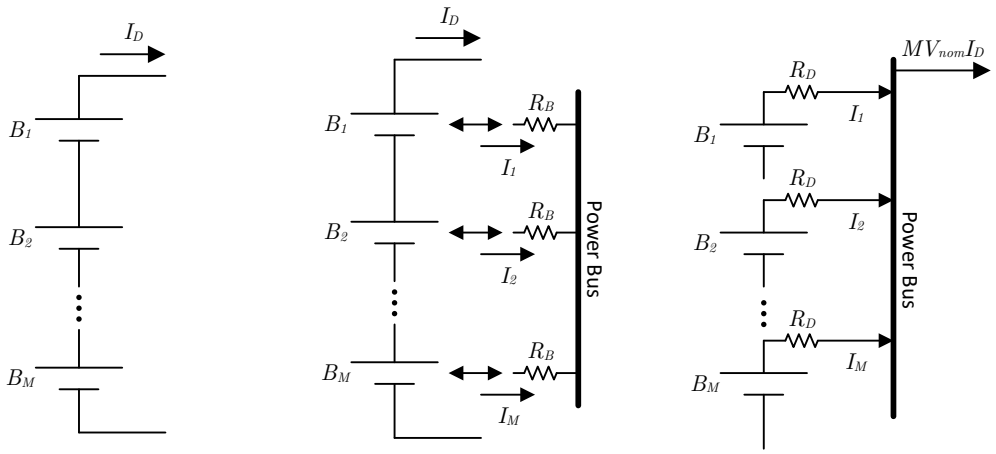
1.6 Accessing all of the energy

The preceding sections have highlighted the different balancing topologies in literature. This section will compare simplified models of three balancing topologies to see how much energy can be extracted during a single discharge. Comparing the amount of energy that is available during discharge determines how long each battery pack will last. In an application such as an electric vehicle, this directly translates into the distance that the EV can travel.

Simplified schematics of the three topologies that will be analysed are given in Fig. 1.6: passive balancing topology in Fig. 1.6(a), active balancing topology in Fig. 1.6(b), and variable loading/charging topology in Fig. 1.6(c).

1.6.1 Calculating the discharge energy

The three topologies of Fig. 1.6 will be analysed to determine the maximum amount of energy that can be extracted during a single discharge. In the following analysis, all energy is calculated in Watt-hours (Wh), C_k refers to the capacity of the k^{th} battery cell in amp-hours (Ah), T_h is time in hours (h), V_{nom} is the nominal voltage of each cell in volts (V), and M is the total number of battery cells in the series string.



(a) Passive balancing, the same current flows through all of the cells.

(b) Simplified active balancing model.

(c) Simplified variable loading/charging model.

Fig. 1.6: Simplified models of different balancing architectures during discharge.

Passive balancing

A battery pack with passive balancing is simply limited by its weakest cell. There is no way to transfer energy around, thus the amount of energy in Wh available during a complete discharge of a passively balanced battery pack is simply:

$$E_{\text{PB}} = \min_{\forall k \in [1,M]} \{C_k\} M V_{\text{nom}} \tag{1.12}$$

Active balancing

A battery pack with active balancing is able to reallocate energy between cells as it discharges, to extract more energy from the pack. In the simplified schematic of Fig. 1.6(b), active balancing is represented by current that flows in a bidirectional manner from each cell through a balancing resistor R_B, onto an "energy bus". This energy bus allows the cells to share energy for the balancing process. In this simplified model, the bus is considered ideal, the losses of the balancing circuitry are captured

entirely by R_B, and there is a limit on the balancing current: $I_k < I_{B,max}$, $k \in [1, M]$. However, there is no limit on the amount of energy that can flow through the energy bus.

When discharging a pack with active balancing, there are two scenarios to consider: (1) the energy storage is the limiting factor, and (2) the balancing circuit is the limiting factor, and thus the pack is limited by its weakest cell in addition to the energy that can be transferred to it. The point at which the balancing circuit becomes the limiting factor is determined by the discharge rate: quickly discharging the pack means that the balancing circuit will have to move more current around to maintain cell balance.

(1) *Energy storage is the limiting factor*

In this scenario, the battery pack is able to use all of the energy stored in every single cell, but has lost some energy to the losses associated with cell balancing. Equation (1.13) summarizes this observation:

$$E_{\text{AB}} = \sum_{k=1}^{M} V_{\text{nom}} C_k - E_{\text{AB,losses}} \tag{1.13}$$

where

$$E_{\text{AB,losses}} = \sum_{k=1}^{M} I_k^2 R_B T_h. \tag{1.14}$$

T_h is the time in hours that the pack is discharging. In this perfectly balanced case, this time will be the same for all of the cells, and an equation for T_h can be written:

$$T_h = \frac{C_k - \int_0^{T_h} I_k dh}{I_D} \tag{1.15}$$

$$T_h = \frac{C_k}{I_D \left(1 + I_k / I_D\right)} \tag{1.16}$$

where I_D is the discharge current of the pack. Since all cells will discharge in T_h hours, (1.13) can be re-written with all known quantities:

$$V_{\text{nom}} I_D T_h M = \sum_{k=1}^{M} V_{\text{nom}} C_k - \sum_{k=1}^{M} I_k^2 R_B T_h. \tag{1.17}$$

Finally, a constraint equation on the power bus of Fig. 1.6(b) can be written, since the power into the bus plus the losses, must always equal the power out of the bus:

$$0 = \sum_{k=1}^{M} I_k^2 R_B + \sum_{k=1}^{M} I_k V_{\text{nom}} \tag{1.18}$$

Unfortunately, we now have to solve a non-linear system of $M+1$ equations with $M+1$ unknowns (T_h, I_1, I_2, ...,I_M) with the constraint equation of (1.18). It is very difficult, if not impossible, to find an analytical solution to this problem, however, numerical methods will be used in the following section to find appropriate solutions.

(2) *Balancing circuit is the limiting factor*

The balancing circuit becomes the limiting factor when any of the I_k solved above are greater than $I_{B,\max}$. In this scenario, the battery pack is limited by the energy in the weakest cell plus the energy that can be reallocated to it during discharge. In this scenario, the equation for T_h becomes:

$$T_h = \frac{\min_{k\in[1,M]}\{C_k\} - \int_0^{T_h} I_{B,\max} dh}{I_D} \tag{1.19}$$

$$T_h = \frac{\min_{k\in[1,M]}\{C_k\}}{I_D\left(1 + I_{B,\max}/I_D\right)} \tag{1.20}$$

and therefore the total energy that can be extracted from the pack is:

$$E_{\text{AB,limited}} = \left(\min_{k\in[1,M]}\{C_k\} - I_{B,\max} T_h\right) M V_{\text{nom}}. \tag{1.21}$$

Variable loading/charging

A battery pack with variable loading/charging is able to continuously discharge all cells proportional to their capacity. The simplified model for this scenario is depicted in Fig. 1.6(c). In this model, each cell is discharged into a power bus through a resistor R_D. In a similar manner to the active balancing analysis, R_D represents all of the losses associated with the power electronics which make the active loading possible. All of the power that is put into the power bus is extracted as useful energy to power a load.

Active loaded topologies will always discharge all of the cells in a pack, thus we can write an equation for the output energy of an actively loaded battery pack:

$$E_{\text{VL}} = \sum_{k=1}^{M} C_k V_{\text{nom}} - E_{\text{VL,losses}} \tag{1.22}$$

where

$$E_{\text{VL,losses}} = \sum_{k=1}^{M} I_k^2 R_D T_h. \tag{1.23}$$

T_h is simply the amount of time to discharge a cell with I_D whose capacity is the average capacity of the pack:

$$T_h = \frac{\text{avg}_{k\in[1,M]}\{C_k\}}{I_D} \tag{1.24}$$

Similarly, the current out of each cell is adjusted by the average capacity:

$$I_k = \frac{I_D C_k}{\text{avg}_{k\in[1,M]}\{C_k\}}. \tag{1.25}$$

1.6.2 Comparison

The amount of energy that can be extracted during a single discharge of a passively balanced pack, actively balanced pack, and variably loaded/charged pack will now be compared for various pack configurations and discharge rates. Table 1.3 lists the parameters and their respective values used in this study. The values of R_D and R_B were selected by first surveying the MOSFETs available from an online retailer, Digikey, with the following filters applied: a drain to source voltage rating of 20 V, in stock and active, silicon MOSFET technology, N-Channel FET type, and cut tape packaging to remove duplicate part numbers. The collected data is shown in Fig. 1.7, along with a best fit curve to the data. The equation for this best fit curve is shown in (1.26). Equation (1.26) does not follow an inverse square relationship, as might be expected due to the squared relationship between power and current through a resistor: $P = I^2R$. This is because as the devices handle more current they physically get larger and therefore, they are able to dissipate more power. This is also shown in Fig. 1.7, where the maximum power that can be dissipated by each device is also plotted. When fitting a curve to the maximum dissipation power, the power is proportional to the current to the power of 0.579. This value is lower than the theoretically expected value of $1/1.241 = 0.806$, the inverse slope of (1.26) on a log-log plot, which indicates that with increasing current requirements, MOSFETs should be increasingly over rated for the same safety factor. The current rating for R_D and R_B was taken as two times the maximum current that could be seen by each device; that is two times 50 A and 1 A, respectively.

$$R_{DS\text{-}on} = 254.1 I_{DS\text{-}\max}^{-1.241} \text{ m}\Omega \tag{1.26}$$

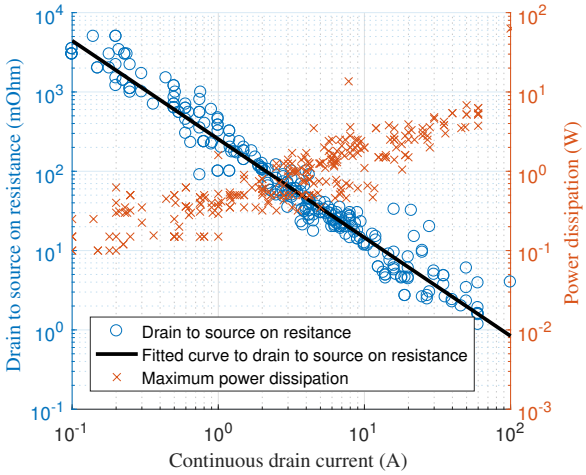


Fig. 1.7: Drain to source on resistance and maximum power dissipation for various available MOSFETs from Digikey.

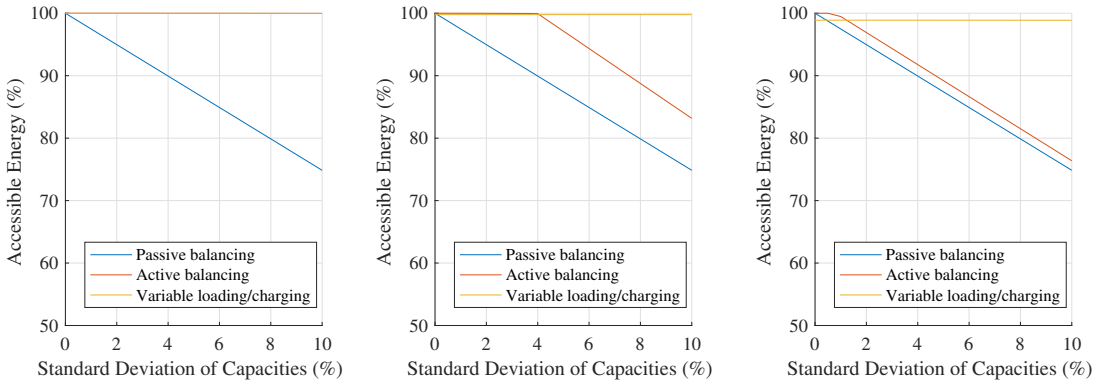
Fig. 1.8 plots the percentage of accessible energy versus the standard deviation of capacities in the pack, for three different discharge currents.

Table 1.3: Values used to compare three cell balancing strategies.

Parameter	**Value**
V_{nom}	3.6 V
R_D	0.8 mΩ
R_B	108 mΩ
$avg_{k\in[1,M]}\{C_k\}$	10 Ah
σ_{C_k}	0.0 to 1.0 Ah
M	100 cells
I_D	1 A, 10 A, 50 A
$I_{B,\text{max}}$	1 A

1.6.3 Discussion

Cell to cell capacity variation is inescapable in large battery packs as shown in [83] and [84]. Fig. 1.8(b) shows that even with a small standard deviation of 1%, it is beneficial to use any type of active balancing circuit to take advantage of the full energy storage potential of a large battery pack. Although the analysis above does not seem to favour



(a) 1 A (0.1 C) discharge current.

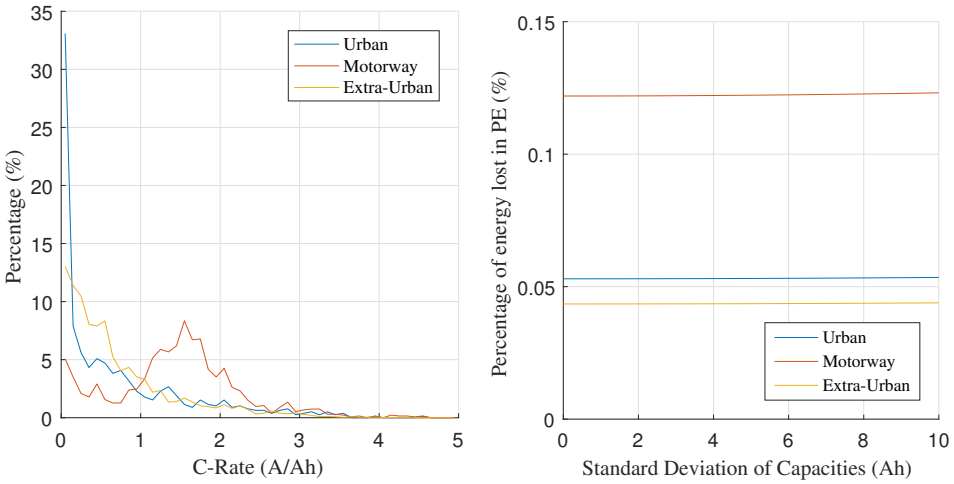
(b) 10 A (1 C) discharge current.

(c) 50 A (5 C) discharge current.

Fig. 1.8: Accessible energy under different discharge currents for the three balancing topologies of Fig. 1.6.

the proportional discharge topology, in a real application there would be a variable C-rate over time. Fig. 1.9(a) shows the percentage of time spent at different C-rates during various ARTEMIS drive cycles. In order to generate this plot, the ARTEMIS velocity profile was converted to a current profile as described in Appendix B of [85] for the urban and motorway drive cycles, and [86] for the extra-urban drive cycle. The absolute value of the resulting currents was taken, and converted to a C-rate to result in a maximum C-rate of 4.51 C. This maximum C-rate is the maximum C-rate of a Tesla Model S P100D [87].

Using the plots of Fig. 1.9(a), the amount of energy lost in the power electronics of the variable loading/charging battery pack can be determined for the three drive cycles. The amount of energy lost was calculated by calculating the efficiency of the variable loading/charging battery pack for all C-rates between 0 and 5 and for all standard deviations of cell capacities. Then, for each drive cycle and standard deviation of cell capacities, the percentage of time spent at each C-rate was multiplied by the efficiency of the pack at that C-rate and standard deviation of cell capacities. Finally, these multiplied values were summed over all of the C-rates to determine a "weighted efficiency" of the variable loading/charging topology for each drive cycle. From this



(a) Percentage of time spent at different C-rates during two ARTEMIS load profiles.

(b) Percentage of the pack energy lost due to the power electronics of the variable loading/charging pack for three ARTEMIS load profiles.

Fig. 1.9: Applying the variable loading/charging topology to the ARTEMIS drive cycle.

value, the percentage of the energy lost is simply 1 minus the weighted efficiency. The result of this analysis is shown in Fig. 1.9(b).

The percentage of the energy lost in the power electronics for the variable loading/charging topology is quite low under the three ARTEMIS drives cycles, which indicates that despite its relatively low performance at high C-rates (Fig. 1.8(c)), it can still be a viable topology for automotive applications. Likewise, the same analysis could be done for the limited active balancing topology, since at low C-rates the pack could be balancing any unbalance which was the result of a high C-rate event. This analysis is non-trivial, but it can be assumed that it will slightly outperform the proportional discharge pack. In either case, based on this analysis, as soon as there is a standard deviation of more than 1.0% in the capacities of the cells within a battery pack, using a proportional discharge battery pack topology will yield an effectively larger pack for all driving conditions, and therefore, more driving range.

In the simplified models presented here, only the conduction losses of the MOSFETs that would implement the balancing circuitry are taken into account. This was done as

they represent all of the losses of an ideal variable loading/charging topology. However, as will be shown in Section 3.2.3, a practical variable loading/charging topology has other losses that must be accounted for. Likewise, the simplified model of the active balancing battery pack does not take into account any system losses, such as losses in the active balancing network which would arise from the additional cabling needed to physically get energy around the pack. Despite this simplification, the results in this section are useful to quickly analyse that variable loading/charging topologies are worthwhile for further exploration.

In [84], Schuster et al. analysed 484 new and 1908 aged lithium ion battery cells to determine their spread in capacity over time. During their analysis they removed outlier cells. The cells used in the study had previously been used in electric vehicles and the aged cells came from two separate vehicles. They found that the standard deviation of new cells was 0.8%, in the aged cells from one vehicle the standard deviation was 2.25% after 124 equivalent full cycles, and from the second vehicle it was 1.57% after 174 equivalent full cycles. The average cell capacity in the aged cells was degraded by 3.0% and 6.1%, respectively. In both of these scenarios, the cells were far from their end of life and yet they both would have benefited from active balancing or variable loading/charging to increase their respective vehicle's range.

1.7 Second life lithium-ion batteries

The previous section derived a method to quickly determine how much energy can be extracted from a pack of cells of varying capacities during a single discharge. This analysis is extremely relevant in the growing market of second life lithium-ion batteries, whose capacity distribution will be much larger than first life cells due to variable ageing.

Second life applications of lithium-ion batteries are growing because they are economically feasible [88] and the recycling of lithium-ion batteries into raw materials is currently not economically feasible [89, 90]. Furthermore, governments such as the government in the United Kingdom require producers and vendors of batteries to pay for waste battery collection, treatment, recycling, and disposal [91]. The fees which these governments collect are passed on to the battery recyclers who use the funds to finance the expensive battery recycling operations. However, battery recyclers and producers are becoming more incentivised to find alternative methods to recycle lithium ion batteries, because they are the most expensive chemistry to recycle. Conversely, lead acid battery recycling is very easy and low cost, where 70% by weight of lead acid batteries sent for recycling is recoverable as valuable lead that can be resold onto the market [89]. Recently, there have been announcements from Nissan [92], BMW [93], and GM [94], who are all experimenting with energy storage systems using batteries recovered from their EVs and HEVs. In the automotive industry, packs from EVs and HEVs are replaced when their SOH reaches 70% to 80% [95], which is the SOH of the weakest series connected module in a pack. Thus there are many cells remaining in these large packs that are prematurely going to waste.

1.8 Practical considerations of large battery packs

Battery management systems do not scale well in large battery packs. As the number of cells increase, an increased amount of cabling is required for all of the sensors. If a pack employs one of the cell balancing circuits of Section 1.4, even more cabling is required to control the gating signals of the power electronic components. Furthermore, in high voltage packs, cell voltages must be measured with the accuracy of millivolts when differential cell voltage measurements can have a common mode offset of hundreds of volts.

A reduction in the amount of cabling within a pack can be reduced by locating a sensor and communication device physically close to the device being measured. The communication device can use a common bus communication network such as a Controller Area Network bus (CAN bus) to transmit information around the pack, which requires less wiring than a wire to every sensor. Cabling can be further reduced by implementing communication devices that use power line communication techniques [96]. Wireless intra-pack communication networks have also been studied as a means to reduce cabling [97, 98], however, the environment within the battery pack presents unique challenges due to all of the reflective surfaces (cans of batteries, metal enclosure of packs, etc.) that affect the quality of the radio signals [98]. A wireless communication medium has also been proposed to implement advanced cell level monitoring using impedance spectroscopy [99].

Wireless communication and power line communication techniques still do not provide an accurate and reliable enough solution to drive the gating signals of power electronic devices. In [99], the authors developed their own triggering mechanism in hardware and software that reduced their timing jitter to 1 μs. Although impressive, this is still not good enough for all applications. A method to simplify the distribution of many gating signals within physically large systems is an active research area of modular multi-level converters (MMCs). In order to address this issue, increasingly decentralised control schemes have been introduced [100, 101] where the gating signals for the power electronics components are generated locally. However, all of these solutions still require a centralised controller for global synchronisation.

Completely decentralized synchronisation of gating signals across multiple power electronic converters has yet to be achieved, however, a solution to this problem can be found in the theory of Kuramoto oscillators [102]. Kuramoto oscillators were first proposed by Yoshiki Kuramoto in 1975 to model systems of coupled oscillators who are

able to synchronise despite differences in phase and natural frequency: pacemaker cells in the heart, flashing fireflies, chirping crickets; to name but a few [103]. Kuramoto oscillators can be modelled with:

$$\dot{\theta_k} = \omega + \frac{K}{M} \sum_{i=1}^{N} \sin\left(\theta_i - \theta_k\right), \tag{1.27}$$

where θ_x is the phase of the x^{th} oscillator, ω is the average frequency of the system, M is the number of oscillators in the system, and K is the controller gain of the system and can be interpreted as the coupling strength between oscillators. For a sufficiently large K, the oscillators will synchronize [102]. The study of Kuramoto oscillators has been a very active and fruitful area of research with many unexplored avenues and applications [103, 104].

In a power electronics system, the oscillators are the gating signals of the converter which can have locally generated gating signals. By introducing some form a coupling, gating synchronisation can be achieved. Therefore, a global synchronization signal to each converter is not required, simplifying the design of systems with physically disparate switching devices.

1.9 Summary and thesis outline

Electrical energy storage will play a crucial role the in future of energy systems [105]. As battery packs get larger, it is crucial to have intelligent and efficient BMS's in place to properly manage and utilize the expensive electrical energy storage devices that make up the pack. One of the main roles of any BMS is cell balancing of series connected cells. An unbalanced pack will be limited by its weakest cell, thus limiting the overall performance of the pack by trapping the unused stored energy of the healthier cells.

The full energy storage potential of large battery packs can be unlocked with active balancing and variable loading/charging.

Actively balanced packs will still be limited by their weakest cell when a pack degrades. Therefore, variably loading/charging a series string of battery cells is the only way to ensure every joule of energy storage potential can be utilized throughout the entire lifetime of a pack. The rest of this thesis will focus on the author's research into variable loading/charging topologies and control algorithms. It is broken down into two main projects: the intelligent battery and the smart cell.

A variable loading/charging battery pack is introduced in Chapter 2 and it presents the design of a an intelligent battery with hot-swappable modules. Chapter 3 summarizes the simulation and experimental results of the intelligent battery.

The intelligent battery uses a centralised controller to manage the entire battery pack, which requires significant hardware overhead for intra-pack communication. To address this issue, the concept of a smart cell, having no communication bus, is presented in Chapter 4. This chapter focuses on the theory behind decentralised battery management. Chapter 5 presents simulation and experimental results which confirm that decentralised battery management is possible.

The thesis concludes with Chapter 6, where the major contributions of this work are summarized and a number of exciting avenues of research and development are proposed.

Chapter 2

Intelligent battery system design

The main goal of building an intelligent battery pack was to create a research platform where new battery management ideas could be tested on a real system composed of any type of electrical energy storage elements. In this chapter, the main mechanical and electrical design features of a research grade intelligent battery pack are discussed. The designed pack has 24 hot-swappable modules, can be configured with up to 192 battery cells, and is integrated with 25 ARM Cortex M4 micro-controllers with floating point units.

2.1 Design requirements

The general design requirements for the intelligent battery were as follows:

- Power and capacity rating large enough to power medium sized (around 1 kW) household loads.
- Easy cell replacement, so that a new battery pack would not have to be built for every cell configuration.
- Mechanically sound so that it could function as a demonstrator unit at conferences and trade shows.

Table 2.1: Specifications of the intelligent battery pack.

Description	Value
Nominal output voltage	48 V
Maximum output current	25 A
Maximum charging current	25 A
Number of modules	24
Maximum number of 18650 cells	192
Maximum cell voltage	5 V

- Module level control, meaning the energy in and out of every series connected module can be controlled.

Using the above design requirements, the electrical specifications of the intelligent battery were set, and are listed in Table 2.1. The intelligent battery pack has 2 kWh of energy storage when fully populated with 3.6 V, 3 Ah battery cells. Its maximum rated output power is 1.2 kW. Therefore, to achieve higher C-rates, fewer cells can be populated.

2.2 Mechanical design

The mechanical design of the intelligent battery was developed to deliver a platform where individual cells can be easily replaced. This enables users of the system to easily reconfigure the battery pack with different energy storage elements. In addition, each series connected energy storage element is contained within a module, which can be physically removed from the battery pack. The module and pack electronics were designed so that the modules can be hot-swapped: they can be removed from, and replaced into, the battery pack while it is operating.

The electrical details of the intelligent battery pack are discussed in Section 2.3.

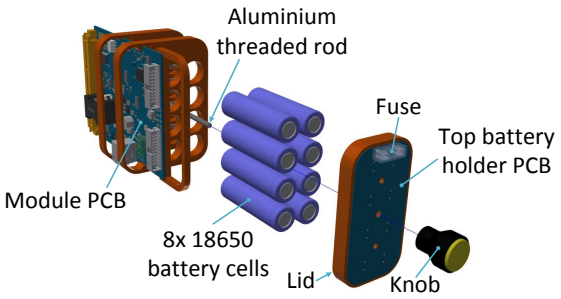


Fig. 2.1: An exploded view of a module of the intelligent battery.

2.2.1 Module design

The intelligent battery pack is comprised of 24 individual modules. Fig. 2.1 shows an exploded view of a single module of the intelligent battery pack. Each module is capable of housing up to eight 18650 battery cells. The battery cells are all connected in parallel, thus each module emulates one large cell.

The modules are constructed out of printed circuit boards, 3D printed parts, and fastening hardware. A module measures 157 mm deep, 78 mm wide, and 106 mm tall, overall.

Easy cell exchange is achieved with spring loaded contacts mounted on PCBs, which are mounted onto the 3D printed parts. The spring contacts are rated at 6 A per cell. As shown in the exploded view, a knob is used to mechanically fasten a "lid" onto the battery cells. This lid is made up of a 3D printed part, and the "top battery holder PCB" (see Fig. 2.1). The lid connects all of the positive terminals of the cells together and is where the module's safety fuse is located. The knob has an aluminium insert which makes contact with a trace on the PCB, electrically connecting the positive terminals of the batteries to the aluminium threaded rod which holds the lid in place. The aluminium threaded rod carries current out of the positive terminal of the battery, down to the "bottom battery holder PCB". The aluminium alloy used for the threaded rod and knob insert was the 6082 alloy, which has a conductivity of 3.8×10^{-8} Ω·m,

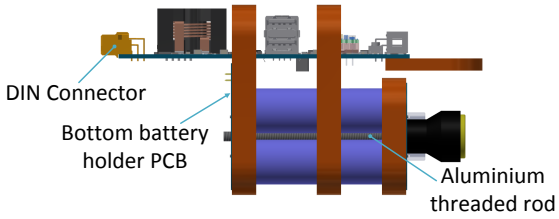


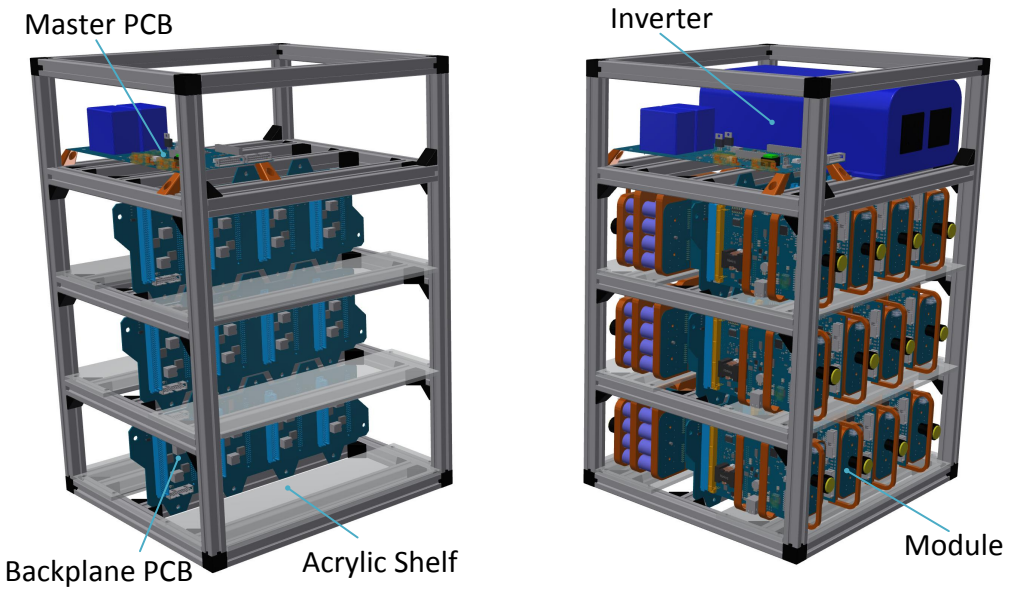
Fig. 2.2: A bottom view of a battery module. The aluminium threaded rod is visible in between the battery cells. It is used to mechanically and electrically connect the cells to the module PCB.

versus 2.65×10^{-8} Ω·m for pure aluminium. The bottom battery holder PCB connects all of the negative terminals of the batteries together and connects both the positive and negative terminals of the battery to the "module PCB". Fig. 2.2 shows a bottom view of a module with the lid and knob in place. Each module connects to a backplane PCB via a three row DIN 41612 connector.

Although designed for 18650 battery cells, this design could be easily adjusted to accommodate different sized cells by redesigning the 3D printed parts and the battery holder PCBs.

2.2.2 Battery pack design

Fig. 2.3(a) shows a 3D drawing of the battery pack itself, with no modules inserted. On its own, the battery pack consists of an aluminium frame with clear acrylic shelves that support the modules. The modules connect to the three backplane PCBs, which are visible in Fig. 2.3(a). Each backplane PCB can accommodate up to 8 modules. The modules are connected in series on the backplanes, and the backplanes are connected in series. There is a 20 pin link cable which connects each backplane to its neighbour and the top backplane to the "master PCB", which is the top most PCB in Fig. 2.3(a). The master PCB manages all of the communication throughout the pack and to the outside world. It also generates the control signals for the modules to regulate the voltage and current of the intelligent battery pack.



(a) Without modules installed. (b) Modules and inverter installed.

Fig. 2.3: 3D Drawings of the intelligent battery pack.

As designed, the battery pack itself is modular in terms of backplane PCBs. Additional backplane PCBs could be added to increase the overall voltage of the pack, up to a maximum of eight backplanes. This maximum number is limited by the number of address lines of each backplane, which is three. Likewise, fewer backplanes could be used to decrease the pack size. Any modification to the number of backplanes may require a small redesign of the master board to ensure all components can meet the minimum and maximum voltage limits of new pack configuration.

The overall dimensions of the battery pack are 330 mm deep, 360 mm wide, and 540 mm tall. Fig. 2.3(b) shows a 3D drawing of a battery pack fully populated with modules, complete with an off the shelf inverter installed.

2.3 Electrical design

The overall pack topology is introduced in this section. In addition, some aspects of the electrical design are studied more closely to highlight their purpose and/or novelty.

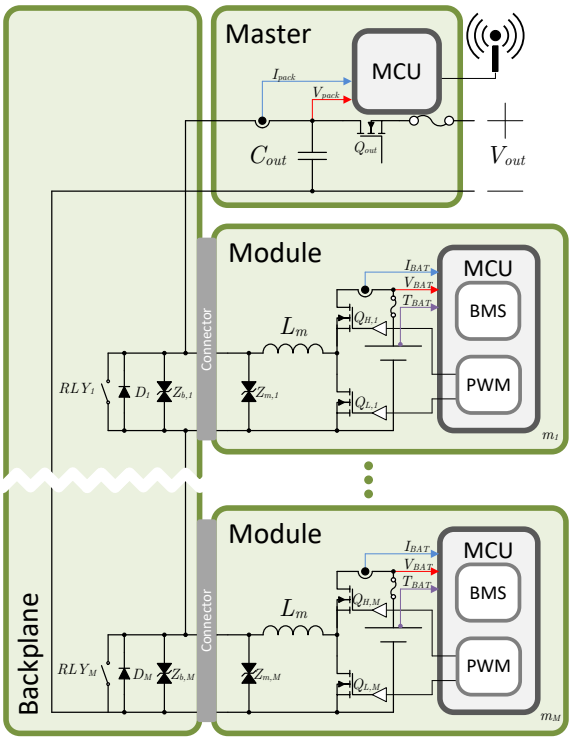


Fig. 2.4: A schematic diagram of the proposed topology to integrate battery cells of various chemistries and capacities.

2.3.1 Topology

The overall pack topology was derived from the modular multilevel converter (MMC) topology [106], using half bridge modules. Using half bridges connected to battery cells, or small battery packs, one can regulate the energy into and out of each module by adjusting its duty cycle, thereby balancing the cells. Fig. 2.4 provides a schematic of the proposed topology.

Each module consists of a half bridge switching network, voltage, current, and temperature sensors, a microcontroller, a battery cell or group of cells of the same chemistry connected in parallel, a filtering inductor, and a connector to plug the module into a backplane as shown in module schematics of Fig. 2.4.

A distributed inductor amongst the modules, L_m, was designed for the intelligent battery pack instead of a single inductor at the output for two reasons: 1) the module

inductor will be used in future work that will involve applying the decentralised battery management algorithms discussed in Chapter 4, and 2) the module inductor is also used as the inductor for the small boost converter that can provide 5 V via a USB connector on the module. Thus, when a module is extracted from the intelligent battery pack, it can still be used as a useful energy storage device itself.

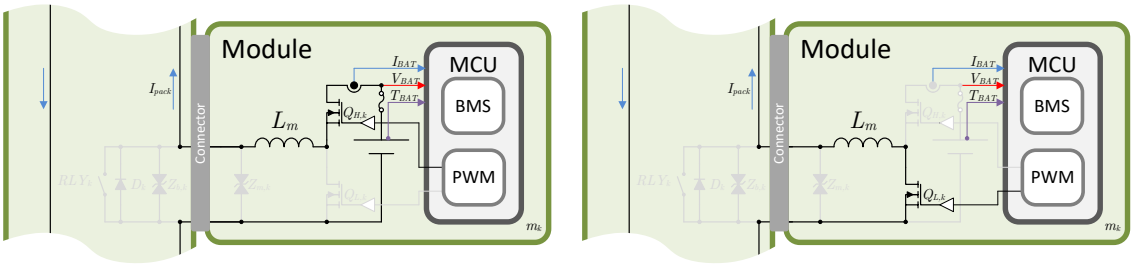
The backplane exists to provide a way to plug modules in and out of the system and to bypass missing or failed modules. As shown in Fig. 2.4, every power connection to each module has a bypass diode (D_k) and relay (RLY_k) connected in parallel. In addition to these, there are a few digital signal lines which are not shown in Fig. 2.4, but were also used to ensure safe operation of the intelligent battery. These digital signal lines were:

- Digital input to master of a hardware present signal from each module. When plugged in, each module pulled a digital line to the master low.

- Isolated digital enable signal from master to module, which was set by the master and read by the module to ensure the module could operate safely.

- Digital input signal to module from the relay, RLY_k, which was a single pole, double throw (SPDT) type. When the relay was open, it pulls a digital pin connected to the module MCU low.

The relay is controlled by the master and will only close if the master cannot get a response from the module and the hardware present signal of the module is high (inserted modules pull the hardware present signal low). The addition of the bypass diode enables the intelligent pack to continue to provide power to a load when a module is removed and is only used until the master can confirm that it can close the bypass relay. During charging, module removal will interrupt the current path, however this



(a) Active switching state 1, $S_{A,1}$. Q_H is on and Q_L is off, connecting the current of the pack, I_{pack}, to the battery cell.

(b) Active switching state 2, $S_{A,2}$. Q_L is on and Q_H is off, bypassing the current of the pack, I_{pack} around the battery cell.

Fig. 2.5: The two active switching states of the k^{th} module, $S_{A,1}$ and $S_{A,2}$.

drawback is negligible since it would not result in the loss of power to a load and charging is resumed shortly afterwards.

The master communicates with all modules, regulates the output voltage, filters the switching noise of the modules with C_{out}, and controls the module bypass relays. External control and monitoring of the entire battery pack is possible via a wifi module, which is also controlled by the master.

2.3.2 Switching states

There are a number of switching states for each module in the proposed system. They can broken down into two categories: (1) active switching states, and (2) module extraction and insertion switching states.

Active switching states

During normal operation of a module, which is defined as when a module is plugged into the system and regulating the energy into and out of its battery cell, there are two active switching states, shown in Fig. 2.5.

In active switching state 1, $S_{A,1}$, $Q_{H,k}$ is on, and $Q_{L,k}$ is off. The current path is highlighted in Fig. 2.5(a) and it shows how the pack's current, I_{pack}, flows through the battery cell. In the case of positive current, this will discharge the cell.

In active switching state 2, $S_{A,2}$, $Q_{L,k}$ is on, and $Q_{H,k}$ is off. The current path is highlighted in Fig. 2.5(b) and it shows how the pack's current, I_{pack}, bypasses the battery cell.

By varying the duty cycle, D_k, between these two states, the energy flow out of, and into, the battery cell can be controlled. By having full control of the energy flow, each module will discharge its energy storage element proportional to its capacity. In this way, every module in the entire pack will traverse its SOC curve together, at the same time, during charge and discharge.

Module extraction and insertion switching states

During module extraction and insertion, the module and intelligent battery pack must work together to ensure the proper sequence of switching states are accomplished. Each module has a dedicated "enable" signal which is driven by the master PCB. This line is driven high to indicate to the module that it can turn on and it is driven low to indicate to the module that it cannot turn on.

Module extraction

The three module extraction switching states during charge are shown in Fig. 2.6 and the three module extraction switching states during discharge are shown in Fig. 2.7. These two sets of switching states are very similar in their operation.

During either charge or discharge, right before extraction, the module can be in either one of its active switching states ($S_{A,1}$ or $S_{A,2}$), as shown by Fig. 2.6(a), showing switching state $S_{E\text{-}C,1}$, and Fig. 2.7(a), showing switching state $S_{E\text{-}D,1}$.

Right after the module is extracted, the intelligent battery enters one of the second extraction switching states from each set. During charge, it enters switching state $S_{E\text{-}C,2}$ shown in Fig. 2.6(b). In this state, the charging current is interrupted and the transient voltage suppressors are briefly activated. The transient voltage suppressor on the backplane, $Z_{b,k}$, turns on briefly to suppress the induced voltage from all of the other modules still connected to the intelligent battery. The worst case amount of energy that is absorbed by $Z_{b,k}$ is therefore:

$$E_{Z_{b,k},S_{E\text{-}C,2}} = \frac{(M-1)\, L_m I_{\text{pack}}^2}{2}, \tag{2.1}$$

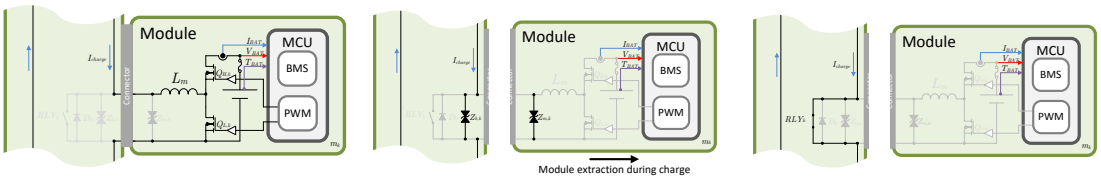
which means the amount of absorption energy increases linearly with the number of modules in the intelligent battery pack. At the same time, the transient voltage suppressor, $Z_{m,k}$, on the module suppresses the voltage induced by its local L_m, and thus will have to absorb the energy calculated with (2.2).

$$E_{Z_{m,k},S_{E\text{-}C,2}} = \frac{L_m I_{\text{pack}}^2}{2} \tag{2.2}$$

In both transient voltage suppressors, the peak current through the suppressor is the pack current, I_{pack}.

During discharge, the intelligent battery enters switching state $S_{E\text{-}D,2}$, shown in Fig. 2.7(b). In this state, the backplane's bypass diode, D_k, turns on to provide an uninterrupted current path for the load. In both situations (charge and discharge), the transient voltage suppressor on the module turns on for a brief amount of time to suppress the induced voltage caused by interrupting the current in its local inductor, L_m.

After the master has identified that a module has been removed, it pulls the enable line low, and closes the bypass relay, RLY_k, as shown in Fig. 2.6(c) and Fig. 2.7(c).



(a) module extraction during charge switching state 1, $S_{E\text{-}C,1}$. In this state, the module can be in either active switching state, right before a module is extracted.

(b) module extraction during charge switching state 2, $S_{E\text{-}C,2}$. Right after module extraction, the transient voltage suppressor, $Z_{b,k}$ briefly turns on to suppress the induced voltage created by all of the inductors, L_m, of the other modules still in the battery pack. On the module side, its transient voltage suppressor $Z_{m,k}$ will turn on for a brief amount of time to suppress the induced voltage of L_m on the extracted module.

(c) module extraction during charge switching state 3, $S_{E\text{-}C,3}$. The relay corresponding to this module, RLY_k, closes after the master board verifies that a module has indeed been extracted.

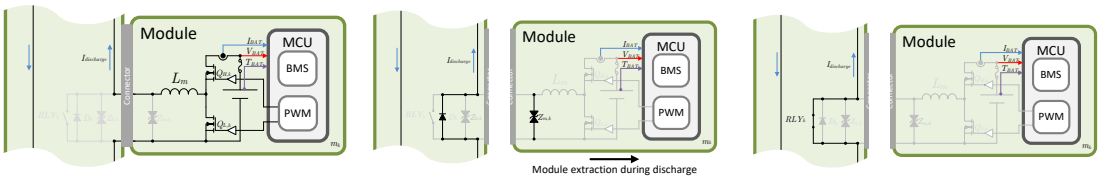
Fig. 2.6: The three module extraction switching states during charging of the k^{th} module, $S_{E\text{-}C,1}$, $S_{E\text{-}C,2}$, and $S_{E\text{-}C,3}$.

If the intelligent battery was charging, i.e. $I_{pack} < 0$ prior to the extraction, then the charging process would be resumed.

Module insertion

The three module insertion switching states are shown in Fig. 2.8. Prior to module insertion, the module is in its off state, and its corresponding bypass relay, RLY_k, is closed as shown in module insertion state 1, $S_{I,1}$, in Fig. 2.8(a).

After insertion, the master will keep the enable line low, but instruct the module to turn on, and enter a bypass mode as shown in Fig. 2.8(b). This is the second module insertion switching state, $S_{I,2}$. The module begins to share some of the current going through the bypass relay, RLY_k.



(a) module extraction during discharge switching state 1, $S_{E\text{-}D,1}$. In this state, the module can be in either active switching state, right before a module is extracted.

(b) module extraction during discharge switching state 2, $S_{E\text{-}D,2}$. Right after module extraction, the backplane bypass diode, D_k turns on to provide an uninterrupted current to the load. On the module side, its transient voltage suppressor $Z_{m,k}$ will turn on for a brief amount of time to suppress the induced voltage of L_m on the extracted module.

(c) module extraction during discharge switching state 3, $S_{E\text{-}D,3}$. The relay corresponding to this module, RLY_k, closes after the master board verifies that a module has indeed been extracted.

Fig. 2.7: The three module extraction switching states during discharge of the k^{th} module, $S_{E\text{-}D,1}$, $S_{E\text{-}D,2}$, and $S_{E\text{-}D,3}$.

In the third module insertion state, $S_{I,3}$, the master opens the bypass relay, RLY_k. During this state, the transient voltage suppressor $Z_{m,k}$ may turn on for a brief period while the current in L_m ramps to I_{pack}. In the worst case scenario, the amount of energy that $Z_{m,k}$ needs to absorb is the $V \times I$ losses in $Z_{m,k}$ as the current in L_m ramps from 0 A to I_{pack}. These losses are calculated by integrating the instantaneous power consumed by $Z_{m,k}$ during this worst case transient event. The instantaneous power of $Z_{m,k}$ is:

$$p_{Z_{m,k},S_{I,3}}(t) = V_{Z_{m,k}} \left(I_{\text{pack}} - \frac{V_{Z_{m,k}} t}{L_m} \right) \tag{2.3}$$

where $V_{Z_{m,k}}$ is the breakdown voltage of $Z_{m,k}$. Assuming the inductor is ideal, we can determine the amount of time it will take to for the inductor to ramp from 0 A to I_{pack}, using $v = Ldi/dt$, and it is $L_m I_{\text{pack}}/V_{Z_{m,k}}$ seconds. The total energy that will be

absorbed by $Z_{m,k}$ will be the integral of (2.3) between 0 and $L_m I_{\text{pack}}/V_{Z_{m,k}}$ seconds. The result is:

$$E_{Z_{m,k},S_{I,3}} = \frac{L_m I_{\text{pack}}^2}{2}. \tag{2.4}$$

The peak current during this transient event occurs right at the begining of the event, and in the worst case it is simply the pack current, I_{pack}.

In the final module insertion state, $S_{I,4}$, the master instructs the module to start gating as shown in Fig. 2.8(d). At this point, the module will be in one of its active switching states, $S_{A,1}$ or $S_{A,2}$.

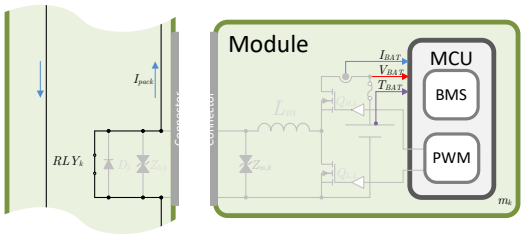
Discussion

An advantage of the switching states presented here is that the relay switches close to zero volts, with the breakdown voltage of $Z_{m,k}$ being the maximum voltage that will be seen across it. As a consequence, it can be implemented with a relatively low cost relay.

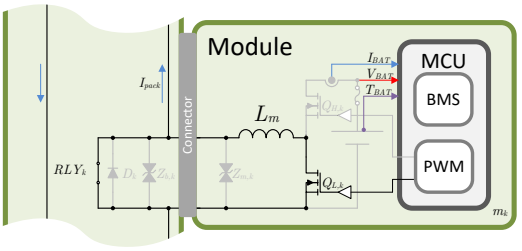
2.3.3 Microcontroller selection

There are a numerous criteria by which to select a microcontroller (MCU). For the design of the intelligent battery, the main focus was on the available peripherals and performance of the MCU. Furthermore, due to the author's familiarity with the STMicroelectronics' STM32 series of MCUs, the search space was primarily limited to this family. Consequently, the STM32F446RE was chosen as the module MCU, and to simplify the programming tasks, it was also chosen for the Master MCU as well. Some of the features of this MCU that were critical to the intelligent battery project include:

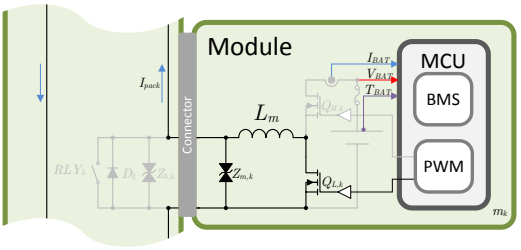
- 512 kB of flash memory, to implement large programs,



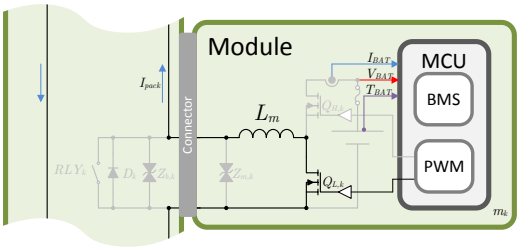
(a) module insertion switching state 1, $S_{I,1}$. In this state, the module is off, and its associated relay, RLY_k, is closed.



(b) module insertion switching state 2, $S_{I,2}$. In this state, the master turns on the module, and keeps its enable signal low. The module turns on $Q_{L,k}$, which starts to share some of the pack current, I_{pack}.



(c) module insertion switching state 3, $S_{I,3}$. In this state, the master opens the relay, RLY_k. During this state, the transient voltage suppressor $Z_{m,k}$ may turn on for a brief period while the current in L_m ramps up to I_{pack}.



(d) module insertion switching state 4, $S_{I,4}$. In this state, the master sets the enable line high, and instructs the module to start gating. After this state, the module will be in one of its active switching states.

Fig. 2.8: The four module insertion switching states of the k^{th} module, $S_{I,1}$, $S_{I,2}$, $S_{I,3}$, and $S_{I,4}$.

- ARM 32-bit Cortex-M4 CPU with FPU clocked at 180 MHz, for future work to implement battery models designed in MATLAB,
- 2x advanced timers for PWM generation with multiple output channels, to implement the PWM and timing,
- 3x 12 bit ADC that can operate up to 2.4 MSPS, and
- multiple communication interfaces including I^2C, and CAN Bus.

2.3.4 Module power supply

The ironic thing about any converter design is the need for power supplies to power the micro-controllers, analogue circuitry, and gate drivers for the converter itself. The intelligent battery pack design is no different, and perhaps an even more demanding challenge.

Every module in the intelligent battery is referenced to a different potential, which means that at some point in the circuit, isolation will be required to facilitate inter-module communication and master to module communication. In order to simplify the analogue circuit design, and to take advantage of local ADCs available on micro-controllers, the isolation point was chosen to be along the communication bus. As a consequence, each module required its own, locally referenced, 3.3 V and 12 V supply.

The decision was made to add a local boost converter to every module that would be able to provide 12 V from the local cell voltage. The design of this converter was based on Intersil's PWM step-up regulator, part number: ISL97519AIUZ. This part features an enable pin and integrated power MOSFET. The 12 V supply was connected in series to another dc/dc converter to create a 3.3 V supply. The series connection of these two power supplies was chosen so that the downstream 3.3 V supply could be a simple, low cost buck converter. A Murata Power Solutions' buck converter was

chosen as the 3.3 V converter, part number: OKI-78SR-3.3/1.5-W36H-C. This part is a drop-in replacement for a linear voltage regulator.

Finally, to reduce the amount of current drawn by each module to effectively zero when it is in an off state, the input to the boost converter, and even the battery voltage sensor, are controlled with a P-channel MOSFET.

2.3.5 Module power stage design

The module power stage consists of the module inductor L_m, the half bridge switching network Q_H and Q_L, and the gate drivers.

Gate driver design

The modules of the intelligent battery pack have high current power electronic switches that are able to handle the full rated current of the pack. These switches require dedicated gate drivers to ensure rapid switching and to increase efficiency. The one challenge with half bridge designs, such as the one depicted for the modules in Fig. 2.4, is their need for a high side gate driver for Q_H.

There are a number of solutions to drive high side switches, however, each module of the intelligent battery pack should be able to output a duty cycle of 100% for an indefinite amount of time. Furthermore, in order to operate the module's 5 V USB power supply, Q_H must be on continuously. For these reasons, the gate drivers for Q_L and Q_H are both low side drivers, powered by the local 12 V supply. Using this configuration, Q_H can be turned on indefinitely and its gate will be driven by a minimum of 7 V when it is connected to a battery cell that can provide 5 V. This gate driver design limits the the maximum voltage that can be connected to the module to $(12 - V_{th})$ volts where V_{th} is the threshold voltage of Q_H.

The gate drivers chosen for the module are from Fairchild Semiconductor, part number: FAN3122TMX. They have a peak sinking current of 11.4 A and a peak sourcing current of 10.6 A, ideal for driving large, high current MOSFETs. This gate driver also features an enable input which is held low (the gate driver is held in a disabled state) during turn on, to avoid spurious gating of the power MOSFETs while the microcontroller is booting up[1].

Q_H and Q_L selection

Q_H and Q_L need to be rated for the full current of the intelligent battery, which was designed for 25 A. However, in order to minimize losses, MOSFETs with a low $R_{DS\text{-}on}$ value should be selected, but not at the expense of a large gate charge which would increase the switching losses.

The MOSFETs need also to be able to withstand the blocking voltages that will be seen in the module. During each active switching state, $S_{A,1}$ and $S_{A,2}$, each switch will have to block the maximum rated input voltage, which was designed for 5 V.

There are numerous MOSFETs are the market today which are low cost and meet the above criteria, however, most of them have a larger than required drain to source breakdown voltage. For larger current MOSFETs, the lowest rate drain to source voltage readily available is 20 V. As a result, the switches will be under utilized throughout the intelligent battery. After a conversation with Infineon, lower voltage high current MOSFETs are not going to be manufactured because they would be just as expensive to a customer as their 20 V counterparts.

MOSFETs from Infineon's OptiMOS series were chosen for Q_H and Q_L, part number: BSC009NE2LS. These MOSFETs have a maximum $R_{DS\text{-}on}$ of 0.9 mΩ, and have a total

[1]This was a serious problem in an early prototype, as the gating signal for Q_H is connected to a pin which will output a clock signal from the microcontroller during start-up. The clock signal has a frequency of 16 MHz, and would result in a significant load on the 12 V supply, as the Q_H gate driver would be driving Q_H at this very high frequency.

gate charge of 126 nC, when driven[2] with a V_{GS} of 10 V. They are rated for a maximum current of 100 A. They are designed for switch mode power supply applications, and have an extremely small footprint of 5.15 mm × 6.15 mm in a PG-TDSON-8 package.

Switching frequency

The switching frequency of the modules will determine the output voltage ripple for given filter parameters (L_m and C_{out}). It cannot be as high as possible to minimize the output voltage ripple because the switching losses increase linearly with switching frequency. However, in the intelligent battery the modules are phase shifted with respect to each other to help minimize the output voltage ripple. Their phase shifts are determined by:

$$\phi_k = 2\pi \frac{k}{M}. \tag{2.5}$$

Using (2.5), the output voltage ripple is greatly reduced in a similar manner to how interleaved parallel converters reduce their output voltage ripple. If we assume the duty cycles of all of the modules are equal, which is a reasonable assumption when all of the modules have the same capacity, an estimate of the output voltage ripple can be calculated using the small ripple approximation in the inductors L_m and the output capacitor, C_{out}. The duty cycles of the modules are calculated with:

$$D_1 = D_2 = \ldots = D_M = D_r = \frac{V_{\text{out}}}{MV_{\text{cell}}}, \tag{2.6}$$

where V_{out} is the nominal output voltage of the intelligent battery and V_{cell} is the voltage of the cell in each module, which for simplicity, is the same for all modules. Using the current ripple diagram shown in Fig. 2.9, the peak to peak ripple current in the module inductors, $I_{p\text{-}p}$, is:

[2]The data sheet does not supply figures for $V_{GS} > 10$ V. The maximum V_{GS} is ± 20 V.

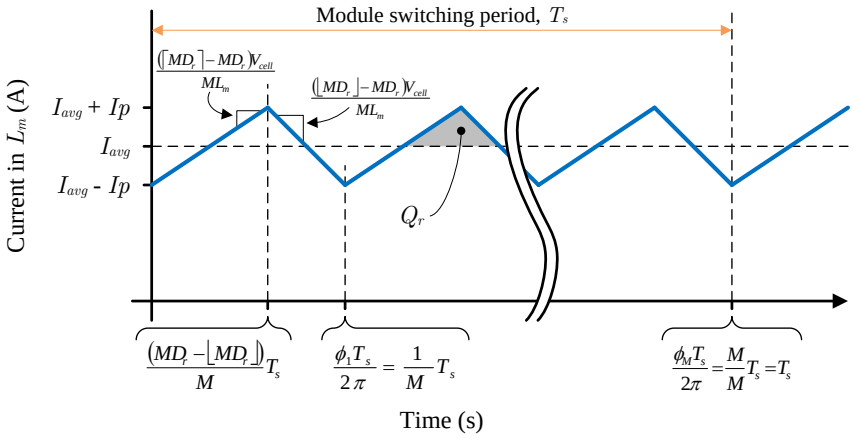


Fig. 2.9: Ripple current diagram in the module inductors.

$$I_{p\text{-}p} = 2I_p = \frac{(\lceil MD_r \rceil - MD_r)\,(MD_r - \lfloor MD_r \rfloor)\,V_{\text{cell}} T_s}{M^2 L_m}. \tag{2.7}$$

It is difficult to make a general statement about the peak to peak inductor ripple current given any system parameters and (2.7) due to the highly non-linear terms in the numerator. However, a generalization about the worst case peak to peak inductor ripple current can be found by realizing that the $(\lceil MD_r \rceil - MD_r)\,(MD_r - \lfloor MD_r \rfloor)$ term of (2.7) can be simplified to $x\,(1-x)$, where $x \in [0, 1]$. Therefore, the maximum value that $(\lceil MD_r \rceil - MD_r)\,(MD_r - \lfloor MD_r \rfloor)$ can be is 0.25. Finally, an upper bound for $I_{p\text{-}p}$ can be written:

$$I_{p\text{-}p} \leq \frac{V_{\text{cell}} T_s}{4M^2 L_m} \tag{2.8}$$

Equation (2.8) says that the *worst case* peak to peak inductor ripple current of a system operating in its optimal switching pattern according to Fig. 2.9 decreases with the inverse square of the number of modules. Keep in mind that the number of modules, M, and module duty cycles, D_r, greatly affect $I_{p\text{-}p}$. For example, a system with $M = 2$ and $D_r = 0.5$ would have an $I_{p\text{-}p} = 0$. However a system with $M = 3$ and

$D_r = 0.5$ would have an $I_{p\text{-}p} = (V_{\text{cell}} T_s) \,/\, (4M^2 L_m)$, an *increase* in peak to peak ripple current despite and increase in M.

The output voltage ripple can be estimated by assuming the ripple current of the inductor is absorbed by C_{out}. From Fig. 2.9, this is equivalent to the charge Q_r being absorbed and provided by C_{out}. Therefore, the peak to peak output voltage ripple, $V_{p\text{-}p}$, is:

$$V_{p\text{-}p} = \frac{Q_r}{C_{\text{out}}} \tag{2.9}$$

$$V_{p\text{-}p} = \frac{I_{p\text{-}p} T_s}{8MC_{\text{out}}}. \tag{2.10}$$

Equations (2.7) and (2.10) show that the ripple current and ripple voltage decreased proportionally with switching period, as expected. Using the worst case $I_{p\text{-}p}$, (2.10) shows that the worst case ripple voltage of the intelligent battery is reduced by a factor of M^3 due to the interleaved switching of the modules. By choosing module phase shifts according to (2.5), the effective switching frequency of the intelligent battery is increased. Therefore, smaller passive components can be used to achieve the same ripple specifications.

As the number of series connected modules increase, the inductor ripple current and output voltage ripple will decrease. Therefore, as the intelligent battery is scaled in voltage, the passive filtering components (L_m and C_{out}) can be reduced in size and only the voltage rating of C_{out} needs to be increased.

The switching frequency of the modules was chosen to be 20 kHz. This frequency will result in extremely low output voltage ripple and shorter control loop latency. Given the filtering components that will be designed in the following subsections, the

estimated peak to peak ripple current is $I_{p\text{-}p} = 12$ mA and the estimated output voltage ripple is $V_{p\text{-}p} = 2.7$ µV.

The ripple current and voltage are extremely low and the filtering components, switching frequency, and control loop latency requirements should be optimized in future designs. A peak to peak output voltage ripple of 0.1% (0.048 V) could be a good starting design criteria.

2.3.6 Inductor sizing

The inductance of the module level inductor was chosen to meet ripple specifications in the worst case switching conditions. The peak to peak ripple current specifications were chosen to be 20% to 40% of the maximum current rating of the battery pack, as suggested in an application note[107]. The worst case switching conditions occur during start-up, when the modules are not yet synchronized and their local battery cells are at 100% SOC. Using the small ripple approximation, the peak to peak ripple current on the module level inductors can be calculated with the following equation:

$$\Delta I_{L_m p\text{-}p} = \frac{M \cdot V_{\text{cell}} - V_{\text{out}}}{M \cdot L_m} \cdot \frac{V_{\text{out}}}{M \cdot V_{\text{cell}}} \cdot \frac{1}{T_s} \tag{2.11}$$

where M is the number of modules, in this case $M = 24$. In the worst case switching conditions, $V_{\text{cell}} = 5$ V, $V_{\text{out}} = 48$ V, and $T_s = 50$ µs. Solving for L_m, this yields an inductance range of 6 µH to 12 µH as suggested by [107]. Leaning towards the conservative side, an inductance of 10 µH was chosen for the module's inductor.

The inductor's current sizing must take into account the maximum current of the intelligent battery, plus the worst case ripple current. Using a 10 µH inductor, the nominal peak current through the inductor is 28 A. Searching available off the shelf parts, an inductor from Wurth Electronics was chosen, part number 7443641000. Its current rating is 30 A and it has a saturation current of 37 A.

2.3.7 Output capacitor sizing

The output capacitor, C_{out}, of the intelligent battery pack needs to be able to handle large ripple currents, voltages of at least $5 \times 24 = 120$ V dc, and be large enough to be connected to loads with large input capacitors without completely discharging. These requirements were met with a parallel combination of film capacitors and aluminium electrolytic capacitors. The film capacitors were chosen from Epcos' (TDK) line of capacitors designed for high frequency switch mode power supplies, part number: B32778G4107K. The capacitor chosen has a voltage rating of 450 V dc, and a capacitance of 100 µF. Two of these capacitors connected in parallel were used in the intelligent battery pack. The aluminium electrolytic capacitors were chosen from Dubilier, part number: DEA 1000 63. This capacitor has a capacitance of 1000 µF, and two of them were placed in parallel. Therefore, the total output capacitance of the intelligent battery pack was designed to be 2200 µF. This capacitance value is very large and results in a very low peak to peak output voltage ripple of 2.7 µV as calculated in a previous subsection. In a future design, the size of this capacitor would be greatly reduced to take advantage of the interleaved switching of the intelligent battery.

Using this capacitor and the module inductors, we can calculate the cut-off frequency of the output LC filter of the intelligent battery pack:

$$f_0 = \frac{1}{2\pi\sqrt{M \cdot L_m C_{\text{out}}}} = 219 \text{ Hz}. \tag{2.12}$$

The cut-off frequency of the intelligent battery pack will dictate its controller bandwidth. This value of 219 Hz means that the controller will not be able to respond extremely quickly (less than 1 ms) to load changes.

2.3.8 Transient voltage suppressor design

The energy absorption requirements of the voltage suppressors were derived in Section 2.3.2. Using those equations and the design specifications of the intelligent battery pack, the maximum amount of energy that the module voltage suppressors must absorb is:

$$E_{Z_{m,k},\max} = \frac{L_m I_{\text{pack}}^2}{2} \tag{2.13}$$

$$E_{Z_{m,k},\max} = 3.125 \times 10^{-3} \text{ J}, \tag{2.14}$$

and the maximum amount of energy that the backplane voltage suppressors must absorb is:

$$E_{Z_{b,k},\max} = \frac{(M-1)\, L_m I_{\text{pack}}^2}{2} \tag{2.15}$$

$$E_{Z_{b,k},\max} = 71.875 \times 10^{-3} \text{ J}, \tag{2.16}$$

where $L_m = 50$ µH, $M = 24$, and $I_{\text{pack}} = 25$ A.

The backplane transient voltage suppressors were chosen from Littelfuse Inc., part number: 1.5SMC24CA. This part has minimum varistor voltage of 22.8 V with a peak pulse current of 45.8 A, well within the requirements of $I_{\text{pack}} = 25$ A, and can absorb 1 J of energy. The varistor voltage was chosen based on the maximum voltage that the bypass diode, D_k, can withstand, which is 45 V. Therefore, the chosen part has a maximum varistor voltage of 33.2 V.

The module transient voltage suppressors were chosen from EPCOS (TDK), part number: B72530T0060M062. These devices have a minimum varistor voltage of 8.8 V

and can absorb up to 0.7 J of energy. Their peak surge current is 300 A. These devices were over designed to minimize failures in the prototype. The varistor voltage was chosen to be as high as possible without damaging the analogue circuitry on the module PCB and therefore, the maximum varistor voltage of this device is 13.2 V.

In addition to the transient voltage suppressor on the module, each module also has a bank of capacitors that forms part of an auxiliary 5 V dc to dc converter. The connection of these capacitors is shown as C_{5V} in Fig. 2.10. The capacitors also help absorb the energy from L_m during transient events, and could be used as a substitute for the transient voltage suppressor. In order to keep the same clamping voltage of 8.8 V, the capacitance must be larger than:

$$E_{Z_{b,k},\max} \leq \frac{1}{2}C_{5V}V_{\text{clamp}}^2 - \frac{1}{2}C_{5V}V_{\text{out-max}}^2 \tag{2.17}$$

$$C_{5V} \geq \frac{2E_{Z_{b,k},\max}}{V_{\text{clamp}}^2 - V_{\text{out-max}}^2} \tag{2.18}$$

$$C_{5V} \geq 119\ \mu\text{F}, \tag{2.19}$$

where $V_{\text{out-max}} = 5$ V in the absolute worst case scenario. However, during normal operation, $V_{\text{out-max}} = 2$ V and in this scenario the minimum capacitance required by C_{5V} is 85 µF. In the current design of the modules, $C_{5V} = 100$ µF and therefore, during normal operation the transient voltage suppressors will not be triggered, as all of the energy of L_m will be absorbed by C_{5V}.

In future designs that may not have C_{5V}, it is still more economical to introduce a transient voltage suppressor instead of a bank of output capacitors to absorb the energy of L_m. Furthermore, a bank of capacitors will also require a discharge resistor, and if not completely discharged before the next transient event, the clamping voltage may increase beyond the desired limits.

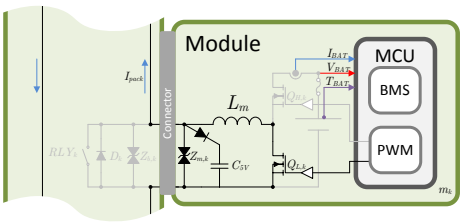


Fig. 2.10: 5 V capacitor, 5_{5V}, connection in modules.

2.3.9 Communication

Intra-pack communication is important to relay information back to the master board, which will in turn relay commands to the modules. However, the communication network should also be able to provide real time commands to maintain tight output voltage regulation. Therefore, the intelligent battery pack uses two communication paths to the modules: 1) a bi-directional, data communication bus over an internal CAN bus, and 2) a uni-directional, real time single wire communication bus from the master to the modules which synchronizes their switching actions and provides the ac component of the duty cycle, $\hat{d}$. $\hat{d}$ is the control signal from the master which is used to regulate the output voltage of the intelligent battery. Each module calculates its own "dc" value of the duty cycle, D_k, via their state of charge controllers. Every module combines D_k and $\hat{d}$ to output a switching signal that regulates the energy of their connected cell and regulates the output voltage. The details of $\hat{d}$ are explained in the subsection: "Sync and data signal".

CAN bus

CAN bus was chosen for the bi-directional, data communication bus within the intelligent battery pack, as it is an industry standard for automotive and other industrial applications. Furthermore, the CAN bus protocol is a master-less protocol, which

would enable future work on the intelligent battery that does not involve a central master board for communication.

The MCU was specifically chosen because it has a hardware implementation of two CAN bus modules. One CAN bus module is used for intra-pack communication and the other is used for external communication.

Sync and data signal[3]

The sync and data signal combines a synchronization pulse and the ac component of the duty cycle, $\hat{d}$, together into a single signal. Furthermore, it is implemented entirely in hardware, freeing up the MCUs for other tasks. Fig. 2.11 is a schematic of how the signal is created by the master and how is it decoded in the module.

At the master, the output voltage is regulated with a voltage controller, $C_v(s)$, which outputs the ac component of the duty cycle, $\hat{d}$. The master MCU uses one of its PWM modules to output a synchronization signal, as shown in Fig. 2.11. At the moment the synchronization signal goes high, the UART module transfers the value $\hat{d}$. The outputs of the UART module and the PWM module are fed through an AND gate. The output of the AND gate is the sync and data signal which is connected to all of the modules.

The module uses the sync and data signal to adjust its duty cycle and synchronize its local PWM counter with all of the other modules in the pack. The sync and data signal is routed directly into the module's UART module to receive $\hat{d}$. The sync and data signal is also routed to an OR gate, whose other input is a blanking signal from the module's PWM module. The output of the OR gate is a synchronization signal which is in phase with the master's synchronization signal. The synchronization signal

[3]Due to time constraints, initial work on the intelligent battery was supported by a consultant, FrostNet, for 36 days. The sync and data signal was developed in collaboration with FrostNet. The author originally suggested to design the sync and data signal with a variable duty cycle. FrostNet improved the design by suggesting the use of a digital signal, rather then a variable duty cycle. The author designed and implemented the hardware and overall architecture for the sync and data signal.

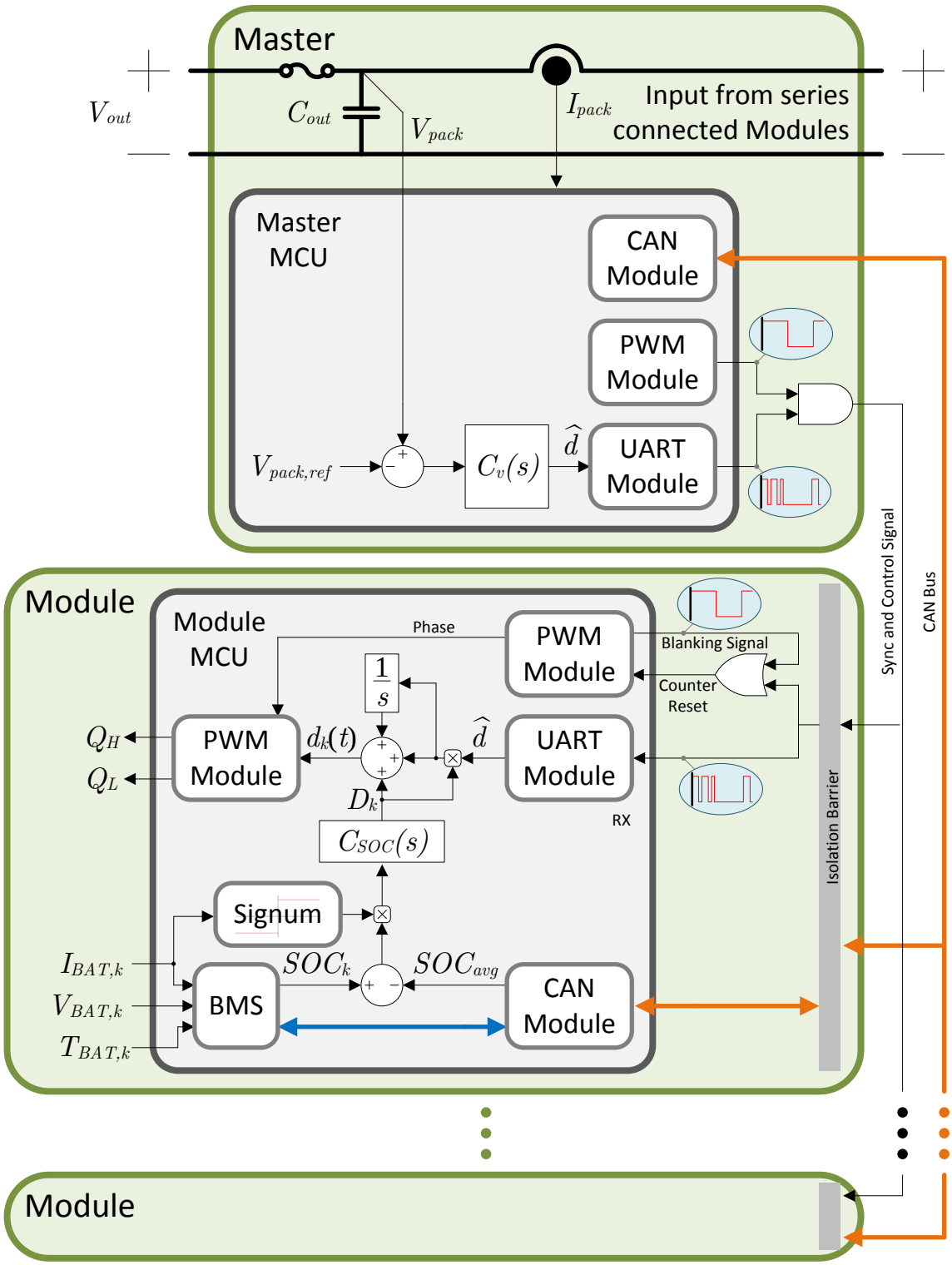


Fig. 2.11: A schematic of the intra-pack communication network in the intelligent battery pack.

is then used to reset the counter of the module's PWM module to synchronize all of the PWM modules in the pack and generate the blanking signal.

The module calculates its duty cycle according to (2.20):

$$d_k(t) = D_k + D_k\hat{d} + \int_0^\infty D_k\hat{d}\,dt, \tag{2.20}$$

which is also represented schematically in Fig. 2.11. The "dc", or slowly changing, part of the duty cycle is D_k. This value is calculated by the module's SOC controller, $C_{SOC}(s)$. The ac component of the duty cycle, $\hat{d}$, adjusts the module's duty cycle in proportion to the dc duty cycle so that cells with larger capacities increase their loads proportionally when the duty cycle increases, and visa versa with smaller capacity cells. The second term of (2.20) is the component which will vary the most in response to the master's voltage controller. The third term of (2.20) is a slow integrator which will gradually integrate any non-zero value of $\hat{d}$, so that the average value of $\hat{d}$ is zero. It is advantageous for $\hat{d}$ to be zero in instances where the connection to the master controller is lost or the master controller is suddenly reset. In both of these cases, the module's duty cycle will not change, thus avoiding any large transients at the output of the intelligent battery pack. The integrator operates on the seconds time scale, meaning it takes about 1-2 seconds for the integrator to integrate $\hat{d}$ to 0. At this rate, it does not effect the voltage or current control loops which operate at the millisecond time scale and nor does it effect the SOC control loop which operates at the tens of minutes time scale.

The module's PWM module applies any necessary phase shift and outputs the appropriate gating signals to Q_H and Q_L.

In this way, all of the PWM counters in all of the modules will be synchronized and the duty cycles of all of the modules can be updated every switching cycle which allows for tight output voltage regulation and controlled output voltage ripple. The

sync and data signal has been implemented with a digital delivery mechanism of $\hat{d}$, but it could have also been implemented with an "analogue" delivery mechanism. Instead of using a UART module to transmit the digital value of $\hat{d}$, the duty cycle of the sync signal generated by the master's PWM module could be varied depending on the value of $\hat{d}$. It would then be up to the modules to measure the duty cycle to determine the value of $\hat{d}$. The analogue method would be prone to noise and would most likely result in chattering amongst the modules. The digital delivery mechanism is more immune to noisy environments.

2.3.10 Start circuit

In the off state, the modular battery pack is completely "cold" to reduce the amount of leakage current drawn from the battery cells to effectively zero. Even the cell's voltage sensor is disconnected in the off state to minimize leakage current. The task of starting up the battery pack from this state is non-trivial and the start circuit which implements this is shown in Fig. 2.12.

The start circuit is powered by a small rechargeable coin cell to guarantee start-up. The circuit can also be powered by the first and second modules in the pack, however if these modules are missing or failed, the pack would not be able to start.

The pack is started by a user pressing the start push button. The depressed start button raises the gate voltage of $Q_{s\text{-}u}$ (start-user), so that it closes. $Q_{s\text{-}u}$ is connected to a P-channel MOSFET which controls the current flow into all of the backplane optocouplers. The optocouplers are manufactured by Toshiba, part number: TLP293(GB-TPL,E[4], and have a minimum current transfer ratio of 50%. The output of each optocoupler is connected between the gate of the P-channel MOSFET which

[4]Surprisingly, TLP293(GB-TPL,E does not contain a typo. This is the official part number.

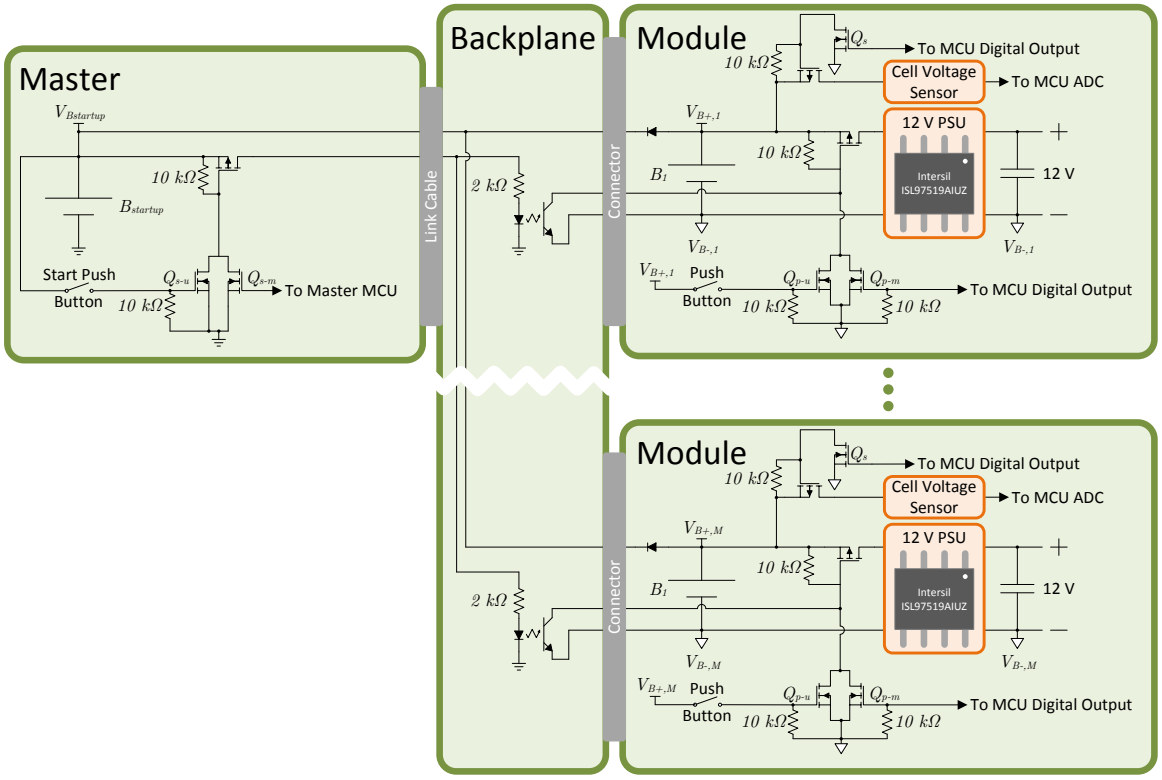


Fig. 2.12: A schematic of the start circuit used in the modular battery pack to turn on all of the modules at the same time.

controls the current flowing into the 12 V supply of a module, and the local ground point of each module.

Once on, each module will follow the start-up flow chart shown in Fig. 2.13. The first step in this start-up procedure is to turn on MOSFET $Q_{p\text{-}m}$ (psu-mcu), which keeps the module power supply on and MOSFET Q_s (sensor), which closes the P-channel MOSFET used to disconnect the module's voltage sensor from the cell. Next, the module MCUs start gating, which in turn powers the point of load converters on the master PCB, which will start-up the master MCU.

MOSFET $Q_{s\text{-}m}$ (start-mcu) is used by the master MCU to start modules that have been inserted into the backplane whilst the intelligent battery has already been turned on. MOSFET $Q_{p\text{-}u}$ (psu-user) is used by the user to turn on the module.

2.4 Scalability

Using the intelligent battery design of Section 2.3, its scalability can be evaluated in the same manner as the balancing circuits of Table 1.2. Fig. 2.14 shows an updated Fig. 1.5 with the proposed intelligent battery scalability figures added.

Using the terminology developed in Section 1.5, the scalability of the intelligent battery places it as a Type A and Type IV topology. It is not surprising that it is a Type A topology since it is based on an MMC topology, which places low voltage switching components in series to meet output voltage requirements.

The intelligent battery's classification as a Type IV topology does not tell the whole story. The Type IV classification is due to the output capacitor which exists to filter the ripple current of the inductors. The capacitor's size depends on each application's ripple voltage requirements and the capacitance required will change as the number of cells increases. As derived in (2.7) and (2.10), the worst case ripple voltage varies with the cubed inverse of the number of cells. For the same peak to peak output voltage

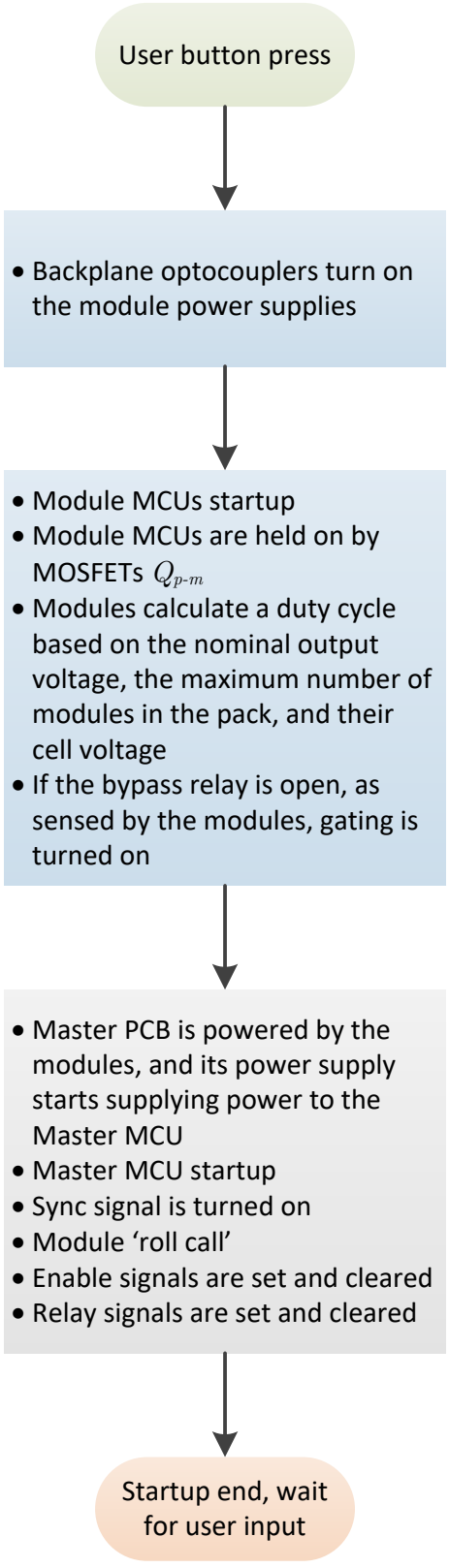
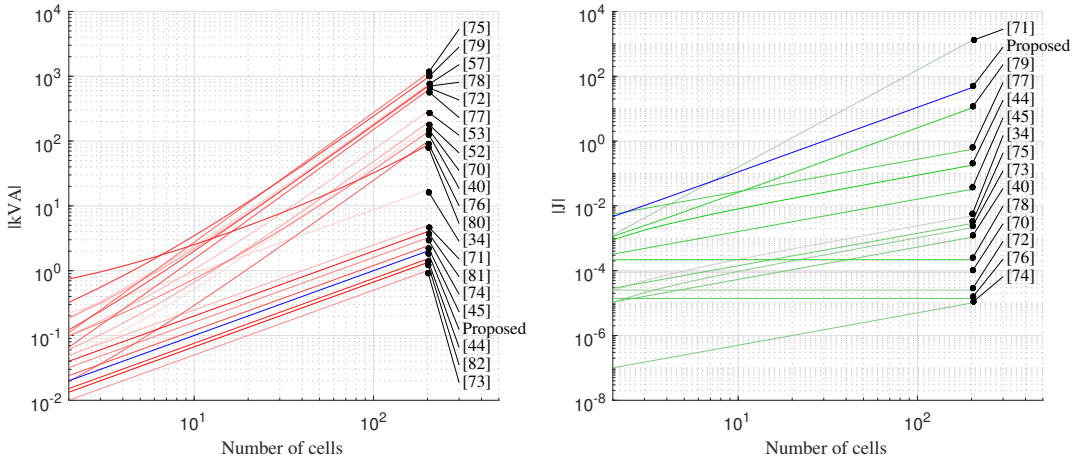


Fig. 2.13: The start-up flow chart of the intelligent battery pack.



(a) Normalized kVA of switches and transformers.

(b) Normalized energy in inductors and capacitors.

Fig. 2.14: Normalized total kVA and total energy in passives versus the number of series cells in a pack including the proposed solution of the intelligent battery shown in blue and labelled as "Proposed".

ripple, the capacitance of the output capacitor could be reduced at a faster rate then its voltage rating squared as the number of series connected cells increase. Therefore, in a practical implementation of the intelligent battery, it can be classed as a scalable, Type A and Type II topology.

2.5 Controller design

The design of the intelligent battery's various controllers is covered in this section. Most of the controllers were designed in continuous time and converted to discrete time using the bilinear transform.

A voltage controller and current controller were designed for the intelligent battery pack. In voltage control mode, the pack acts like a regulated voltage source. In current control mode, the pack acts like a current source and this mode was used when the pack was connected to a dc power supply for charging. These two modes were chosen so that the intelligent battery pack could operate easily with an electronic load when

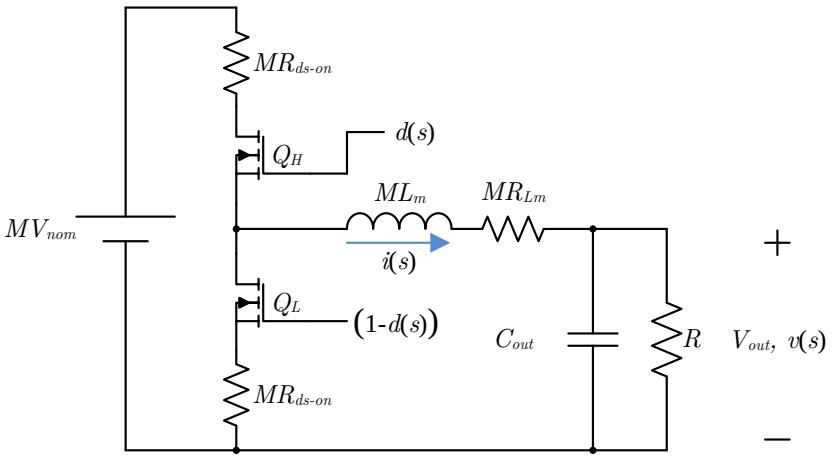


Fig. 2.15: Simplified topology of Fig. 2.4 used to derive control to output transfer functions of the intelligent battery.

discharging and a dc power supply while charging. Since the intelligent battery executes its own constant current, pseudo constant voltage charging algorithm (see Subsection 2.5.4), it can be connected to any type of dc source to charge.

2.5.1 Voltage regulation

The voltage controller is used by the intelligent battery to regulate its output voltage. In order to model the intelligent battery pack in an efficient manner for controller design, a few simplifications can be made.

Firstly, we can simplify the topology of Fig. 2.4 into a single half bridge switching network with the same output capacitance, but with a single inductor whose value is $M \times L_m$, where M is the number of modules. This simplified topology is shown in Fig. 2.15 and includes some elements to model resistive losses in the circuit. The switching frequency remains the same at $f_s = 20$ kHz, because this is the update rate of the controller. Furthermore, we can simplify the controller diagram of Fig. 2.11 to only focus on the voltage control loop, since the other controllers operate much more slowly. Using this simplified topology and the small signal approximation, the control $(\hat{d}\,(s))$ to output $(v\,(s))$ transfer function can be derived and is shown below:

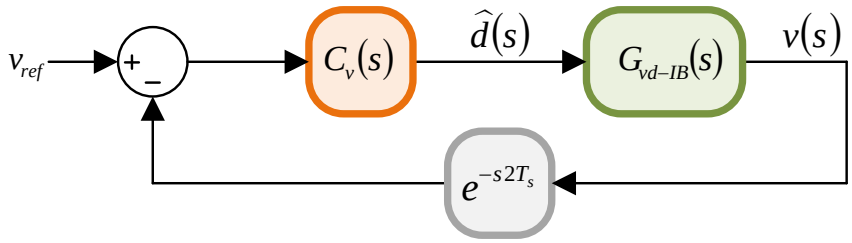


Fig. 2.16: Voltage control loop of the intelligent battery.

$$G_{vd\text{-}IB}(s) = \frac{v(s)}{\hat{d}(s)} \tag{2.21}$$

$$G_{vd\text{-}IB}(s) = V_{nom} \frac{R}{(R_{ds\text{-}on} + R_{Lm}) + \frac{R}{M} + s\left(L_m + C_{\text{out}} R\left(R_{ds\text{-}on} + R_{Lm}\right)\right) + s^2 R L_m C_{\text{out}}} \tag{2.22}$$

where $R_{ds\text{-}on}$ is the on resistance of the MOSFETs ($Q_{H,k}$ and $Q_{L,k}$), and R_{Lm} is the dc resistance of each inductor, L_m. Fig. 2.16 shows the voltage control loop of the intelligent battery pack, which includes the control loop delay in the feedback loop.

$G_{vd\text{-}IB}(s)$ is also the loop gain of the system when the voltage controller, $C_v(s)$, has unity gain. Let $T_v(s) = G_{vd\text{-}IB}(s)$ be the loop gain of the system. The bode plot of the intelligent battery system can be drawn using the parameters listed in Table 2.2, and the plot is shown in Fig. 2.18(a). However, before controller design can commence, it is important to include the delay caused by the digital control loop. Fig. 2.17 is a timing diagram showing the events that occur during the execution of the voltage control loop.

Using Fig. 2.17 as a reference, the master board of the intelligent pack takes two samples of the output voltage at T_{S1} and T_{S2} during each iteration of the voltage control loop. Two samples are taken to yield an improved measurement of the output voltage. Since the modules will be varying their duty cycles, it is difficult to choose a sample time that will always be at the peak or trough of the output voltage ripple. Ideally,

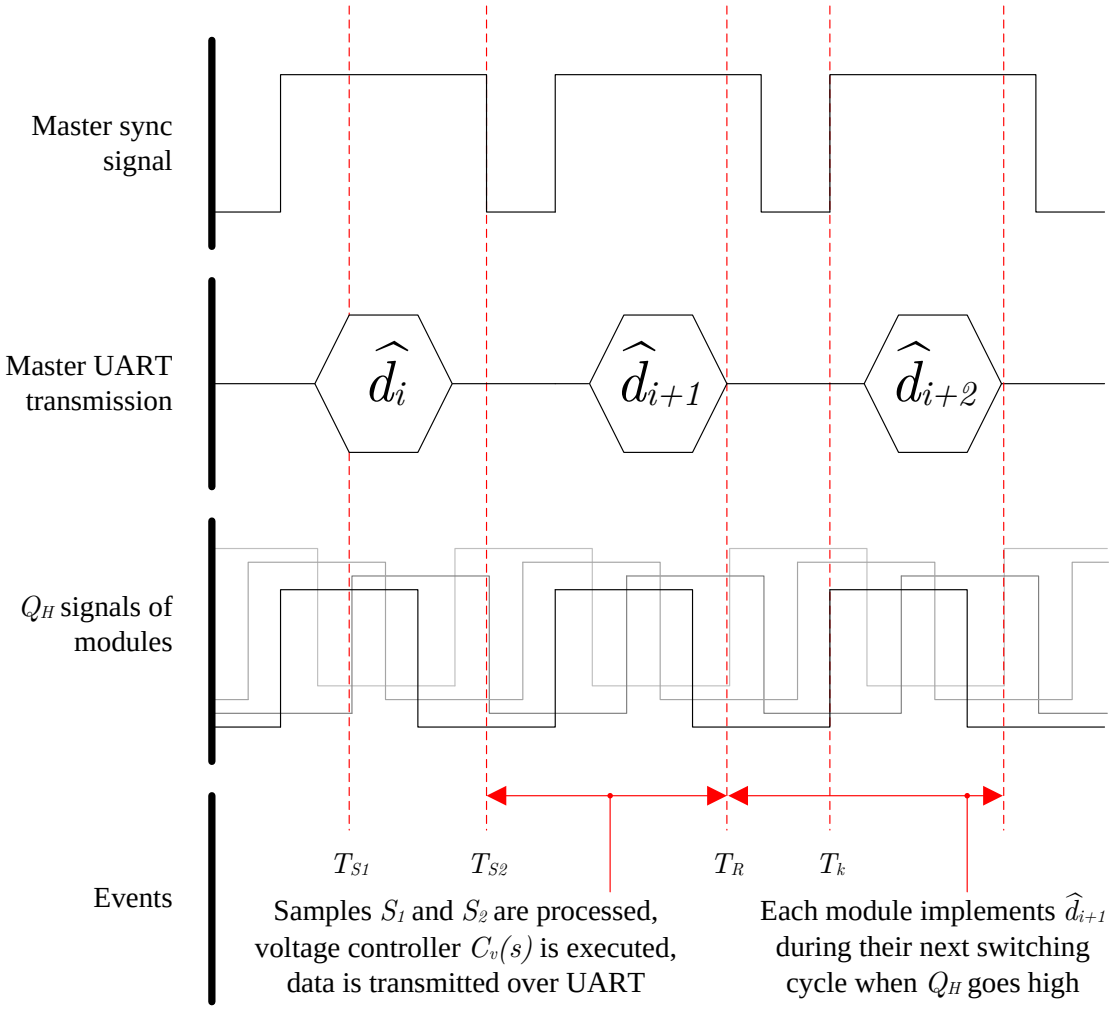


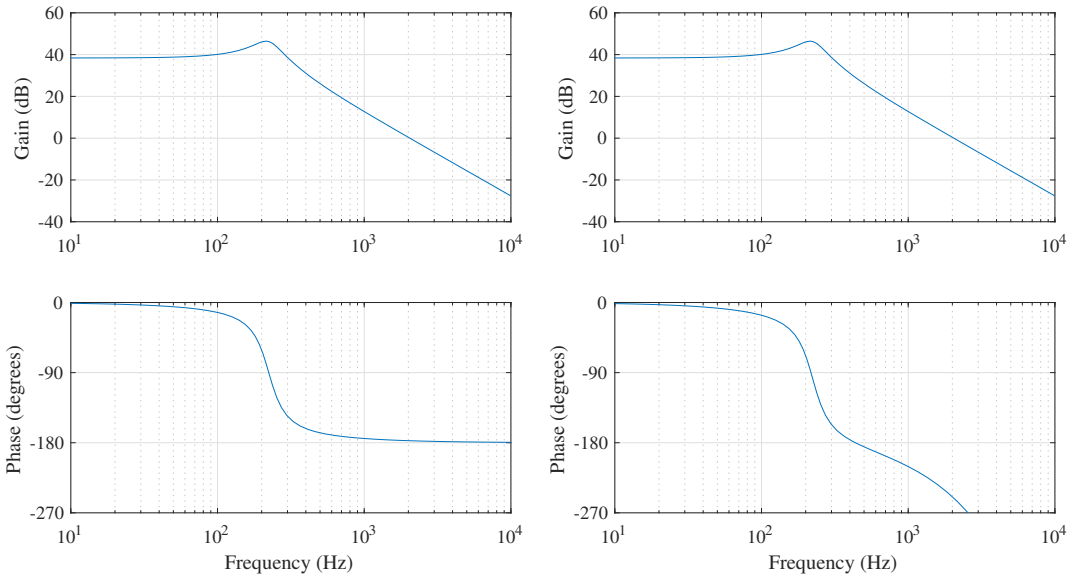
Fig. 2.17: A timing diagram of the voltage sampling and control signal. The delay between sampling the output voltage and the execution of a new duty cycle command is about 1.5 to 2.5 switching cycles, depending on the phase shift of each module.

Table 2.2: Parameters used to design the controllers of the intelligent battery pack.

Description	**Parameter**	**Value**
Module inductance	L_m	10 µH
Output capacitance	C_{out}	2200 µF
Switching frequency	f_s	20 kHz
Switching period	T_s	50 µs
Number of modules	M	24
Nominal module voltage	V_{nom}	3.6 V
Output voltage reference	V_{ref}	48 V
Digital control delay	T_{delay}	$1.5 \times T_s$
Load	R	1.92 Ω
Module MOSFET on resistance	$R_{ds\text{-}on}$	0.9 mΩ
Inductor dc resistance	R_{Lm}	2.4 mΩ

many samples of the output voltage would be taken and averaged every switching period. As a compromise, two samples are averaged and then processed through the voltage controller, $C_v(s)$. The output of the controller, $\hat{d}$, is sent to the master's UART module for transmission to all of the modules. The modules receive the duty cycle command at T_R. However, each module updates its duty cycle only on the rising edge of their Q_H signal, therefore the duty cycle of each module is updated between 0 and 1 switching cycles after T_R. The exact time will be determined by each module's phase shift. In Fig. 2.17, the highlighted module updates its duty cycle at T_k, with a duty cycle of $\hat{d}_{i+1}$. Therefore on average, the digital control loop adds a constant time delay of $T_{delay} = 2.0 \times T_s$ for all frequencies. This manifests itself as an additional phase shift of $2\pi \cdot T_{delay} \cdot f$ radians. The control loop delay is represented by the e^{-s2T_s} block in Fig. 2.16. Fig. 2.18(b) shows the loop gain of the intelligent battery with the digital control time delay taken into account.

A simple proportional-integral (PI) controller was designed as the compensator for the voltage control loop. The equation for the controller is shown in (2.23). The controller constants were chosen using the graphical method, with the aid of the bode



(a) ideal continuous time bode plot of $T_v(s)$

(b) bode plot of $T_v(s)$ with a digital delay of $2.0 \times T_s$ added.

Fig. 2.18: Uncompensated loop gain bode plots of the intelligent battery.

plots. Table 2.3 lists the controller constants for the intelligent battery's voltage controller. Fig. 2.19 shows the compensated bode plot for various operating conditions of the intelligent battery.

$$C_v(s) = K_{p,v} + \frac{K_{i,v}}{s} \tag{2.23}$$

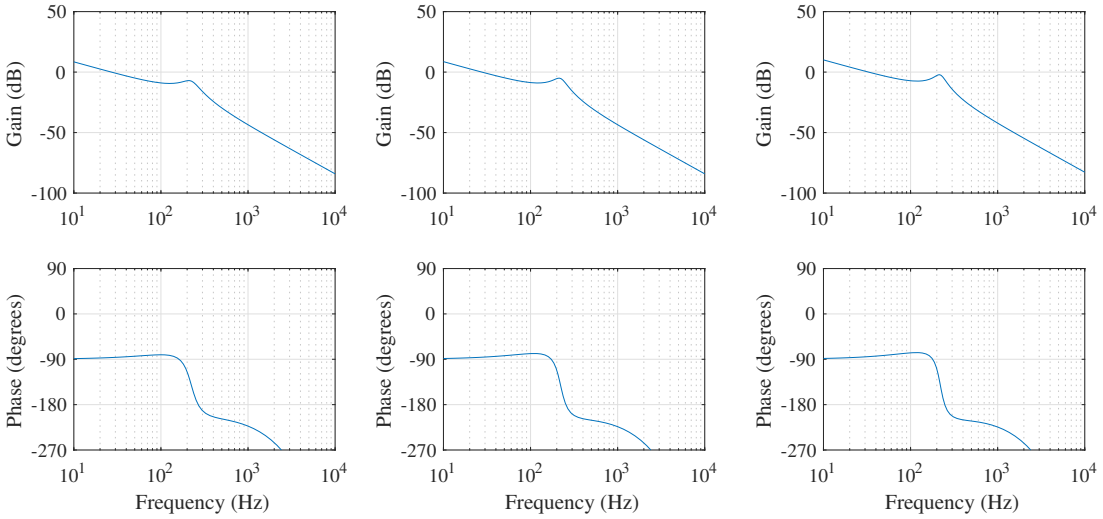
As shown in Fig. 2.19, the double pole caused by the output filter reduces the stability of the system as the load decreases. The transient response of the voltage controller could be improved by increasing the natural frequency of the system caused by the output filter, by reducing the size of the filter. In particular, the filtering inductors (L_m) could be reduced in size, by relaxing the design criteria of Section 2.3.6.

2.5.2 Current regulation

The current controller is used by the intelligent battery to regulate the current into and out of the pack, and is predominantly used when it is being charged and connected

Table 2.3: Voltage controller constants for the intelligent battery pack.

Parameter	**Value**
$K_{p,v}$	1.0e-3
$K_{i,v}$	0.2



(a) Phase margin: 93.4°, gain margin: 12.9 dB.

(b) R =3.84Ω. Phase margin: 94.1°, gain margin: 11.5 dB.

(c) $R = 9.6\ \Omega$, $V_{nom} = 4.2\ V$. Phase margin: 95.2°, gain margin: 6.4 dB.

Fig. 2.19: Bode plots of the compensated voltage loop gain under various operating conditions.

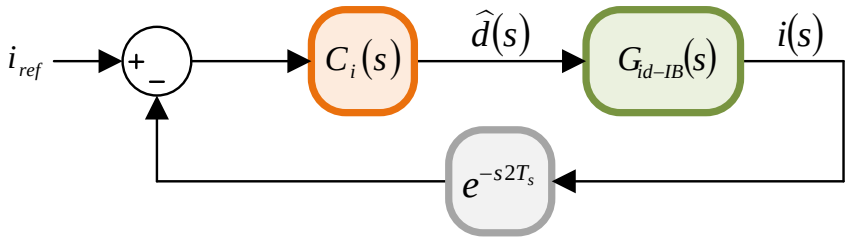
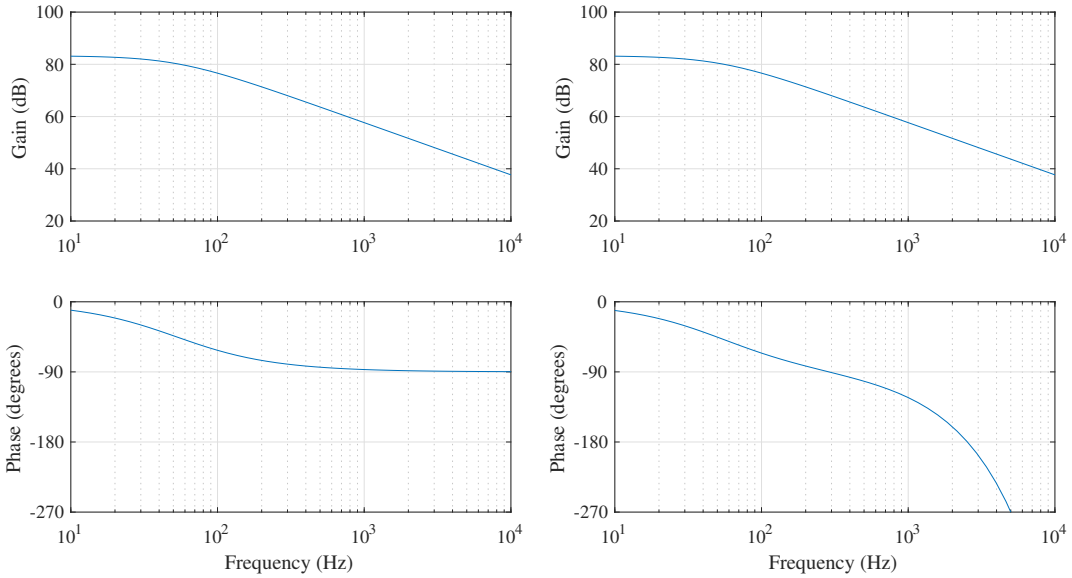


Fig. 2.20: Current control loop of the intelligent battery.



(a) ideal continuous time bode plot of $T_i(s)$

(b) bode plot of $T_i(s)$ with a digital delay of $2.0 \times T_s$ added.

Fig. 2.21: Uncompensated current loop gain bode plots of the intelligent battery.

to a voltage source. Using the same simplified topology as Section 2.5.1, we can derive a control to output transfer function, $G_{id}(s)$, for the current controller:

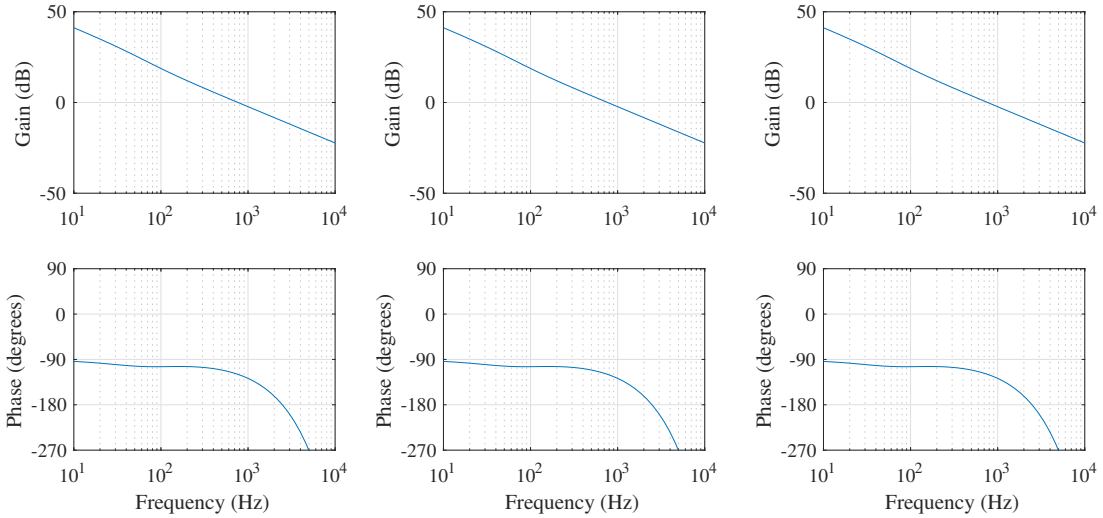
$$G_{id\text{-}IB}(s) = \frac{i(s)}{\hat{d}(s)} \tag{2.24}$$

$$G_{id\text{-}IB}(s) = \frac{DMV_{nom}}{sML_m + R_{ds\text{-}on} + R_{Lm}}. \tag{2.25}$$

A PI controller was designed as the compensator for the current control loop and it is shown in Fig. 2.20 as $C_i(s)$. The equation for the controller is shown in (2.26). As was

Table 2.4: Current controller constants for the intelligent battery pack.

Parameter	Value
$K_{p,i}$	1.0e-3
$K_{i,i}$	0.5



(a) Phase margin: 60.4°, gain margin: 10.3 dB.

(b) R =3.84Ω. Phase margin: 60.4°, gain margin: 10.3 dB.

(c) $R = 9.6\ \Omega$, $V_{nom} = 4.2\ V$. Phase margin: 60.4°, gain margin: 10.3 dB.

Fig. 2.22: Bode plots of the compensated current loop gain under various operating conditions.

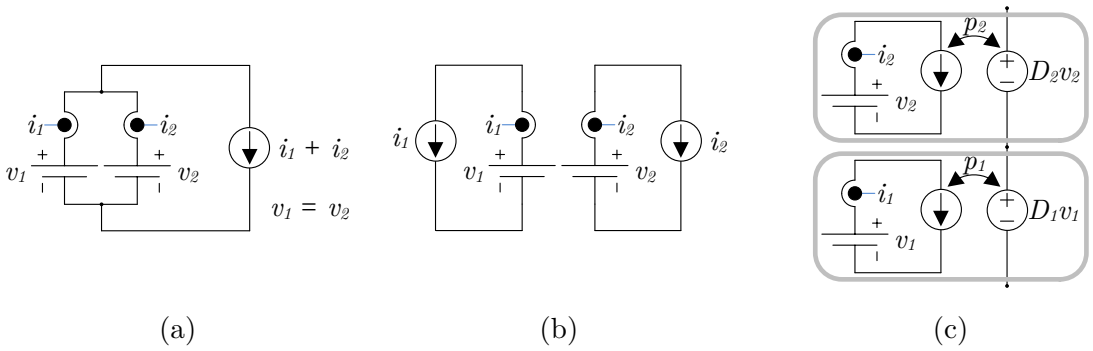
the case for the voltage controller, the uncompensated loop gain of the current control loop, $T_i(s)$, is equal to $G_{id\text{-}IB}(s)$, when the compensator has unity gain. $G_{id\text{-}IB}(s)$ is the control to output transfer function of Fig. 2.15 when the control signal is $\hat{d}(s)$ and the output is $i(s)$. The controller constants were chosen using the graphical method, with the aid of the bode plots. Table 2.4 lists the controller constants for the intelligent battery's current controller. Fig. 2.22 shows the compensated bode plot for various operating conditions of the intelligent battery.

$$C_i(s) = K_{p,i} + \frac{K_{i,i}}{s} \tag{2.26}$$

2.5.3 State of charge control

Each module in the intelligent battery pack operates its own SOC controller. The SOC controllers adjust the duty cycles of modules using a PI controller to synchronize their terminal voltages with the average terminal voltage of the pack. The terminal voltage of each module is the voltage that the module measures across its local group of cells.Each module receives the average terminal voltage from the master via the CAN Bus. Operation in this manner is equivalent to operating all of the cells from all of the modules in the intelligent battery pack in parallel, and cells that are connected in parallel are considered balanced. As an example of this, consider the two cell simplified example of Fig. 2.23. When two cells form a parallel pack of parallel cells, their terminal voltages are equal and their output currents are i_1 and i_2, where i_1 is not necessarily the same as i_2, as shown in Fig. 2.23(a). In this configuration, they are considered balanced. One can split up this parallel connection and load each cell individually with i_1 and i_2 such that their terminal voltages are *still* equal, as shown in Fig. 2.23(b). Thus, the two cells are operating as if they were connected in parallel. Finally, one can place the two cells in series as shown in Fig. 2.23(c), operating them with currents i_1 and i_2, such that their terminal voltages are equal and using a power converter to enable the series connection. The SOCs of parallel connected cells are considered to be nearly identical and require no further management [29]. Thus, the SOC of series connected modules will also be well synchronized, without having to directly compute their SOC. The modules of the intelligent battery pack measure the terminal voltage of the group of cells it is connect to. The modules use their half bridge switching network to load their cells so that their terminal voltage is equal to the average terminal voltage of the pack, in a similar manner to Fig. 2.23(c).

The one difference between the series connection of cells as shown in Fig. 2.23(c) and the parallel connection of cells as shown in Fig. 2.23(a), is that during rest (when



(a) (b) (c)

Fig. 2.23: Schematic showing the equivalence between the SOC controller of the smart cells and operation of the same cells in a parallel configuration.

there is no current flowing through the cells), the cell voltages will slowly return to their true open circuit voltage. During this time, there may be current flowing between the parallel cells as each cell's internal chemical states reach their equilibrium. Although this would mean that the parallel cells would be perfectly balanced, this is not always necessarily advantageous, as there would be spurious current flowing during an "off" state, leading to ohmic losses and heat generation in the cells, and ultimately, energy loss.

This SOC control method will only work if the modules are populated with cells of the same chemistry. In future work that will involve the combination of cells of various chemistries, the SOC will need to be computed.

2.5.4 Charging algorithm

The recommended charging algorithm for lithium ion batteries from a discharged state is by first charging them with a constant current (CC) and then when their terminal voltage reaches their top voltage, charging them with a constant voltage (CV). This is commonly referred to as a CCCV charging profile. Since the intelligent battery does not have the ability to regulate the module terminal voltages on the sub-millisecond time scale, a true CV charging step is not possible. However, a pseudo-CV charging

step is possible and a flow chart of the constant current, pseudo constant voltage (CCpCV) algorithm that is implemented in the master is show in Fig. 2.24.

During the pseudo-CV phase of charging, the intelligent battery remains in current control mode. As soon as the voltage of one of the modules reaches a threshold value, the charging current is reduced by $I_{\Delta\text{pCV}} = 0.5$ A. This is shown by the block called "Decrease charging current by $I_{\Delta\text{pCV}}$ A" in Fig. 2.24. The voltage threshold is computed by:

$$\min_k\{\Delta V_{\text{top},k}\} < \Delta V_{\text{top,limit-cc}} \tag{2.27}$$

where:

$$\Delta V_{\text{top},k} = V_{\text{top-max},k} - V_{\text{Bat},k} \tag{2.28}$$

$$\Delta V_{\text{top,limit-cc}} = 0.050 \text{ V}. \tag{2.29}$$

$V_{\text{top-max},k}$ is the maximum top voltage of the module k, and $V_{\text{Bat},k}$ is the terminal voltage of the cells connected to module k.

Once the charging current reaches a minimum current, $I_{pCV,\min}$, then the charging rate is limited by time and a minimum module threshold value defined by (2.30):

$$\min_k\{\Delta V_{\text{top},k}\} < \Delta V_{\text{top,limit-cv}} \tag{2.30}$$

where:

$$\Delta V_{\text{top,limit-cv}} = 0.0 \text{ V}. \tag{2.31}$$

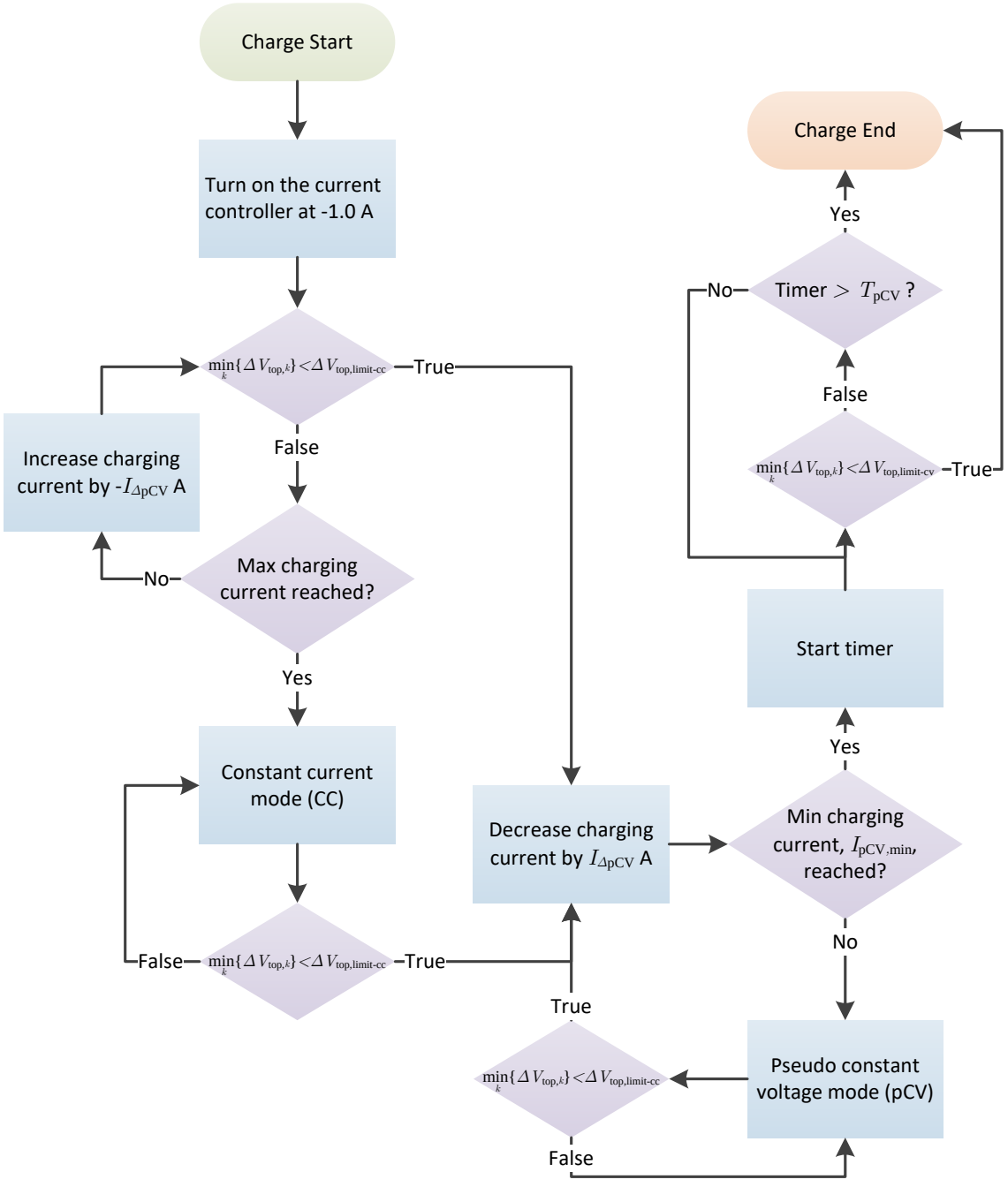


Fig. 2.24: Flow chart of the constant current, pseudo constant voltage charging (CCpCV) algorithm implemented by the master board of the intelligent battery.

All of the parameters that are used to define the CCpCV charging profile are easily modified in the intelligent battery and can be customized for the type and number of cells installed in each module.

2.6 Summary and discussion

Mechanically, the ability to easily replace individual cells throughout the pack is made possible through the innovative module design. However, this design will introduce increased conduction losses as compared to a conventional pack design, whose cells are normally welded together. A break down of these conduction losses are presented in Section 3.2.3. Conduction losses could be reduced by increasing the quality of the spring contacts, but at a cost.

The hot-swappable modular design of the intelligent battery pack is also an innovative approach to battery pack construction. The intelligent battery pack designed in this chapter is based on modules that contain cells in parallel. However, the modules could easily be small battery packs themselves to increase the scalability of the system, especially if such a design was implemented for a much larger battery pack (greater than 300 V, 10 kWh). This modular design introduces the idea of battery pack maintenance, where packs could be repaired instead of replaced when a series connected energy storage device fails. The ability to repair battery packs would be very advantageous for companies who must maintain battery packs in remote areas. Technicians could carry many small modules with them that would facilitate the repair of many battery packs, instead of carrying a single battery pack to replace in the event of a failure.

The dual communication channels to the modules solves the need for a real time synchronization signal and a data bus between the modules and the master. The CAN bus can provide the bandwidth necessary (up to 1 Mbps) to monitor all of the states of the modules with ease. Its inherent master-less architecture will be ideal

for future work that dissolves the need for master control. The sync and control signal is an elegant solution to provide two pieces of information with a single wire: 1) a synchronization pulse, and 2) a regular digital value for precise control actions. By choosing a digital delivery mechanism for the control action, the system is more immune to noise. Granted, the dual communication channels increase the system complexity and cost, but for a research grade battery pack, this was an acceptable trade-off. Furthermore, with both communication channels now in place, different intra-pack communication architectures may be investigated.

The intelligent pack has been built with research in mind and thus almost every variable in all of the modules and the master can be modified using a the serial, CAN, or WiFi interface.

Chapter 3

Intelligent battery simulation and experimental results

Chapter 2 introduced the intelligent battery design. In this chapter, results are presented from the simulations and laboratory testing of the device. The results indicate the improvements made possible by additional power electronics in multi-cell battery packs.

3.1 Simulations

The intelligent battery pack was simulated in MATLAB's Simulink environment using two different models: a switched model and an averaged model.

The switched model was used to design the voltage controller, $C_v(s)$, of Fig. 2.11. This model takes into account the delays in the communication network and models the switching actions of all 24 modules.

The averaged model was used to design the SOC controller, $C_{SOC}(s)$, of Fig. 2.11. The averaged model does not simulate any of the high frequency actions and therefore, can run hundreds of times faster than the switched model. Using battery models

available in the Simulink environment, the charge and discharge characteristics of the intelligent battery pack can be simulated.

In both models, the 24 cell capacities were randomly generated using MATLAB's pseudo random number generator. The equation for each module's capacity is shown below:

$$C_k = 10.0 + X_u \times 10.0, \tag{3.1}$$

where:

$$X_u \sim (0, 1)\,. \tag{3.2}$$

Equation (3.2) defines X_u as a uniformly distributed random number between 0 and 1. Therefore, the capacities of the simulated modules varied between 10 Ah and 20 Ah.

Simulation Parameters

Unless otherwise stated, the parameters listed in Table 3.1 were used throughout the simulation study.

3.1.1 Switched model

The switched model was used to verify the operation of the intelligent battery pack at the millisecond time scale. It was used to design and tune the output voltage controller, $C_v\,(s)$.

Table 3.1: Parameters used throughout the simulation study of the intelligent battery pack.

Description	**Parameter**	**Value**
Module capacities	C_k	$10.0 + X_u \times 10.0$ Ah
Module inductance	L_{sc}	10 µH
DC resistance of module inductor	R_{Lsc}	2.4 mΩ
Output capacitance	C_{out}	2200 µF
Switching frequency	f_s	20 kHz
Switching period	T_s	50 µs
On resistance of module MOSFETs	R_{DS-on}	0.72 mΩ
Number of modules	M	24 modules
Nominal module voltage	V_{nom}	3.6 V
Output voltage reference	V_{ref}	48 V

DC Duty cycle

At the millisecond time scale, some of the dynamic variables of the system can be assumed to be constant over a few seconds to simplify the model. The switched model assumes each module's dc duty cycle and phase shift can be treated as constant for these simulations and were calculated at the start of the simulation.

The dc duty cycle for each cell was calculated using the nominal voltage of the cells, the desired reference voltage, and the requirement that each cell is discharging in proportion to its capacity. Therefore, for a string of modules with a current of I_{string} flowing through them, we can start to write some equations about the system. The current through each module will be proportional to its capacity, therefore:

$$I_k \propto C_k \tag{3.3}$$

$$I_k = G \cdot C_k, \tag{3.4}$$

where G is a constant of proportionality. The output voltage of the string of modules is:

$$V_{out} = V_{ref} = V_{nom} \sum_{i=1}^{M} D_i \tag{3.5}$$

Finally, the duty cycle of each module can be related to each module's current:

$$I_k = D_k I_{string} \tag{3.6}$$

Using equations (3.4) and (3.6), a expression for D_k/C_k is obtained:

$$\frac{D_k}{C_k} = \frac{G}{I_{string}} \tag{3.7}$$

Solving (3.7) for D_k, and substituting the result into (3.5) yields:

$$\frac{G}{I_{string}} \sum_{i=1}^{M} C_i = \frac{V_{ref}}{V_{nom}} \tag{3.8}$$

Finally, we can use (3.7) and (3.8) to find an expression for D_k, the dc duty cycle for the k^{th} module:

$$D_k = \frac{V_{ref} \cdot C_k}{V_{nom} \cdot \sum_{i=1}^{M} C_i}. \tag{3.9}$$

Equation (3.9) was used to calculate the starting duty cycles of each module for the switched model simulations.

Phase shift

The output voltage ripple can be greatly reduced by phase shifting the modules with respect to each other. The modules in the intelligent battery pack were spaced evenly in time throughout the switching cycle. This is represented by (3.10):

$$\phi_k = 2\pi \frac{k}{M} \tag{3.10}$$

Table 3.2: $C_v(s)$ Control parameters.

Parameter	**Value**
$K_{p,v}$	1.0e-3
$K_{i,v}$	0.2

where ϕ_k is the phase shift of the k^{th} module in radians.

Time delay modelling

In the experimental version of the intelligent battery pack there are non negligible time delays in the voltage control loop that must be modelled in order to accurately model its behaviour, as described in Section 2.5.1.

In the switched model of the intelligent battery pack, the sampling and communication delay was implemented with delay blocks, for a total delay of $1.5 \times T_s$. The variable delay caused by the different phase shifts of each module that will introduce another delay of $0.0 \times Ts$ to $1.0 \times T_s$ was accurately modelled with sample and hold blocks triggered by each module's gating signal of Q_H.

Results

The voltage controller was implemented with a simple proportional integral controller (PI). The continuous time version of the controller implemented in MATLAB is shown in (3.11).

$$C_v(s) = K_{p,v} + \frac{K_{i,v}}{s} \tag{3.11}$$

The gain values used in the controller were designed in the previous chapter, but are repeated here in Table 3.2 for convenience.

Fig. 3.1 shows the simulation results of two circuits undergoing a series of load changes: 1) the 24 module intelligent battery pack and 2) an equivalent half bridge converter with the same controller as shown in Fig. 2.15. At 400 ms, the load is increased by 100% from 12.5 A to 25 A. At 800 ms, the load is decreased by 50% from 25 A to 12.5 A. At both load transitions the natural frequency of the module inductors and the output capacitor is excited. This is largely due to the very large inductor designed for the intelligent battery and the very low impedance of the inductors and switches that would dampen this oscillation. A more advanced control technique could be employed to reduce these deviations from the reference value of 48 V, however this is not the focus of this work.

As expected, both models are nearly identical in their simulation results, validating the simplifications of Fig. 2.15 where the intelligent battery pack was modelled as a single half bridge switching network in order to simplify controller design. The largest difference between the two simulations is the voltage and current ripple. The phase of each module of the intelligent battery pack was phase shifted according to (3.10), and this has the effect of reducing the output voltage ripple, as shown in the inset graphs of Fig. 3.1.

3.1.2 Averaged model

The averaged model was used to verify the operation of the intelligent battery pack at the minute time scale. It was also used to tune the SOC controller, $C_{SOC}(s)$. The continuous time version of the controller implemented in MATLAB is shown in (3.12) and the values of the controller are shown in Table 3.3.

$$C_{SOC}(s) = K_{p,SOC} + \frac{K_{i,SOC}}{s} \tag{3.12}$$

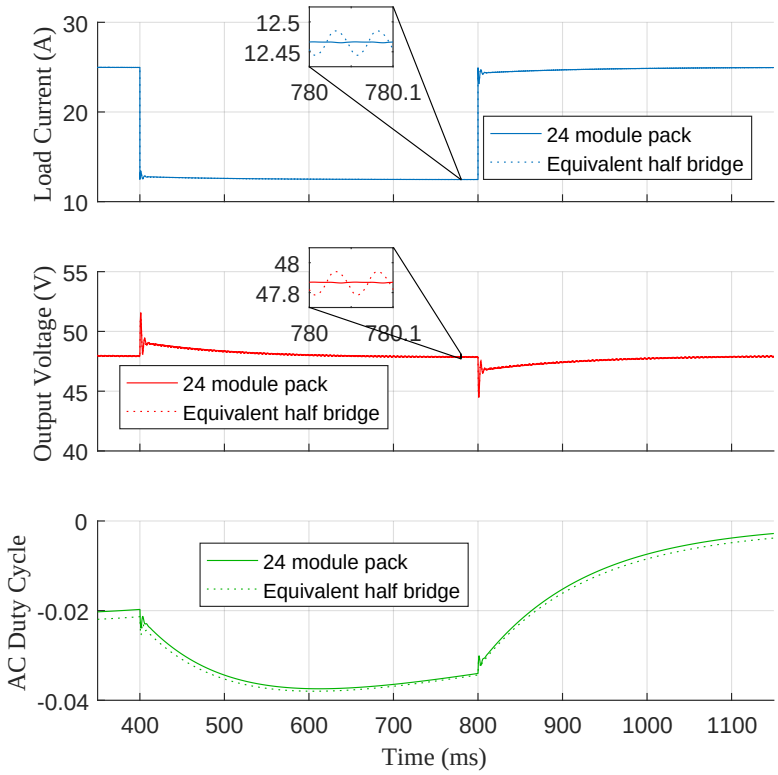


Fig. 3.1: Simulation results of a 24 module intelligent battery pack undergoing a 12.5 A increase in load at 40 ms and then a 12.5 A decrease in load at 80 ms. The bottom graph is the ac component of the duty cycle, $\hat{d}$.

Table 3.3: $C_{SOC}(s)$ Control parameters.

Parameter	**Value**
$K_{p,SOC}$	1.0
$K_{i,SOC}$	1.0e-3

In the following simulation of the averaged model, a simulated intelligent battery pack was subjected to a ± 25 A current whose polarity changes when any one of the modules reaches its terminal voltage limits. For the simulation, the lower limit was set to 3.1 V and the upper limit was set to 4.1 V. The intelligent battery pack was initialized with 24 random capacities as defined in Table 3.1; the initial SOC of each module was defined by (3.13):

$$SOC_k = 25 + X_u \times 50. \tag{3.13}$$

Capacity regulation

In this simulation, a 24 module intelligent battery pack was initialized with 24 random capacities as defined in Table 3.1. The state of charge of each module at the start of the simulation was randomly calculated using (3.13). Each module was unaware of its random capacity and thus they were all initialized to the same duty cycle, $D_i = 48/(3.6 \times 24) = 0.56$. The SOC controller used only the cell's local terminal voltage and subtracted the average terminal voltage of the pack for its error calculation.

Fig. 3.2 shows how the states of intelligent battery pack evolved over the course of the simulation, driving the SOCs of the modules to a state of synchronization. In the top plot, the total amount of energy delivered to the load was also calculated and as expected, this amount grows each cycle until all of the SOCs were synchronized.

Fig. 3.3 compares the normalized capacities and normalized ending duty cycles from the modules simulated in Fig. 3.2. As expected, the normalized duty cycles were all almost perfectly equal to the normalized capacities. Discrepancies exist due to the component loses which were not modelled in determining each module's D_k using (3.9). These results are very good considering the SOC controller used only the terminal voltages of the local cell and the average terminal voltage of the pack in its calculations.

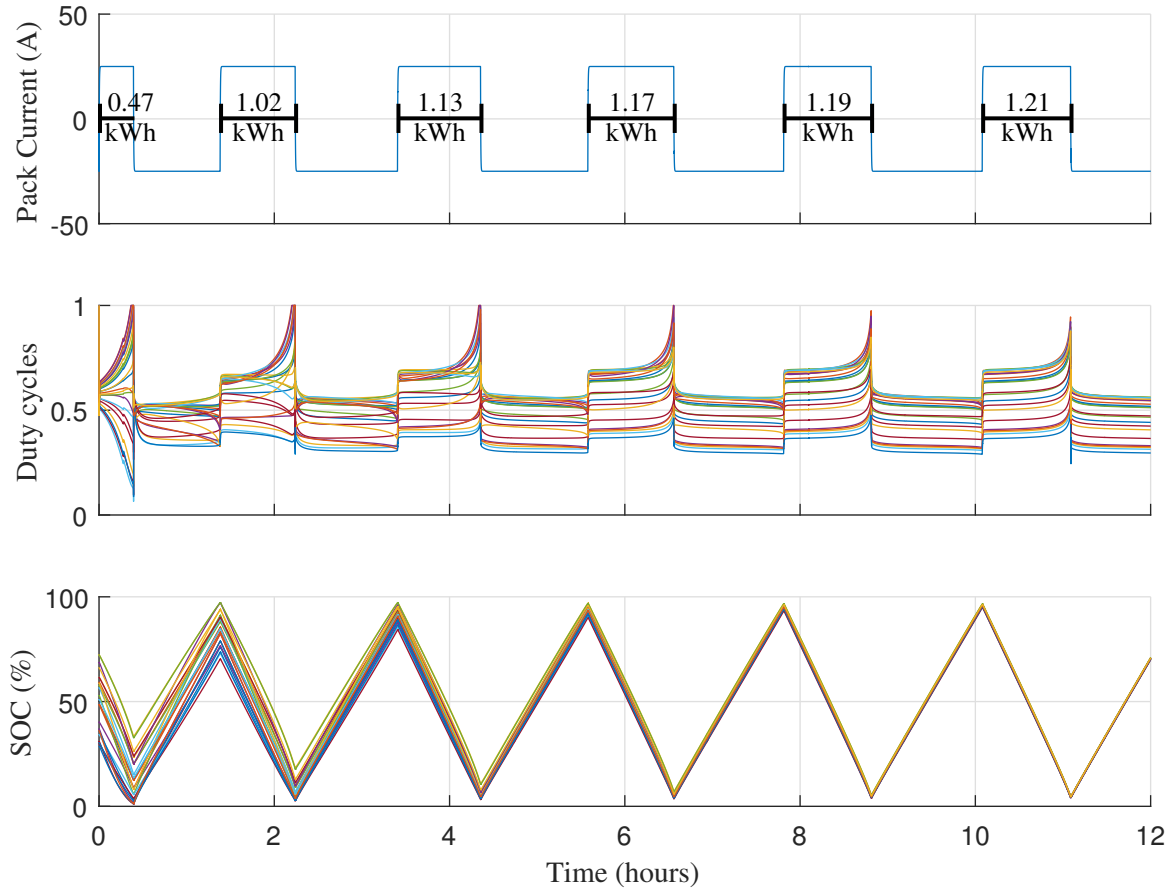


Fig. 3.2: Simulation results of a 24 module intelligent battery pack under a ±25 A load. Each module is initialized with an initial duty cycle of 0.56 and is connected to a battery cell of random capacity as described in Table 3.1.

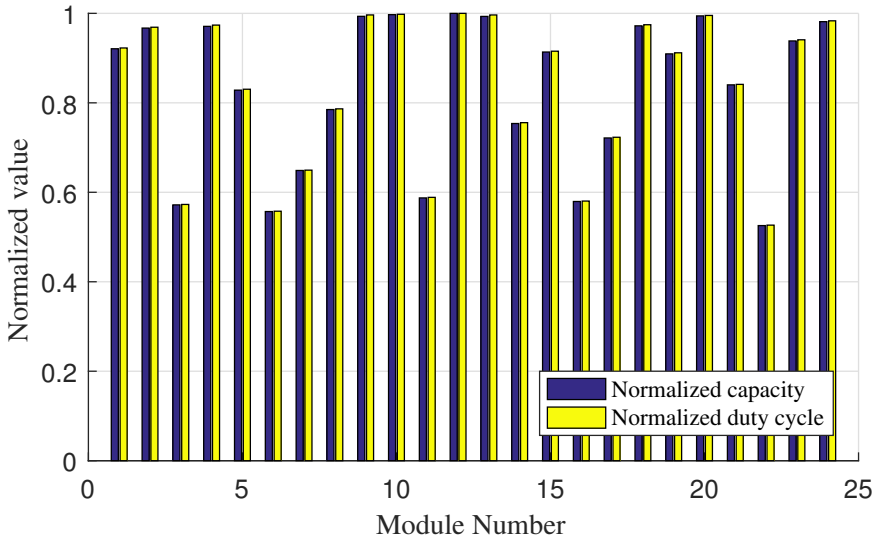


Fig. 3.3: Normalized capacities of the modules simulated in Fig. 3.2, along with the normalized duty cycles at the end of the simulation.

3.1.3 Limitations

Capacity spread

The steady state duty cycle of each cell was calculated using (3.9) and is repeated below for convenience. However, because the duty cycle of each module must remain within the limits of $D_k \in (0, 1]$, in a practical system, this places a limit on the spread in module capacities.

$$D_k = \frac{V_{ref} \cdot C_k}{V_{nom} \cdot \sum_{i=1}^{M} C_i} \tag{3.14}$$

For example consider a pack with the following capacities, output voltage, and nominal voltage:

$$C = \begin{bmatrix} 10 \\ 1 \\ 1 \end{bmatrix} \tag{3.15}$$

$$V_{ref} = 6 \text{ V} \tag{3.16}$$

$$V_{max} = 4.2 \text{ V} \tag{3.17}$$

$$V_{nom} = 3.6 \text{ V} \tag{3.18}$$

$$V_{min} = 2.8 \text{ V} \tag{3.19}$$

The calculated duty cycles are:

$$D = \begin{bmatrix} 1.39 \\ 0.14 \\ 0.14 \end{bmatrix} \tag{3.20}$$

Clearly, this set of duty cycles is invalid because D_1 is greater than 1. Using (3.14), a boundary condition for the capacities can be derived:

$$\max\{C_i\} \leq \frac{V_{nom} \sum_{i=1}^{M} C_i}{V_{ref}} \tag{3.21}$$

Equation (3.21) is only valid at V_{nom}, whereas this equation must hold at any operating point along the voltage curve of the battery cells being used. Despite this caveat, (3.21) is a good starting point when designing a system.

The only way to remain within the bounds of (3.21) for a given set of capacities, is to adjust V_{ref}. Lowering the output voltage of the intelligent battery pack relaxes the bounds. Using the capacities of (3.15) and the worst case cell voltage, V_{min}, the maximum V_{ref} that can be achieved with that combination of cells can be determined:

$$10 \leq \frac{2.8\,(10+1+1)}{V_{ref}} \tag{3.22}$$

$$V_{ref} \leq 3.36 \text{ V} \tag{3.23}$$

Using the value for V_{ref} calculated above, the new duty cycles in the worst case scenario are:

$$D = \begin{bmatrix} 1.00 \\ 0.10 \\ 0.10 \end{bmatrix} \tag{3.24}$$

Changing the voltage reference to 3.36 V as calculated with (3.23) results in a system which discharges all three cells in proportion to their capacities, but a system where the output voltage of the pack is significantly lower that simply connecting the three cells in series. In a real system, this type of extreme case should be avoided by replacing the under performing cells. Alternatively, if confronted with a system as specified by (3.15), a different control algorithm could be applied. The new control algorithm could discharge the cells at the same rate to yield the maximum possible output voltage. When cells 2 and 3 are discharged, they can be bypassed until cell 1 is completely discharged.

The only way to discharge all three cells of (3.15) in proportion to their capacities while maintaining a higher output voltage than calculated with (3.23) is to change the topology of the intelligent battery pack. Implementing each module with some type of buck-boost topology would solve the low output voltage issue.

Despite the low output voltage calculated with (3.23), the intelligent battery would be able to extract all of the energy out of this three cell pack. Using this pack in a

standard configuration, without any cell balancing during discharge, would mean that only 25% of the energy in the pack would be accessible during a single discharge.

3.1.4 Discussion

The averaged and switched models of the intelligent battery have demonstrated the theory of its basic operation. The switched model confirmed that the controller design of Section 2.5 will provide basic voltage regulation. The controller itself could be improved with more advanced controllers; notwithstanding, the approach presented is a simple, efficient solution.

The averaged model demonstrated that even with a simple PI controller operating on the terminal voltages of the battery cells, the SOCs of a random pack of cells can be well synchronized. The controller took a number of cycles to settle to the correct duty cycles as shown in Fig. 3.2. However, once the cells are synchronized, they will remain perfectly balanced. Therefore, this momentary loss of synchronization will only be temporary.

3.2 Experimental results

This section will highlight some of the experimental results conducted with the intelligent battery. Two intelligent batteries were constructed: a blue one and a yellow one, where the colour refers to the colour of the 3D printed parts. Fig. 3.4 shows a photo of both intelligent batteries in the lab.

The yellow intelligent battery was fully populated with new 18650 battery cells from Samsung, model number: INR18650-25R [108]. They have a nominal capacity of 2.5 Ah per cell, thus the yellow pack can store a total of 1728 Wh of energy. The blue intelligent battery was populated with 48 recycled 18650 cells, 2 cells per module,

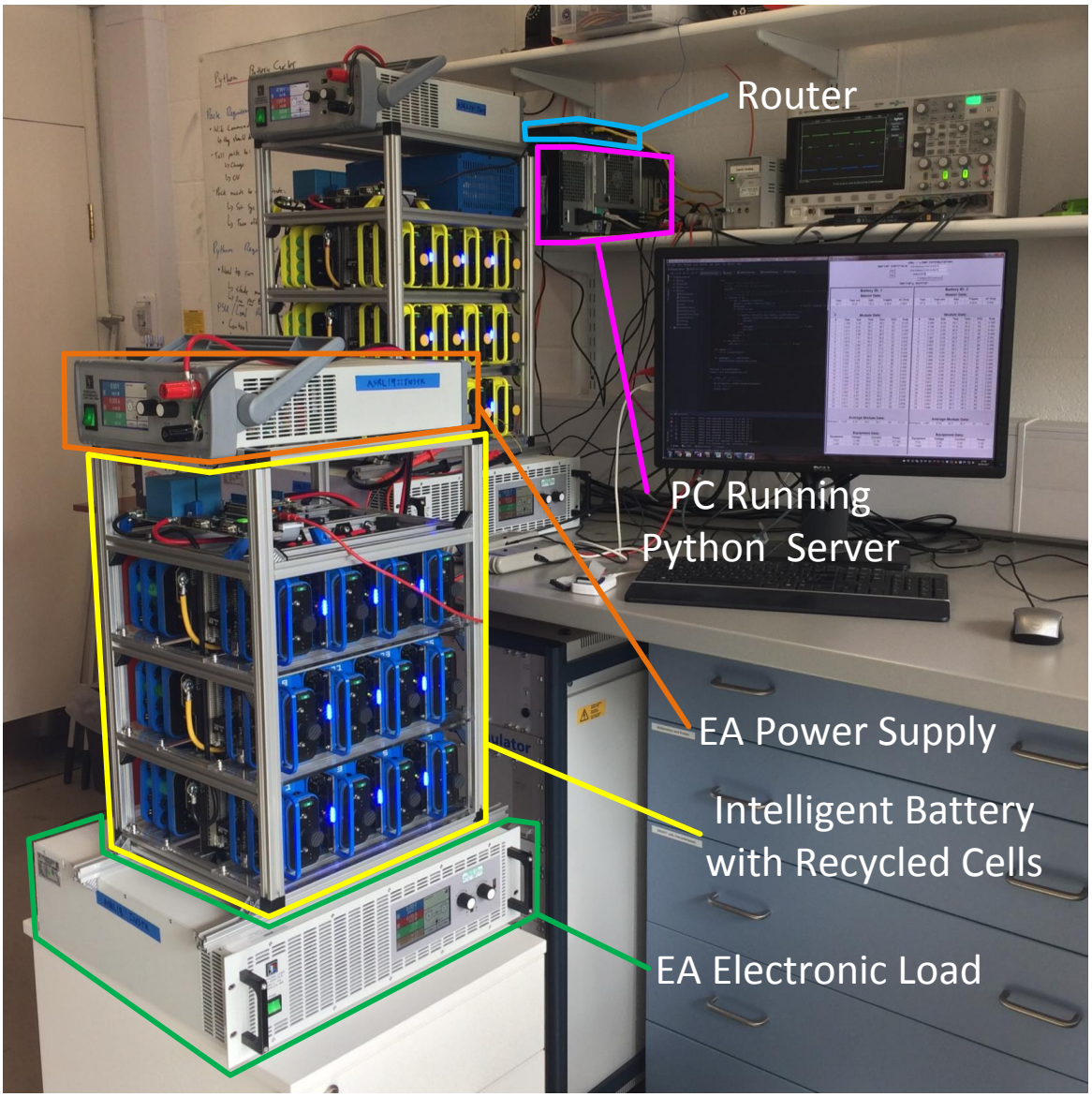


Fig. 3.4: Photograph of the experimental set-up with the main components highlighted. The non-highlighted intelligent battery in the background is populated with new cells.

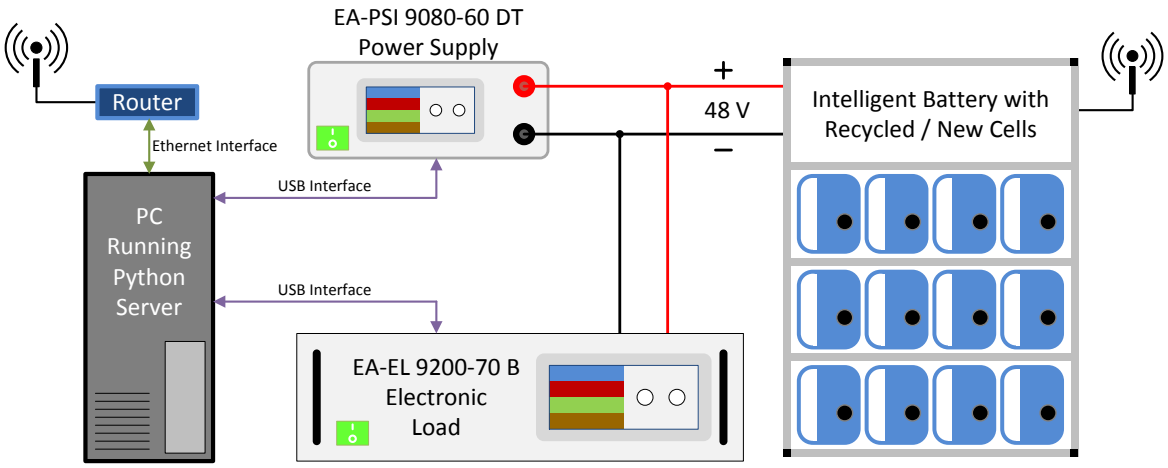


Fig. 3.5: Schematic of the experimental set-up to test the intelligent battery packs.

recovered from old devices. A full list of the recovered cells is shown in Table 3.4. The blue pack's total energy storage capability was 228 Wh.

3.2.1 Set-up

Both intelligent batteries were connected to a power supply and load for cycle testing. Fig. 3.5 shows a schematic drawing of the test set-up for each intelligent battery.

The power supplies used were both from Elektro-Automatik, model numbers EA-PSI 9080-60 DT (yellow) and EA-PSI 9200-25 DT (blue). The loads were also from Elektro-Automatik, model number EA-EL 9200-70B. The PSUs and loads were integrated with a server running on the PC so that they could be controlled and monitored.

The server was written in the Python programming language and was the main interface between the intelligent batteries and the user. Fig. 3.6 shows a screen shot of the graphical user interface (GUI) which was used to interface with the battery packs. The server lists all of the values of each module and the overall system values. At the bottom of the interface, values of the equipment are shown. All data displayed in the GUI was saved to binary files for further analysis.

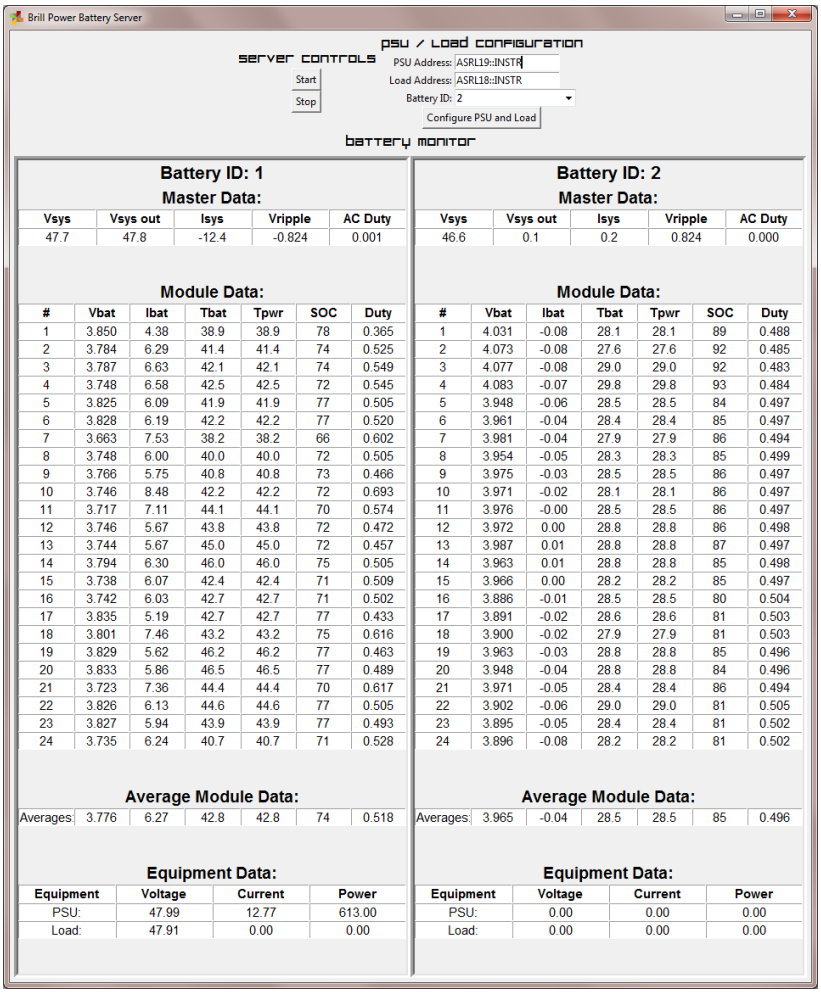


Fig. 3.6: Screen shot of the graphical user interface used by the Python server.

Fig. 3.4 shows an annotated photograph of the experimental set-up used to cycle both intelligent batteries. In the foreground is the blue intelligent battery populated with the cells listed in Table 3.4.

3.2.2 Transient experiments

A number of transient experiments were conducted to verify the operation of the intelligent battery under the most interesting operating conditions: load steps, and module insertion and removal. For all experiments in this subsection, three Agilent N2891A differential voltage probes captured pertinent traces around module number

Table 3.4: List of cells used to populate the blue intelligent battery.

Module Number	**Cell 1 (Ah)**	**Cell 2 (Ah)**	**Total (Ah)**
1	1.86	1.89	3.74
2	1.87	1.88	3.75
3	1.89	1.61	3.49
4	1.88	1.88	3.76
5	1.09	1.01	2.09
6	1.02	1.08	2.10
7	1.06	1.08	2.14
8	1.20	1.21	2.41
9	1.15	1.19	2.34
10	1.16	1.10	2.26
11	1.27	1.15	2.41
12	1.26	1.26	2.51
13	1.25	1.26	2.50
14	1.26	1.25	2.51
15	1.23	1.24	2.48
16	1.27	1.27	2.53
17	1.27	1.27	2.53
18	1.27	1.27	2.53
19	1.23	1.23	2.47
20	1.28	1.28	2.57
21	1.28	1.28	2.57
22	1.81	1.72	3.52
23	0.95	1.11	2.06
24	1.02	1.11	2.13
		Average:	2.64
		Standard Deviation:	0.55

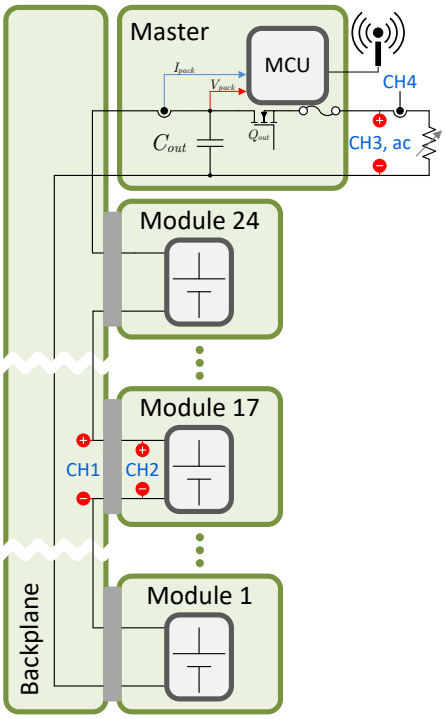
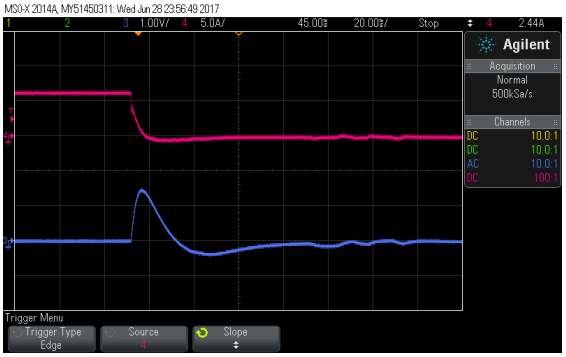


Fig. 3.7: Schematic showing the four probe placements (CH1, CH2, CH3, and CH4) used throughout the measurements of the transient experiments.

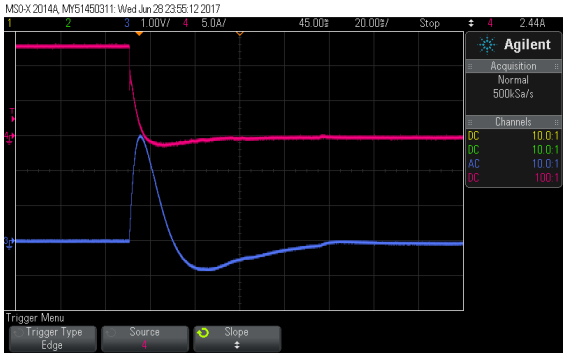
17 and a Fluke i310s ac/dc current clamp captured the output current of the intelligent battery pack. Positive current is out of the intelligent battery pack. The probes were placed according to Fig. 3.7. The output voltage of the intelligent battery pack was set to 48 V for all experiments. In some descriptions, individual components are referenced, please use Fig. 2.4 as a guide.

Load step

The behaviour of the intelligent battery's output voltage under various load steps are shown in Fig. 3.8 and Fig. 3.9. The load step was created by turning the output of the electronic load on and off while the intelligent battery regulated the output voltage to 48 V. In all scenarios, the output voltage remains within reasonable bounds, the worst case occurring during a 12.90 A load decrease shown in Fig. 3.8(b). In this case, a voltage overshoot of about 3 V occurs during the load step, representing a 6.25% overshoot.

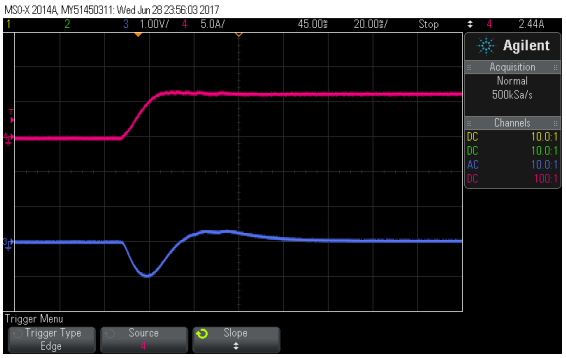


(a) 298 W, 6.23 A load decrease

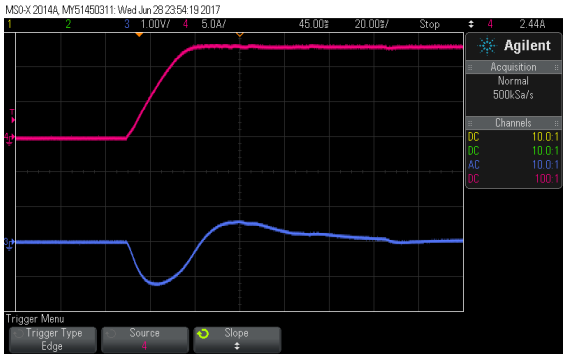


(b) 616 W, 12.90 A load decrease

Fig. 3.8: Output voltage and output current responses to various load decreases to zero. Channel 4, top, magenta, is the output current. Channel 3, bottom, blue, is an ac coupled trace of the output voltage. Time scale: 20 ms per division.



(a) 298 W, 6.23 A load increase



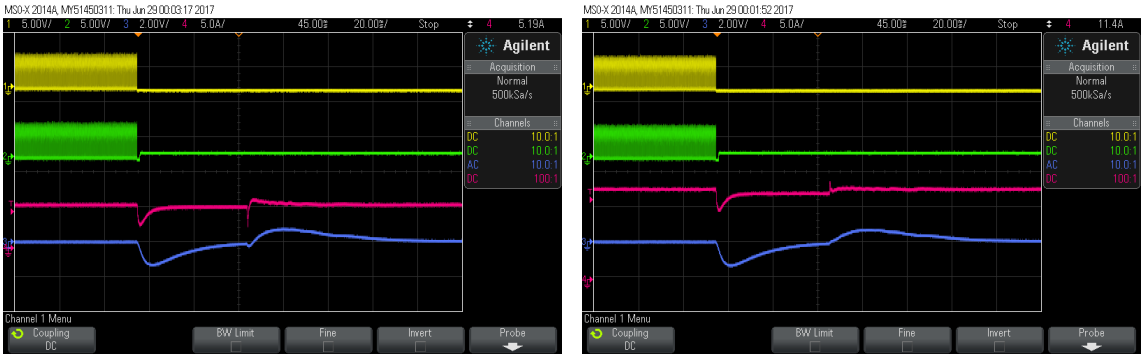
(b) 616 W, 12.90 A load increase

Fig. 3.9: Output voltage and output current responses to various load increases from zero. Channel 4, top, magenta, is the output current. Channel 3, bottom, blue, is an ac coupled trace of the output voltage. Time scale: 20 ms per division.

Module extraction during discharge

Fig. 3.10 shows the voltage traces around module 17 and the output during an extraction event of module 17. Channels 1 and 2 show the switching action of module 17, which is occurring at 20 kHz and therefore cannot be discerned at the zoom level of Fig. 3.10. However, as soon as the module is extracted, the output current drops, along with the output voltage. This is because the positive output voltage provided by module 17 was extracted from the pack and was replaced by a slightly negative voltage of the bypass diode, D_{17}, turning on and taking over the current flow. The initial 2.5 A drop in the output current is due to the large output capacitance of the electronic load charging the large output capacitance of the intelligent battery at the moment when module 17 is extracted. About 110 ms after the extraction event, there was a small overshoot in the output voltage. This occurs because the relay closes and the voltage drop across D_{17} was reduced to ≈ 0 V. Despite the different currents being provided by the pack, Fig. 3.10(a) and Fig. 3.10(b) show that the transient response at the output is almost identical in both cases.

What was also crucial in this experiment was that the voltage across the module does not exceed 13.2 V, the maximum varistor voltage of the transient voltage suppressor located on the output of the module. As expected, the output voltage of the module did not reach 13.2 V, or even the minimum varistor voltage of 8.8 V, due to the bank of capacitors, C_{5V}, used for the auxiliary 5 V dc to dc converter as described in Section 2.3.8. In addition to C_{5V}, the energy in the inductor is also absorbed by the diode which connects the output of the module to C_{5V} and the body diode of $Q_{L,17}$ which together form the discharge path of L_m right after the extraction event. This also explains why the output voltage across module 17 after the extraction event remained well within limits.



(a) 298 W, 6.22 A load (b) 616 W, 12.912 A load

Fig. 3.10: Waveforms measured around module 17 during extraction under various discharging conditions. Channel 1, yellow, is the voltage across the backplane slot of module 17. Channel 2, green, is the voltage across the output of module 17. Channel 3, blue, is an ac coupled trace of the output voltage. Channel 4, magenta, is the output current. Time scale: 20 ms per division.

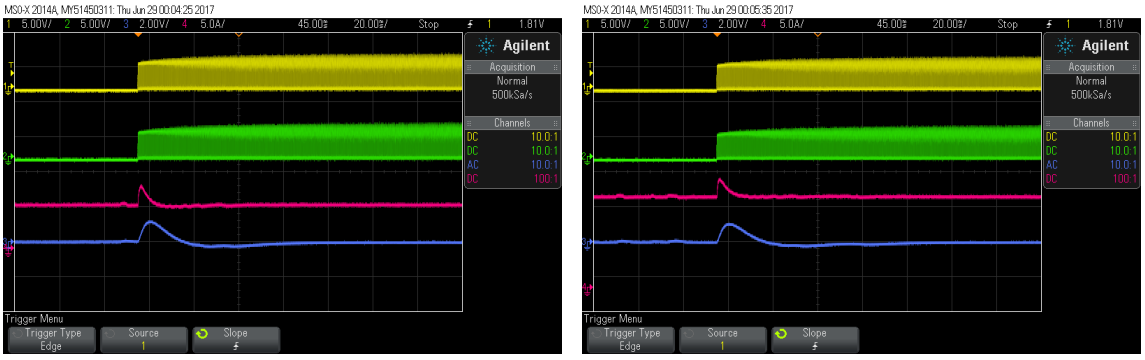
Module insertion during discharge

Fig. 3.11 shows the voltage traces around module 17 and the output during an insertion event of module 17. In both current loads, there is an almost identical output voltage overshoot of 0.5 V when module 17 started gating again.

Module extraction during charge

Fig. 3.12 shows the voltages around module 17 during extraction under various charging currents. These waveforms were important to analyse to ensure that none of the voltage ratings of any of the devices were exceeded during these extraction events. During charge, the current through the pack is abruptly interrupted, thus the inductors of the 23 other modules that are still in the pack will cause an increase in voltage around the module that is being extracted. It is important to keep this voltage to a minimum for two reasons: 1) to avoid component damage - the bypass diodes D_k are rated to 45 V, and 2) to avoid arcing as the module is physically removed from the backplane.

As shown in Fig. 3.12, the voltage across the module 17's slot on the backplane spiked to about 25 V in both scenarios. 25 V is right in between the minimum (22.8 V)



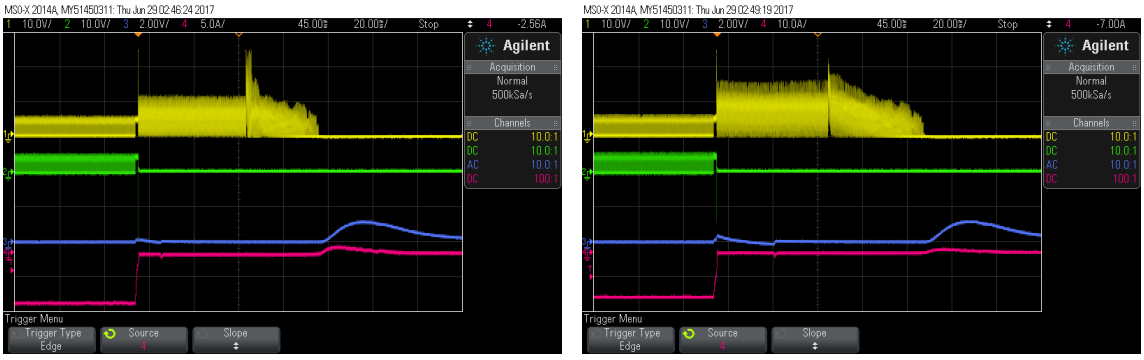
(a) 298 W, 6.23 A load (b) 616 W, 12.91 A load

Fig. 3.11: Waveforms measured around module 17 during insertion under various discharging conditions. Channel 1, yellow, is the voltage across the backplane slot of module 17. Channel 2, green, is the voltage across the output of module 17. Channel 3, blue, is an ac coupled trace of the output voltage. Channel 4, magenta, is the output current. Time scale: 20 ms per division.

and maximum (33.2 V) varistor voltage for the backplane transient voltage suppressor, and thus it performed its desired function. The voltage remained higher than normal as the rest of the modules continued gating, trying to "charge" module 17. The slight overshoot in output voltage seen about 180 ms after the extraction event was mainly due to the voltage controller taking over from the current controller to raise the output voltage of the pack. By raising the output voltage and closing the output MOSFET Q_{out}, a current surge into the modules is prevented when the relay, RLY_{17}, closes. The relay closing event and the resumption of charging was not captured in Fig. 3.12. The resumption of charging occurs about 4 s after an extraction event and the charge current is ramped back up to its former value.

Module insertion during charge

There are no interesting transient events during a module insertion when the intelligent battery is charging. Upon detection of a module insertion, the intelligent battery will stop the current charging process, turn on the inserted modules, and then resume the charging process.



(a) 335 W, 7.00 A charge (b) 613 W, 12.77 A charge

Fig. 3.12: Waveforms measured around module 17 during extraction under various charging conditions. Channel 1, yellow, is the voltage across the backplane slot of module 17. Channel 2, green, is the voltage across the output of module 17. Channel 3, blue, is an ac coupled trace of the output voltage. Channel 4, magenta, is the output current, which is abruptly interrupted when a module is extracted during charge. Time scale: 20 ms per division.

3.2.3 Efficiency

Efficiency measurements for the intelligent battery are non-trivial since each module has its own power source, the battery cells, thus one would need to monitor the input power on each module and compare it to the output power. As a compromise, the efficiency of the intelligent battery was calculated by first analysing a module at various operating currents and then measuring the conduction resistances through the battery pack to determine the overall system efficiency.

The efficiency calculations include the losses for all of the control and communication hardware, thus, are a true measure of system efficiency.

Module efficiency

The module's efficiency was determined with the help of a test rig, which consisted of a number of power resistors connected in parallel that can be connected and disconnected from the output of the module. Fig. 3.13 shows an annotated photograph of a module undergoing an efficiency test.

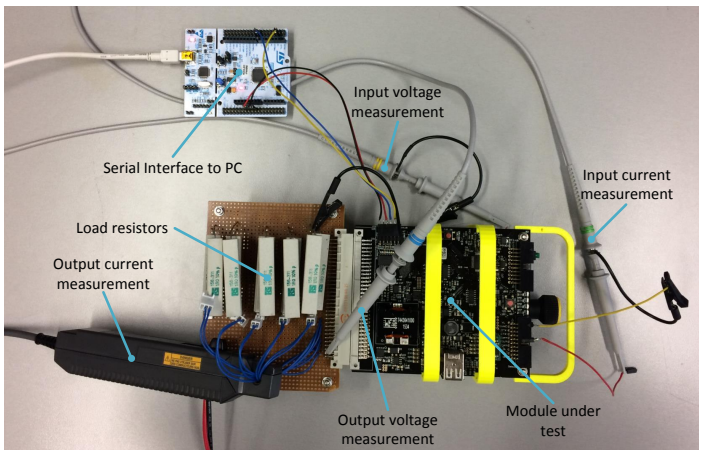


Fig. 3.13: Annotated photograph of a module undergoing an efficiency measurement.

The input voltage to the module was measured using an Agilent N2894A oscilloscope probe which was connected directly to one of the cells via a Kelvin voltage connection. The input current to the module was measured using an Agilent N2894A oscilloscope probe which was connected to the output of the module's hall effect battery current sensor: Allegro MicroSystems' ACS711EEXLT-31AB-T. The output voltage was measured using an Agilent N2894A oscilloscope probe across the output of the DIN connector on the test rig, thus the losses of the DIN connectors were taken into account. The output current was measured using an Agilent N2783B current probe.

An Agilent MSO-X 2014A oscilloscope was used to obtain all of the measurements during the efficiency tests. For each measurement, two values were taken: the average value and the ac rms value. The average input power was added to the ac rms input power to calculate the true input power. Likewise, the average output and ac rms output powers were summed together to yield the true output power.

Efficiency measurements were taken at 5 current points and the duty cycle of the module was adjusted so that it provided an average voltage of 2 V at the output. This is because if it were working in the intelligent battery pack, each module would

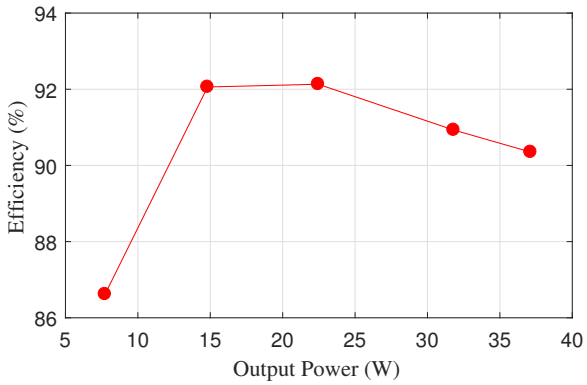


Fig. 3.14: Module efficiency for various output powers.

contribute 2 V to the output to generate the desired 48 V. The nominal voltage across the cells was about 3.6 V.

Fig. 3.14 plots the module efficiency for various output powers. The peak efficiency that occurred was 92.1% at an output power of 22.4 W. The efficiency drops sharply at the low power range because the power that was required to power the module's electronics becomes increasingly dominant. The power consumed by the module's electronics was measured to be 0.61 W when the gating of Q_H and Q_L was off.

Losses in the pack

Resistance values for different parts of the pack were measured by measuring the voltage across the different parts while applying a current of 0 A to 13 A in 1 A increments.

The resistance of a backplane was measured by first removing all of the modules from one backplane. The voltage across the backplane was measured, along with the voltage across one of the relays. The resistance of the relays were discounted from the measured resistance across the backplane to yield the resistance a backplane would introduce if it were fully populated with modules. Table 3.5 lists the results.

The resistance between the (+) output terminal of the battery and the top most backplane is significantly higher than the resistance between the (-) output terminal of

Table 3.5: Measured resistances inside the intelligent battery pack.

Description	Value
Resistance of each backplane and wiring	1.40 mΩ
Resistance between the (+) output terminal of the battery and the top most backplane	11.28 mΩ
Resistance between the (-) output terminal of the battery and the bottom most backplane	1.44 mΩ

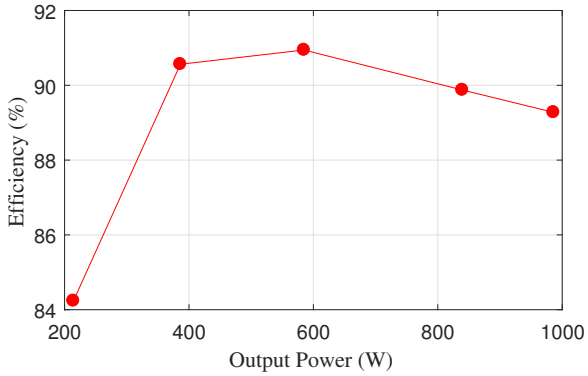


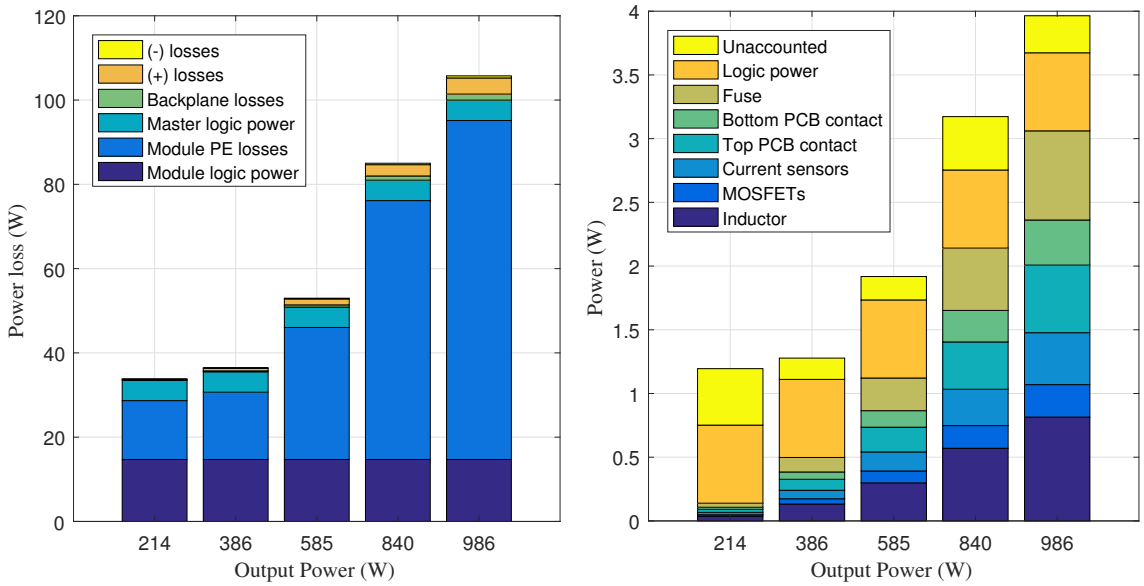
Fig. 3.15: Efficiency of the intelligent battery pack.

the battery and the bottom most backplane because of an additional output MOSFET, shown as Q_{out} in Fig. 2.4, which was used to disconnect the intelligent battery from a load (5.5 mΩ), output fuse (2.06 mΩ), current sensor (0.18 mΩ), and generally smaller tracks through these components on the Master PCB.

Overall system efficiency

The results of Fig. 3.14 and Table 3.5 can be combined to yield the overall efficiency of the intelligent battery pack, as shown in Fig. 3.15.

The overall efficiency of the system was good, especially considering the plot of Fig. 3.15 includes all of the losses in the system, including the losses associated with powering the logic circuits. The losses were dominated by the modules, as shown in the stacked bar chart of Fig. 3.16(a). The losses of the pack, which include the PCB traces



(a) Breakdown of power losses in the intelligent battery pack.

(b) Breakdown of the power losses in a module.

Fig. 3.16: Stacked bar charts of the power losses in the intelligent battery pack and a module.

of the backplanes and master board and all of the power interconnections between the backplanes and master board, were very small in comparison.

Fig. 3.16(b) breaks down the losses of a single module in more detail. There is a portion of power losses that was not accounted for, 7% to 13%, due to a few sources that have not been addressed:

- switching losses,
- conduction losses on the PCB, in particular between the bottom PCB and module PCB, and
- conduction losses from the top PCB to the aluminium threaded rod.

The last item on the list is particularly important as this connection point is one of the bottlenecks of conduction. Fig. 3.17 shows the top PCB disassembled from one of the modules, with the aluminium nut which secures it in place resting on the PCB. All of the current which flows through the battery cells must travel from the PCB through

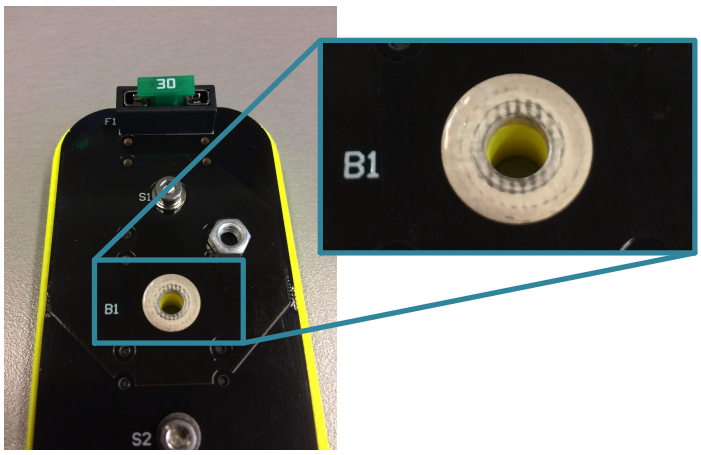


Fig. 3.17: Close up photograph of the top PCB disassembled, with aluminium securing nut placed on top.

the nut and then down the threaded aluminium rod. The contact surface between the nut and PCB is not ideal, shown by the more polished and reflective area of the pad B1, which is only a small circle around the hole. In addition, the nut will only engage a few threads with the rod when it is in place. In practice, the top PCB heated up considerably if the nut is not fixed tightly enough and some modules were more susceptible to heating than others.

The module MOSFETs are the least lossy components in the module, as shown in Fig. 3.16(b). This shows that the additional hardware of the modules has introduced losses that should be minimized during the next design iteration of the intelligent battery. As another comparison, the losses in all of the "power electronics equipment": MOSFETs, inductor, and current sensor, is almost the exactly the same as the losses in the "connection equipment": fuse, top PCB connection, and bottom PCB connection. The connection equipment was expected to add to the power loss, and designing it to be equivalent to the power electronics equipment is a good result. In a real system, the connection equipment losses could be almost entirely eliminated. The module level fuse is highly redundant in the intelligent battery and a real system would weld battery cells together, instead of using spring contacts.

In summary, the efficiency of the intelligent battery pack was very satisfactory given that this design was designed for research. The hot-swappable nature of the mechanical design and extra fusing at each module have contributed heavily to the power losses. Furthermore, all MCUs in the intelligent battery are high performance MCUs, and none of their power saving features were implemented.

3.2.4 SOC synchronization

For these experiments, the settings in Table 3.6 were used.

Table 3.6: List of settings for each intelligent battery for the SOC synchronization experiments. See Fig. 2.24 for a graphical representation of the values.

Setting	**Description**	**Yellow pack**	**Blue pack**
$I_{\text{charge,max}}$	Maximum charging current (A)	12.5	4.0
$I_{\Delta\text{pCV}}$	Charging current step during pCV charging (A)	0.5	0.25
$I_{\Delta\text{pCV,min}}$	Minimum charging current during pCV charging (A)	2.0	2.0
T_{pCV}	Charging timer expiry (minutes)	30	30
$\Delta V_{\text{top,limit-cc}}$	Reduce current threshold (V)	0.050	0.050
$\Delta V_{\text{top,limit-cv}}$	Stop charging threshold (V)	0.0	0.0

New cells, yellow pack

Fig. 3.18 shows the time evolution of the yellow pack with new cells installed. The two cycles shown are the first full cycle after the batteries were installed and the 10^{th} full cycle.. The intelligent battery did a good job at keeping the cell voltages in sync, however this could be improved. The duty cycles during the first cycle were a bit more noisy during charge than the subsequent charge cycle due to the controller and filter used at the time. It was tuned slightly to yield the more “smooth” duty cycle traces of the subsequent charge cycle.

It is important to remember that the modules had no prior knowledge of the cells that were installed and were simply operating to match their terminal voltage with the average terminal voltage of the pack. During the first cycle, the cells started with different terminal voltages, as is shown by the voltage error plot during the first hour. 1.3 kWh of energy was delivered to the load during this first cycle. Conversely during the subsequent cycle shown, the voltage error during this time period (hour 6 to 7), was much lower and 1.4 kWh was delivered to the load. In both cycles, the SOC controller struggled to maintain synchronisation near the bottom voltage. This is because the voltage would have been changing very rapidly at this point, especially with the constant power load that was applied. During the very short rest period shown, the the module voltages recover to different values shortly after the 6 hour mark. Although this indicates there is more energy left in some cells, they are all practically exhausted. In order to extract the maximum amount of energy from the pack, it is more important that the module voltages reach the "roll-off" point near the end of the cycle at the same time.

In a well matched pack with new cells, the intelligent battery pack topology would not increase the amount of energy that can be delivered to a load. However, as the cells age, the intelligent battery pack topology would enable the extraction of all of the energy from all of the degraded cells, as will be shown in the next subsection.

Recycled cells, blue pack

The enhanced performance of the intelligent battery pack is much more noticeable when used with recycled cells, as was done with the blue pack. Fig. 3.19 shows the time evolution of the system after two consecutive full cycles of the pack. During the first full cycle, the SOC controller was on and the pack delivered 142 Wh to a 334 W load. In the next cycle, the SOC controller was turned off and all of the modules

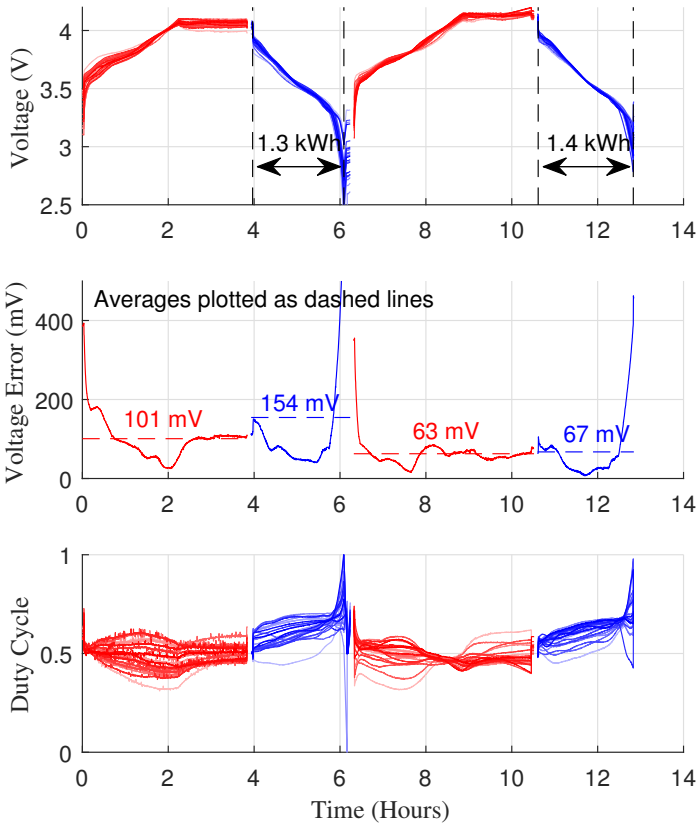


Fig. 3.18: Time evolution of the module cell voltages, module voltage error, and module duty cycles through two complete charge and discharge cycles of the intelligent battery with new cells.

output the same duty cycle. In this scenario, the pack was limited by its weakest cell and could only deliver 97 Wh to the 334 W load. In the following cycle, which is not shown, the SOC controller was turned back on and the battery delivered 144 Wh to a 192 W load.

This experiment clearly shows the effectiveness of adding power electronics to a battery pack to take advantage of all of the energy storage potential of all of the individual cells. Furthermore, although simplistic in nature, the SOC controller was able to take advantage of most of the energy storage potential without any prior knowledge of the cells. Therefore, packs of recycled cells of the same chemistry can be quickly assembled, without having to fully characterise all of the cells within.

Fig. 3.20 shows the normalized duty cycle distribution within the pack. The duty cycles were calculated by taking their average values over the first three half cycles of Fig. 3.19. The duty cycles should be proportional to the capacities, thus Fig. 3.20 suggests that further controller tuning is required. With more advanced controllers, each module could start to learn the behaviour of the cells it is connected to and adjust its output accordingly to optimize its performance. This will be discussed further in the future work section of Chapter 6.

3.2.5 Discussion

The performance of the intelligent battery pack designed in Chapter 2 was verified. The efficiency of the battery pack was quite good considering efficiency was not a targeted design criteria for this design iteration. Furthermore, the unique ability to hot-swap modules and easily replace cells added extra series resistance that does not normally exist in a typical battery pack or dc to dc converter.

When using variably degraded cells, the benefits of integrating power electronics into a battery pack are clear. In the experimental results presented here, the useful

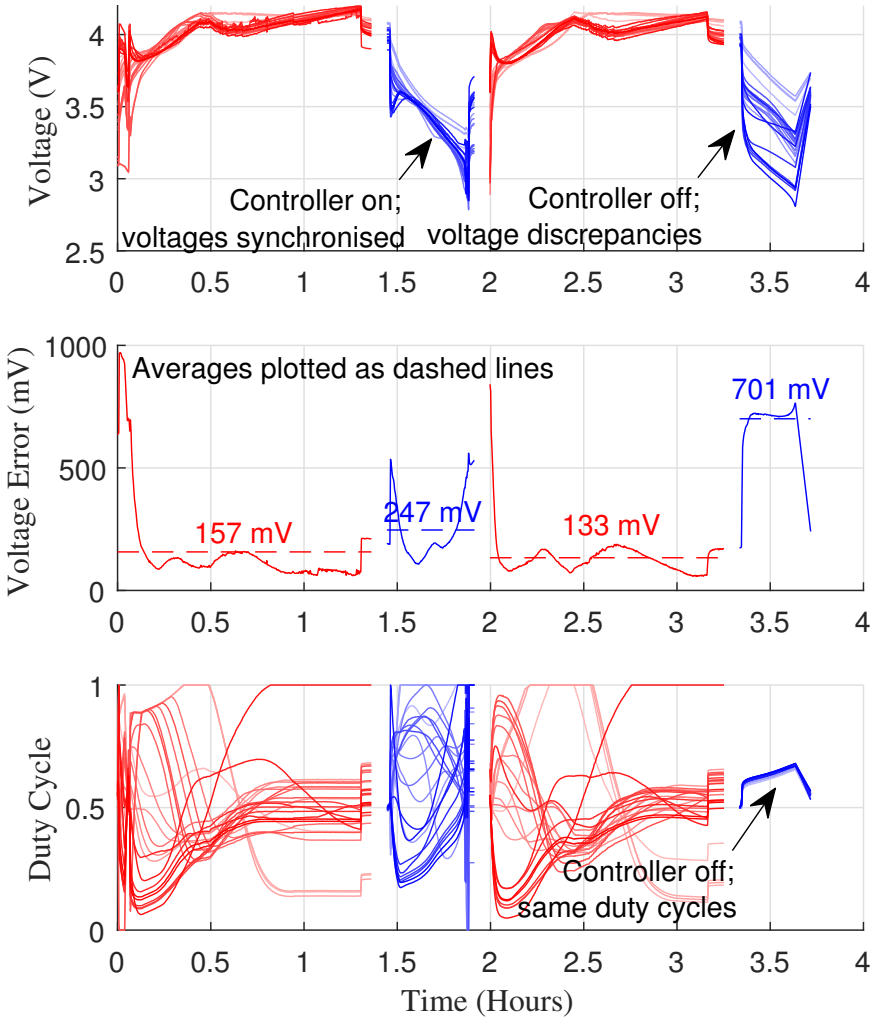


Fig. 3.19: Time evolution of the module cell voltages, module voltage error, and module duty cycles through two complete charge and discharge cycles of the blue intelligent battery with recycled cells.

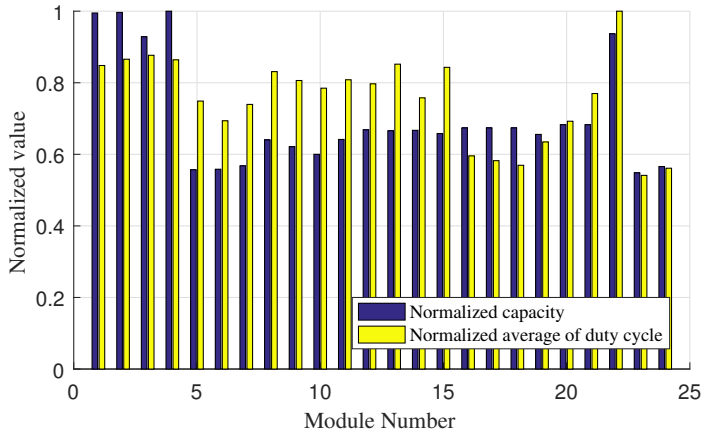


Fig. 3.20: Distribution of the normalized duty cycles and capacities of the blue intelligent battery using recycled cells. The normalized duty cycle was taken as the average duty cycle over the 3 half cycles of Fig. 3.19 where the SOC controller was on.

capacity of the blue pack increased by 46% from 97 Wh to 142 Wh using very simple terminal voltage control. However, in a real system that does not have a method to variably load cells, there would not be the extra losses created by the intelligent battery pack topology. Therefore, if the losses of the intelligent battery are taken into account, the pack of cells without control could have provided about 107 Wh of energy. Even still, this is not a just comparison because the intelligent battery is also providing some power conditioning.

The performance of the SOC controller never matched the performance of the simulation results presented earlier in this chapter. When adding a random resistance in series with each battery cell to the simulations to better emulate the varying resistance of the cell holder, the SOC controller performed just as well as reported in Section 3.1. Therefore, in order to fully understand the SOC controller performance discrepancy, a comparison of the battery model used in MATLAB should be compared with a battery model that represents the Samsung 25R cell. Furthermore, a unique battery model for each group of cells connected to each module should be characterised to determine how they interact with the SOC controller.

3.3 Summary

This chapter analysed the performance of the intelligent battery in theory and in practice. The hardware and software designs of Chapter 2 worked as designed, enabling low latency voltage and current control at the pack level, pack level monitoring via the CAN bus, and hot-swappable modules.

The simulation results showed that excellent SOC synchronization can be achieved by synchronizing the terminal voltages of all of the modules. Using only the terminal voltage could greatly simplify BMS design, as a complex battery model would not be required. Furthermore, it would allow the easy recombination of recycled cells into packs, whose individual battery models would be largely unknown. However, the experimental results showed that more work needs to be done to understand why the same level of synchronization could not be achieved in practice.

The control strategy of the intelligent battery presented was based on a current sinking load and a voltage controlled charging source. It is not limited to this single operating scenario. The intelligent battery is also capable of emulating a real battery pack, which can be connected to a bi-directional source-sink.

This chapter brings the discussion about the intelligent battery to a close. The following two chapters will explore how the integration of power electronics into battery packs can be simplified.

Chapter 4

Decentralised battery management

In this chapter, the possibility of a decentralised battery management system for series connected cells with the same architecture as Fig. 2.4 is explored. However, the system will not have any any inter-module communication, or any communication to a master controller. A schematic of the proposed decentralized battery management system is shown in Fig. 4.1.

In this schematic, the system is constructed out of three "smart cells", each containing a half bridge switching network identical to the switching network in the modules of the intelligent battery pack. Therefore, it has the same scalability metrics as the intelligent battery pack. Each smart cell has two distinct features that make it different from the modules of the intelligent battery pack:

1. There exists an independent, decentralized controller in each smart cell.

2. The filter inductor in each smart cell, L_{sc}, is used as a multi-purpose sensor.

The decentralized controller manages the state of charge (SOC) and monitors the state of health (SOH) of its locally connected battery cell. This information is used to apply a duty cycle to the switches Q_L and Q_H, such that the connected battery cell

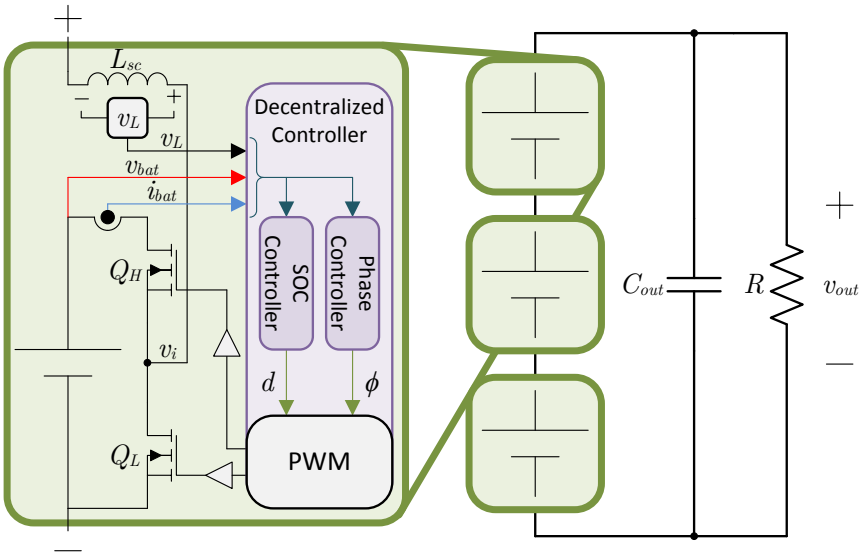


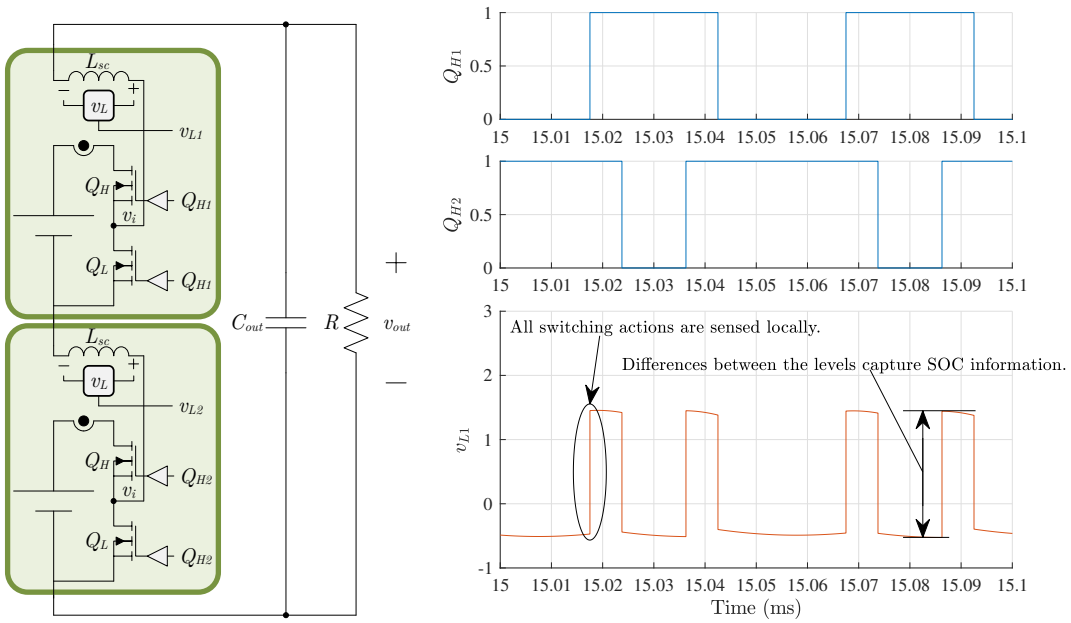
Fig. 4.1: A schematic diagram of the proposed decentralised battery management system. Each cell is called a "smart cell".

discharges in proportion to its capacity. Discharging all cells in proportion to their respective capacities yields two large benefits for the string of smart cells:

1. The SOC of all of the cells in the string will be synchronized.

2. Larger, healthier battery cells will be loaded more than the smaller, more degraded battery cells, thus the pack will degrade at a more uniform rate [109, 110].

As will become clear throughout this chapter, the voltage across the small filter inductor, v_L, contains all of the information required for each smart cell to determine its optimal switching pattern and to adjust its duty cycle to synchronize its SOC with the other smart cells in the string. To help motivate this fact, Fig. 4.2(b) is a simulation of a two smart cell system switching in its optimal switching pattern, with the voltage across one of the sense inductors shown. As shown by the annotations in the figure, all of the switching transitions were captured by the sense inductor, L_{sc}. Furthermore, the differences between the voltage "levels" of the voltage across the inductor captured SOC information.



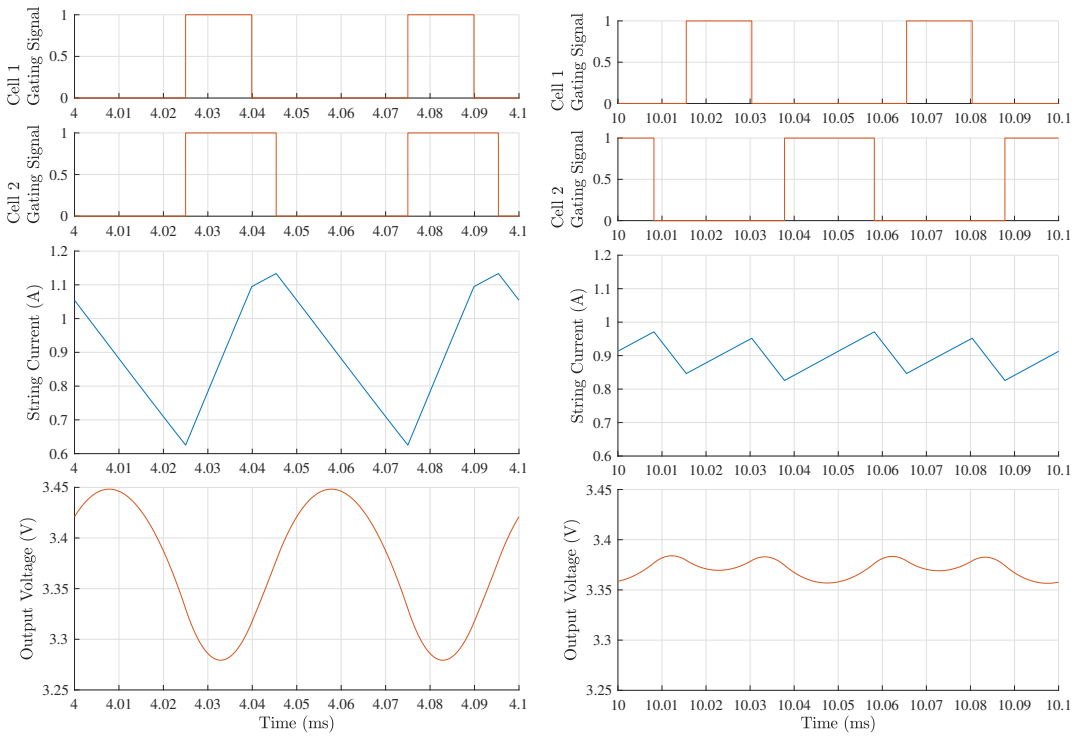
(a) Schematic of the two cell simulation example.

(b) Simulation results showing the voltage across the sensing inductor and its salient features.

Fig. 4.2: A simulation of two smart cells switching.

In addition to sensing, L_{sc} is used as a distributed inductor to provide output filtering. Eventually L_{sc} could be small enough to be implemented on the trace of a PCB, greatly reducing the cost and size of this component. The dc output to the load requires a small filter capacitor, C_{out}, whose capacitance depends on the application requirements.

The first few sections of this chapter focus on the phase controller of Fig. 4.1. Sections 4.2 and 4.3 discuss how all of the information required to solve this problem can be extracted from the local v_L measurement and how the decentralised phase controller can be implemented on low cost hardware. Section 4.4 derives the phase controller and Section 4.5 proves the stability of the phase controller around local minima of (4.11). This chapter concludes with the SOC controller design in Section 4.6.



(a) Synchronized switching pattern of a two cell battery pack.

(b) Optimal switching pattern of a two cell battery pack.

Fig. 4.3: Simulation results of a two cell battery pack operated with synchronized switching pattern and an optimal switching pattern.

4.1 Optimal Switching Pattern

The topology of Fig. 4.1 operates in a similar manner to a multilevel dc to dc converter, just like the intelligent battery of Chapter 2. In a similar manner to the intelligent battery, the switching actions of all of the smart cells could be evenly spaced in time. However, in situations where the duty cycles have large discrepancies, a more optimal switching pattern can be achieved. This section will discuss the mathematics behind finding an optimal switching pattern for a generalized group of M battery modules.

4.1.1 Problem and Assumptions

Given set of M battery cells $B_i = \{B_1, B_2, \ldots, B_M\}$ with capacities $C_i = \{C_1, C_2, \ldots, C_M\}$, our objective is to find a set of phases, $\phi_i = \{\phi_1, \phi_2, \ldots, \phi_M\}$ for the turn-on of each smart cell which will minimize the ripple current in the local inductor L_{sc}, thus minimizing the output ripple voltage.

For simplicity, the nominal voltages of all of the battery cells will be $V_{nom} = V_1 = V_2 = \ldots = V_M$, which is a reasonable assumption if the SOCs of all of the battery cells are synchronized. The duty cycle of each smart cell can be calculated using the following equation:

$$D_i = \frac{C_i}{C_{MAX}} \tag{4.1}$$

where C_{MAX} is the maximum capacity expected amongst all of the battery cells, or ideally, the maximum value found in the capacity array such that $0 < D_i \leq 1$ for all i.

In a series string of smart cells, the voltage applied to each inductor, L_{sc}, will be identical. Thus, we can group all of the distributed inductors together into a single inductor, $L = ML_{sc}$. The voltage across L will be determined by the sum of all of the v_i voltages of the smart cells and the output dc voltage. The output dc voltage is given by (4.2):

$$V_{out} = \sum_{i=1}^{M} D_i V_{nom} = \sum_{i=1}^{M} \frac{C_i}{C_{MAX}} V_{nom} = \frac{V_{nom}}{C_{MAX}} \sum_{i=1}^{M} C_i. \tag{4.2}$$

The ac root mean squared (rms) value of the inductor ripple current can be expressed by (4.3):

$$I_{Lac-rms} = \sqrt{\frac{1}{T_s} \int_0^{T_s} \left[I(s) + \frac{1}{L} \int_s^t \left(v_{out}(\tau) - V_{out} \right) d\tau \right]^2 dt} \tag{4.3}$$

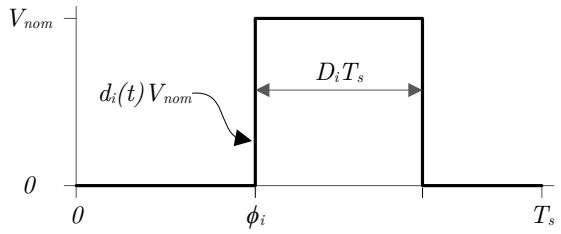


Fig. 4.4: Output voltage, $d_i(t)\,V_{nom}$, of a smart cell with phase ϕ_i, duty cycle D_i, and switching period, T_s.

where $I(s)$ is the anti-derivative of $(v_{out}(s) - V_{out})/L$, τ and s are dummy variables of integration, and t is time. The variable $v_{out}(t)$ is defined by (4.4):

$$v_{out}(t) = \sum_{i=1}^{M} v_i(t) \tag{4.4}$$

where $v_i(t)$ is the output voltage of the i^{th} smart cell as measured from the negative terminal of the battery cell to the output terminal of the transistors, as shown in Fig. 4.1. Therefore, $v_{out}(t)$ is the output voltage of a series string of smart cells.

4.1.2 Determine $I_{Lac-rms}$

In order to determine an optimal set of phase angles, ϕ_i, a function which describes the output of a smart cell in terms of ϕ_i needs to be derived. The output voltage of a smart cell will generally look like a periodic rectangular wave, as shown in Fig. 4.4.

Using the generalized values in Fig. 4.4, the Fourier Series representation of the output voltage of any smart cell can be derived and it is shown in (4.5) - (4.9).

$$v_i(t) = d_i(t)\,V_{nom} \tag{4.5}$$

$$d_i(t) = \frac{a_{0i}}{2} + \sum_{n=1}^{\infty}\left[a_{ni}\cos\left(\frac{2\pi nt}{T_s}\right) + b_{ni}\sin\left(\frac{2\pi nt}{T_s}\right)\right] \tag{4.6}$$

where:

$$a_{0i} = 2D_i \tag{4.7}$$

$$a_{ni} = \frac{1}{n\pi}\left(\sin\left(2\pi n\left(D_i + \frac{\phi_i}{T_s}\right)\right) - \sin\left(2\pi n\frac{\phi_i}{T_s}\right)\right) \tag{4.8}$$

$$b_{ni} = \frac{1}{n\pi}\left(\cos\left(2\pi n\frac{\phi_i}{T_s}\right) - \cos\left(2\pi n\left(D_i + \frac{\phi_i}{T_s}\right)\right)\right) \tag{4.9}$$

Now we can substitute (4.5) into (4.4) and solve for $I^2_{Lac-rms}$ using (4.3). It can be shown that the result is:

$$I^2_{Lac-rms} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4} \left[\sin\left(\pi n D_i\right)\sin\left(\pi n D_j\right)\cos\left(\pi n\left(D_i - D_j + 2\frac{\phi_i}{T_s} - 2\frac{\phi_j}{T_s}\right)\right)\right] \tag{4.10}$$

Now let $\theta_x = 2\pi\phi_x/T_s$, so that the switching angles can be measured in radians instead of time:

$$I^2_{Lac-rms} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4}\cdot \left[\sin\left(\pi n D_i\right)\ \sin\left(\pi n D_j\right)\cos\left(\pi n\left(D_i - D_j\right) + n\left(\theta_i - \theta_j\right)\right)\right] \tag{4.11}$$

Equation (4.11) can now be minimized to determine an optimal set θ_i that will minimize the ac rms current in the inductor L_{sc} and, therefore, the output voltage ripple in v_{out}.

4.2 Simplifying the problem

In the previous section, an expression for the ac rms ripple current in the intelligent battery's inductors in terms of each module's duty cycle and phase shift was derived in (4.11).

Examining (4.11), we see that solving for an optimal set $\boldsymbol{\theta}$ to minimize $I_{Lac-rms}$ is non trivial and difficult to achieve without significant computational power and global information about the system. Therefore, in this section we present a way to identify a set $\boldsymbol{\theta}$ which will yield a satisfactory solution, with significantly less computational requirements and in a decentralized fashion.

First, let us represent the switching action of the k^{th} smart cell as a vector, v_k, in the unit circle as depicted in Fig. 4.5. The k^{th} smart cell will turn on at θ_k and turn off at $\theta_k + 2\pi D_k$. Now define a new vector, v'_k, which will be known as the weighted vector, whose phase places the vector half way between the turn on and turn off times and whose length is $\sin(\pi D_k)$. Therefore, the phase and length of the weighted vector, v'_k, are given by:

$$\angle v'_k \triangleq \theta'_k = \theta_k + \pi D_k \tag{4.12}$$

$$|v'_k| \triangleq \sin(\pi D_k). \tag{4.13}$$

Applying the transformation described in (4.12) and (4.13) to all of the smart cells, and summing all v'_k, we can find the square of the magnitude of the total sum vector, $|v'_\Sigma|^2$:

$$|v'_\Sigma|^2 = \sum_{i=1}^{M}\sum_{j=1}^{M} \sin(\pi D_i)\sin(\pi D_j)\cos(\pi(D_i - D_j) + \theta_i - \theta_j). \tag{4.14}$$

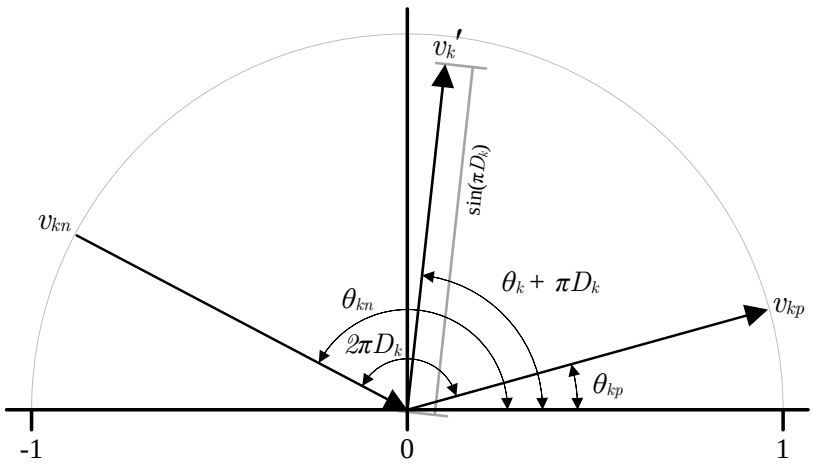


Fig. 4.5: Representing the switching action of the k^{th} smart cell as a vector, with its weighted, phase shifted vector, v_k'. The switching actions of the k^{th} smart cell are also shown as vectors v_{kp} and v_{kn}.

Equation (4.14) has the exact same form as (4.11) when $n = 1$ (i.e. only the fundamental is considered). Therefore, one control algorithm that will yield a sub-optimal but acceptable minimum of (4.11) is to minimize the magnitude of the total sum vector, $|v_\Sigma'|^2$.

4.3 Extracting information from v_L

In order to minimize the magnitude of the total sum vector, $|v_\Sigma'|^2$, found in (4.14), the duty cycle and phase shift of every smart cell in the string is still required. This section will show how all of the necessary information required to calculate $|v_\Sigma'|^2$ can be obtained from v_L, the voltage across the filtering inductor L_{sc}.

As shown in Fig. 4.2(b), every time a smart cell switches in and out of the string, this transition is captured by every sense inductor, L_{sc}, in the string of smart cells. Using Fig. 4.5 as reference, from the point of view of a single smart cell, it will see the switching actions of the k^{th} smart cell as two corresponding voltage transitions: a positive voltage transition across the inductor L_{sc}, depicted by the vector v_{kp} with switching angle θ_{kp}; and its negative corresponding voltage transition, depicted by the

vector v_{kn} with switching angle θ_{kn}. For a smart cell detecting only one other smart cell, the problem is trivial and it is easy to determine not only when the other smart cell is switching, but its duty cycle as well.

The challenge arises when multiple smart cells start switching. As soon as a single smart cell needs to determine the switching angles and duty cycles of two or more other smart cells, it is impossible to match every "on" transition with its corresponding "off" transition. We will now show that this is not necessary to yield the optimal solution as defined by (4.14).

First, use (4.15) and (4.16) to replace all of the D_x's and θ_x's with the notation of Fig. 4.5.

$$\theta_i = \theta_{ip} \tag{4.15}$$

$$\pi D_i = \left(\frac{\theta_{in} - \theta_{ip}}{2}\right) \tag{4.16}$$

This yields an expression in terms of measured quantities:

$$|v'_\Sigma|^2 \;=\; \sum_{i=1}^{M}\sum_{j=1}^{M} \sin\left(\frac{\theta_{in} - \theta_{ip}}{2}\right) \sin\left(\frac{\theta_{jn} - \theta_{jp}}{2}\right) \cos\left(\left(\frac{\theta_{in} + \theta_{ip}}{2}\right) - \left(\frac{\theta_{jn} + \theta_{jp}}{2}\right)\right). \tag{4.17}$$

Equation (4.17) gives the magnitude of the total vector in terms of quantities measured by each smart cell. However, this equation still seems to imply that the "on" transitions must be correctly paired with each of their corresponding "off" transitions. We will now show that this is not the case by first considering the case where only one set of "on" transitions are swapped. Consider a set of M smart cells, where the k^{th} and

l^{th} positive transitions are paired with the l^{th} and k^{th} negative transitions, respectively. Using MATLAB's Syms toolbox, it can be shown that:

$$
\begin{aligned}
&\left|v'_{\Sigma}\right|^2 = \\
&\sum_{\substack{i=1 \\ i\neq k, i\neq l}}^{M} \sum_{\substack{j=1 \\ j\neq k, j\neq l}}^{M} \left[\sin\left(\frac{\theta_{in}-\theta_{ip}}{2}\right)\sin\left(\frac{\theta_{jn}-\theta_{jp}}{2}\right)\cos\left(\left(\frac{\theta_{in}+\theta_{ip}}{2}\right) - \left(\frac{\theta_{jn}+\theta_{jp}}{2}\right)\right)\right] \\
&+\sin^2\left(\frac{\theta_{kn}-\theta_{lp}}{2}\right)+\sin\left(\frac{\theta_{ln}-\theta_{kp}}{2}\right)\sin\left(\frac{\theta_{kn}-\theta_{lp}}{2}\right)\cos\left(\left(\frac{\theta_{ln}+\theta_{kp}}{2}\right) - \left(\frac{\theta_{kn}+\theta_{lp}}{2}\right)\right) \\
&+\sin^2\left(\frac{\theta_{ln}-\theta_{kp}}{2}\right)+\sin\left(\frac{\theta_{1n}-\theta_{kp}}{2}\right)\sin\left(\frac{\theta_{ln}-\theta_{kp}}{2}\right)\cos\left(\left(\frac{\theta_{kn}+\theta_{lp}}{2}\right) - \left(\frac{\theta_{ln}+\theta_{kp}}{2}\right)\right) \\
&= \sum_{i=1}^{M}\sum_{j=1}^{M}\sin\left(\frac{\theta_{in}-\theta_{ip}}{2}\right)\sin\left(\frac{\theta_{jn}-\theta_{jp}}{2}\right)\cos\left(\left(\frac{\theta_{in}+\theta_{ip}}{2}\right) - \left(\frac{\theta_{jn}+\theta_{jp}}{2}\right)\right). \quad (4.18)
\end{aligned}
$$

By extension, we can swap any pair and any number of transitions with each other and get the same result. Therefore, in order to minimize the total sum vector of (4.14), each smart cell need only know when the positive and negative transitions *occur* to determine its local optimal switching pattern. Moreover, it can be shown that these results are also true for all harmonics, 1 to n.

4.4 Phase Controller Design

The smart cell controller needs to be designed such that a group of cells working together will minimize (4.14). By taking the derivative of (4.14) with respect to the phase angles and setting it to zero, the local minima can be found. The partial derivative of (4.14) with respect to θ_k is shown below:

$$
\frac{\partial\left|v'_{\Sigma}\right|^2}{\partial\theta_k} = 2\sin\left(\pi D_k\right)\sum_{i=1;i\neq k}^{M}\sin\left(\pi D_i\right)\sin\left(\pi\left(D_i-D_k\right)+\theta_i-\theta_k\right) \quad (4.19)
$$

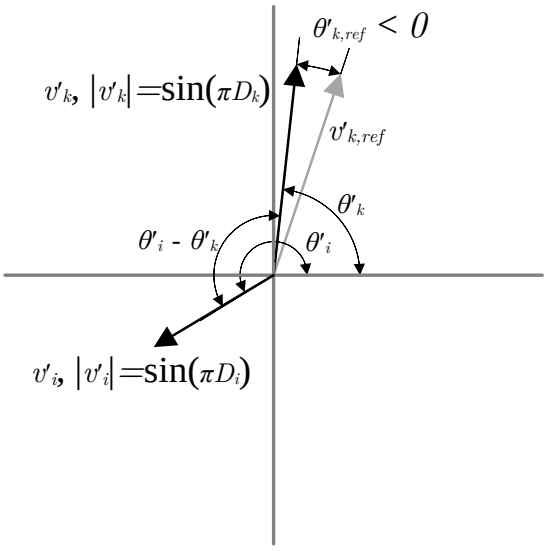


Fig. 4.6: Graphical representation of the weighted vectors v'_k and v'_i. By pointing these two vectors in the opposite direction, (4.14) will be minimized. This is accomplished with the controller of (4.20).

Graphically, setting (4.19) to zero is equivalent to "pointing" the weighted vector v'_k in either 1) an opposite direction, or 2) the same direction, to all of the other weighted vectors $v'_{i,i\neq k}$ summed together. Clearly, "pointing" v'_k in the same direction as $\sum_i v'_{i,i\neq k}$ would result in large currents in the inductor since all of the cells would eventually be in phase, maximizing the ripple current. However, if we chose to direct v'_k in the *opposite* direction to $\sum_i v'_{i,i\neq k}$, the current through the inductors will be reduced. Fig. 4.6 summarizes this observation.

Therefore, during each iteration of the smart cell controller, every smart cell will sum up the weighted vectors of all of the other smart cells it senses, and set its local reference to be 180 degrees away from that sum. By doing this, each smart cell will be driving (4.19) to zero, thus finding a local minimum to (4.14). Using this controller design, (4.20) defines the reference angle, $\theta'_{k,ref}$, for the kth smart cell's weighted sum vector, v'_k.

$$\theta'_{k,ref} = -2\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\sin(\pi D_i)\sin(\pi(D_i - D_k) + \theta_i - \theta_k) \tag{4.20}$$

Note the negative sign in (4.20), this ensures that that the angle between $\theta'_{k,ref}$ and $\sum_i v'_{i,i\neq k}$ is driven to π. Using (4.20) and the angle transformation of (4.12), a non-linear model for the phase (θ'_k) of the k^{th} smart cell can be constructed and is shown below:

$$\dot{\theta'_k} = \omega_k - 2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\sin(\pi D_i)\sin(\theta'_i - \theta'_k) \tag{4.21}$$

where ω_k is the switching frequency, and K is a controller constant.

4.5 Phase Controller Stability Analysis

Using the smart cell controller model developed in Section 4.4, the stability of a group of smart cells around local minima of (4.19) will be investigated. First note that the controller chosen in (4.21) is very similar to the Kuramoto Model of coupled oscillators [102], which is repeated in (4.22):

$$\dot{\theta_k} = \omega + \frac{K}{M}\sum_{i=1}^{N}\sin(\theta_i - \theta_k), \tag{4.22}$$

where ω is the nominal switching frequency of the system, M is the number of agents, and K is a global controller constant, identical for all agents (coupled oscillators).

Second, consider the dynamics of the system described by (4.21) in a rotating reference frame, where all of the ω_k's are equal, thus $\omega_k = \omega$, and let

$$\theta'_k = \omega t + \gamma'_k. \tag{4.23}$$

Equation (4.21) becomes:

$$\dot{\gamma'_k} = -2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\sin(\pi D_i)\sin(\gamma'_i-\gamma'_k) = f_k(\mathbf{\Gamma'}) \tag{4.24}$$

where $\mathbf{\Gamma'} = \{\gamma'_1, \gamma'_2, \ldots \gamma'_M\}$. Linearise $f_k(\mathbf{\Gamma'})$ around the equilibrium point $\mathbf{\Gamma'^\star} = \{\gamma'^\star_1, \gamma'^\star_2, \ldots \gamma'^\star_M\}$ to assess the stability of a group of smart cells around a local minimum of 4.14.

$$\dot{\gamma'_k} = f_k(\mathbf{\Gamma'}) \approx f_k(\mathbf{\Gamma'^\star}) + \sum_{j=1}^{M}\frac{\partial f_k(\mathbf{\Gamma'})}{\partial\gamma'_j}\bigg|_{\mathbf{\Gamma'^\star}}\left(\gamma'_j-\gamma'^\star_j\right) \tag{4.25}$$

$$\begin{aligned}\dot{\gamma'_k} \approx -2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\sin(\pi D_i)\sin(\gamma'^\star_i-\gamma'^\star_k) + \\ \sum_{j=1}^{M}\frac{\partial}{\partial\gamma'_j}\left(-2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\sin(\pi D_i)\sin(\gamma'_i-\gamma'_k)\right)\bigg|_{\mathbf{\Gamma'^\star}}\left(\gamma'_j-\gamma'^\star_j\right)\end{aligned} \tag{4.26}$$

The first term of 4.26 is zero because the function $f_k(\mathbf{\Gamma'})$ is evaluated at the equilibrium point $\mathbf{\Gamma'^\star}$, which by definition, is zero. The second term of 4.26 must be considered in two cases: one where $j \neq k$, and another where $j = k$. This is written explicitly as:

$$\begin{aligned}\dot{\gamma'_k} \approx \sum_{j=1;j\neq k}^{M}\left(-2\frac{K}{M}\sin(\pi D_k)\sin(\pi D_j)\cos\left(\gamma'^\star_j-\gamma'^\star_k\right)\left(\gamma'_j-\gamma'^\star_j\right)\right) + \\ 2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\left(\sin(\pi D_i)\cos(\gamma'^\star_i-\gamma'^\star_k)\right)(\gamma'_k-\gamma'^\star_k).\end{aligned} \tag{4.27}$$

Perform another change of variables to centre the equilibrium point of 4.27 about the origin. Let:

$$\delta'_x = \gamma'_x - \gamma'^\star_x, \tag{4.28}$$

it follows that:

$$\dot{\delta}'_x = \dot{\gamma}'_x. \tag{4.29}$$

Therefore:

$$\dot{\delta}'_k \approx \sum_{j=1;j\neq k}^{M} \left(-2\frac{K}{M}\sin(\pi D_k)\sin(\pi D_j)\cos\left(\gamma'^{\star}_j - \gamma'^{\star}_k\right)\delta'_j\right) + 2\frac{K}{M}\sin(\pi D_k)\sum_{i=1;i\neq k}^{M}\left(\sin(\pi D_i)\cos\left(\gamma'^{\star}_i - \gamma'^{\star}_k\right)\right)\delta'_k. \tag{4.30}$$

Put 4.30 in matrix form, using s_x as a short-hand for $\sin(\pi D_x)$:

$$\dot{\boldsymbol{\Delta}}' \approx \begin{bmatrix} 2\frac{K}{M}\mathrm{s}_1\sum_{i=1;i\neq 1}^{M}\left(\mathrm{s}_i\cos\left(\gamma'^{\star}_i - \gamma'^{\star}_1\right)\right) & -2\frac{K}{M}\mathrm{s}_1\mathrm{s}_2\cos\left(\gamma'^{\star}_2 - \gamma'^{\star}_1\right) & \cdots & -2\frac{K}{M}\mathrm{s}_1\mathrm{s}_M\cos\left(\gamma'^{\star}_M - \gamma'^{\star}_1\right) \\ -2\frac{K}{M}\mathrm{s}_2\mathrm{s}_1\cos\left(\gamma'^{\star}_1 - \gamma'^{\star}_2\right) & 2\frac{K}{M}\mathrm{s}_2\sum_{i=1;i\neq 1}^{M}\left(\mathrm{s}_i\cos\left(\gamma'^{\star}_i - \gamma'^{\star}_2\right)\right) & \cdots & -2\frac{K}{M}\mathrm{s}_2\mathrm{s}_M\cos\left(\gamma'^{\star}_M - \gamma'^{\star}_2\right) \\ \vdots & \vdots & \ddots & \vdots \\ -2\frac{K}{M}\mathrm{s}_M\mathrm{s}_1\cos\left(\gamma'^{\star}_1 - \gamma'^{\star}_M\right) & -2\frac{K}{M}\mathrm{s}_M\mathrm{s}_2\cos\left(\gamma'^{\star}_2 - \gamma'^{\star}_M\right) & \cdots & 2\frac{K}{M}\mathrm{s}_M\sum_{i=1;i\neq 1}^{M}\left(\mathrm{s}_i\cos\left(\gamma'^{\star}_i - \gamma'^{\star}_M\right)\right) \end{bmatrix} \cdot \begin{bmatrix} \delta'_1 \\ \delta'_2 \\ \vdots \\ \delta'_M \end{bmatrix}. \tag{4.31}$$

This creates the linear system:

$$\dot{\boldsymbol{\Delta}}' = -\frac{K}{M}\boldsymbol{L}\cdot\boldsymbol{\Delta}', \tag{4.32}$$

where each element, L_{ij}, of the matrix $\boldsymbol{L}$ is defined explicitly as:

$$L_{ij} = \begin{cases} -2\sin(\pi D_j)\sum_{i=1;i\neq j}^{M}\sin(\pi D_i)\cos\left(\gamma_i^\star - \gamma_j^\star\right), & i = j \\ 2\sin(\pi D_j)\sin(\pi D_i)\cos\left(\gamma_i^\star - \gamma_j^\star\right), & i \neq j \end{cases}. \tag{4.33}$$

The matrix $\boldsymbol{L}$ can also be represented by the partial derivatives of (4.14). Letting $\boldsymbol{\Theta}^\star = \{\theta_1^\star, \theta_2^\star, \cdots, \theta_M^\star\}$ be the corresponding equilibrium point of $\boldsymbol{\Gamma}'^\star$ yields:

$$\boldsymbol{L} = \begin{bmatrix} \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_1^2}\right|_{\boldsymbol{\Theta}^\star} & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_1\partial\theta_2}\right|_{\boldsymbol{\Theta}^\star} & \cdots & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_1\partial\theta_M}\right|_{\boldsymbol{\Theta}^\star} \\ \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_2\partial\theta_1}\right|_{\boldsymbol{\Theta}^\star} & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_2^2}\right|_{\boldsymbol{\Theta}^\star} & \cdots & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_2\partial\theta_M}\right|_{\boldsymbol{\Theta}^\star} \\ \vdots & \vdots & \ddots & \vdots \\ \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_M\partial\theta_1}\right|_{\boldsymbol{\Theta}^\star} & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_M\partial\theta_2}\right|_{\boldsymbol{\Theta}^\star} & \cdots & \left.\frac{\partial^2\left|v_\Sigma'\right|^2}{\partial\theta_M^2}\right|_{\boldsymbol{\Theta}^\star} \end{bmatrix}. \tag{4.34}$$

Equation (4.34) is the Hessian of the total sum vector, $\left|v_\Sigma'\right|^2$ of (4.14) evaluated at $\boldsymbol{\Theta}^\star$. Since we chose $\boldsymbol{\Theta}^\star$ to be a local minimum of (4.14), we also know that (4.34) is positive semi-definite. Therefore, all of the eigenvalues of $-\boldsymbol{L}$ are all less than or equal to zero. As a consequence, the local minimum point, $\boldsymbol{\Theta}^\star$, is an asymptotically attracting equilibrium point and therefore, a stable operating point.

It is not possible for $\boldsymbol{L}$ to be positive definite. This is due to the cyclic nature of oscillatory systems. For example, if $\boldsymbol{\Theta}^\star$ is a local minimum, then so is $\boldsymbol{\Theta}^\star + x$, where x is any angle. However, since we are only concerned about the relative angle between the smart cells to minimize (4.14), this is expected.

4.6 SOC Controller Design

The SOC of each smart cell is regulated by synchronizing its SOC with the average SOC of a series string of smart cells, which is determined by analysing v_L, the voltage across the sense inductor, L_{sc}. The SOC controller relies on the string of smart cells

being composed of cells of the same chemistry, so that there is a consistent relationship between the SOC and cell terminal voltage throughout the string.

As shown in Fig. 4.2(b), every time a smart cell switches in and out of the string, the voltage that it switches will be sensed by all of the sense inductors in the string of smart cells. Therefore, by calculating the differences in the levels of the v_L waveform, the terminal voltage of the cell that switched in or out can be extracted by each smart cell. Averaging all of these differences yields an average terminal voltage for the series string of smart cells. In order to yield an accurate average voltage measurement, two parasitic properties of the inductor must be overcome: 1) non-linear inductance due to inductor saturation, and 2) variations in inductance.

Real inductors suffer from non-linear inductance as the current through them increases beyond their rated saturation current. This non-linear inductance will manifest itself as a variable gain in the measurements of the levels v_L waveform, which is undesirable. Therefore, the smart cell inductors should be designed in a manner such that they are operated within their linear region. Operation in the linear region is assisted by the phase controller, which will minimize the ripple current in the inductors, and thus minimize their peak current.

In order to account for variations in the inductance of L_{SC} and the sensing hardware, the gain of the v_L sensor is measured and adjusted every time the SOC controller is executed. Since the local cell knows its duty cycle and phase, it can determine which transitions in the v_L waveform are caused by its cell switching in and out of the circuit. Using these transitions, along with the local cell voltage measurement, the local cell can calculate the gain of its v_L sensor to accurately determine the voltages of the other cells switching in and out of the circuit.

The SOC controller adjusts the duty cycle of the local cell using a simple proportional-integral (PI) controller to synchronize its terminal voltage with the string's average

terminal voltage. The PI controller was tuned in the lab through a number of experiments.

4.7 Summary and discussion

This chapter presented the theory behind converting an intelligent battery with a centralized controller into a group of smart cells which does not rely on any inter-cell communication. In order to achieve this, a small filtering inductor has been introduced into each cell and augmented to be a multi-purpose sensor. There are two tasks the smart cell controller must accomplish: 1) synchronize its switching actions with the string of smart cells it is connected to, with a phase shift that minimizes the output voltage ripple; and 2) synchronize its terminal voltage with the terminal voltages of the other smart cells in the series string.

The output voltage minimization task was simplified to only include the first harmonic and this simplification will be studied in more detail in the next section. However, a detailed analysis of the theoretical implications of the simplification are shown in Appendix A, where a conservative lower bound on $I_{Lac\text{-}rms}$ is derived and repeated here for convenience:

$$I_{Lac-rms} = \left(\frac{(\lceil MD_{eq} \rceil - MD_{eq})\, V_n}{ML_{sc}}\right)\left(\frac{(MD_{eq} - \lfloor MD_{eq} \rfloor)\, T_s}{2M}\right)\left(\frac{1}{\sqrt{3}}\right) \tag{4.35}$$

where:

$$MD_{eq} = \sum_{i=1}^{M} D_i. \tag{4.36}$$

Although the stability analysis of a group of smart cells was limited to proving that a group of smart cells is stable around local minima of (4.14), theoretical analyses of

systems described by Kuramoto oscillators is a challenging subject that has been an on-going area of research since its introduction in 1975 [103].

Chapter 5

Smart cell simulations and experimental results

This chapter puts the theory of Chapter 4 into practice. Simulations to verify the smart cell algorithms are presented, followed by experimental results on low cost hardware. The chapter concludes with a discussion which highlights, in particular, some of the challenges that arose in building the experimental set-up.

5.1 Simulation results

Simulation results of the decentralised control strategies of Chapter 4 were conducted using MATLAB's Simulink environment. This development environment was ideal to develop and debug the complex control algorithms and, once completed, export the algorithms as generated C-code for implementation on experimental hardware in the laboratory.

5.1.1 Implementation of the control algorithm

A MATLAB-Simulink model of a smart cell using the theory developed in this work was built using the SimPowerSystems toolbox. The model uses the Simscape battery model and MOSFETs to simulate the power circuit. The controller was implemented as an embedded MATLAB function and was executed once per switching cycle when the upper MOSFET, Q_H, was switched on.

Fig. 5.1 illustrates the algorithm the controller implemented as a block diagram. Steps 1 through 5 were implemented by the embedded MATLAB function.

1. **Signal Processor:** Detects all of the positive and negative transitions that occur during every switching cycle, T_s. The local cell voltage, V_{local}, and the average cell voltage, V_{avg}, are measured using the levels of the v_L waveform. The edge detector also counts the number of transitions, divides the total by two, and feeds the result through a low pass filter to keep track of the number of smart cells in the string. The output of this low pass filter is also used to verify that all of the edges have been detected. Using the low pass filter output and the differences between the levels in the v_L waveform, transition points where more than one smart cell switches on or off at the same time can be detected and properly accounted for.

2. **Calculate $\theta'_{k,ref}$:** A new reference phase shift is calculated using (4.20).

3. **Calculate $\theta'_{k,new}$:** The new phase that is sent to the PWM generator is calculated by the phase controller.

4. **Apply limits:** $\pm 2\pi$ is added to $\theta'_{k,ref}$ until it lies between $-\pi$ and π.

5. **SOC Controller:** A new duty cycle is computed using V_{local} and V_{avg}. The updated duty cycle, D_k, is sent to the PWM module.

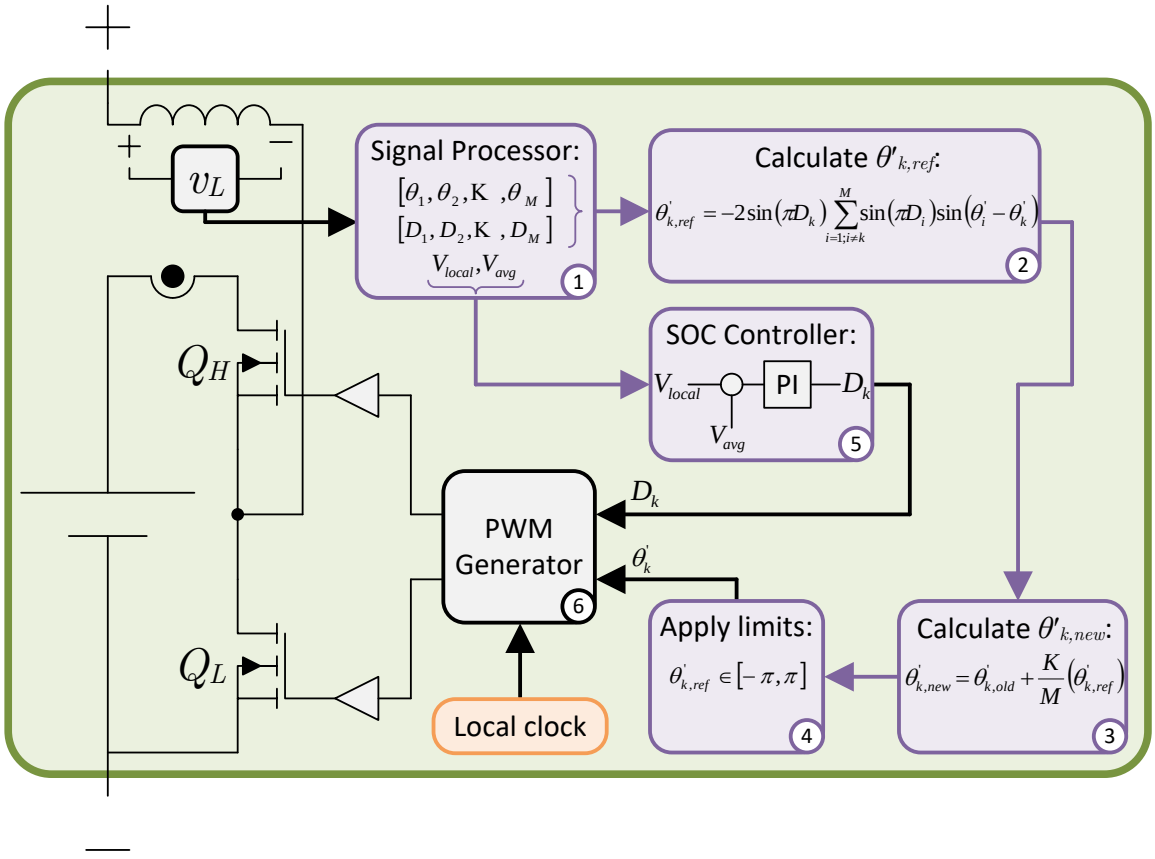


Fig. 5.1: Control block diagram of a smart cell built in MATLAB-Simulink. The steps 1 to 5 outlined in purple, are implemented in an embedded MATLAB function.

6. **PWM Generator:** $\theta'_{k,new}$ is used by the PWM generator to produce gating signals for the MOSFETs.

The phase control loop, defined by steps 1 to 4 in Fig. 5.1, ran one hundred times faster than the SOC control loop. The SOC control loop is defined by steps 1 and 5, and did not modify the duty cycle unless the phase controller reached a steady state value. Every smart cell had a locally generated clock signal for their PWM generators, which was *not* sourced or synchronised globally.

The embedded MATLAB function that implements the controllers was converted into C++ code by MATLAB's coder toolbox, for easy integration into the hardware.

5.1.2 Continuous time simulation study of the phase controller

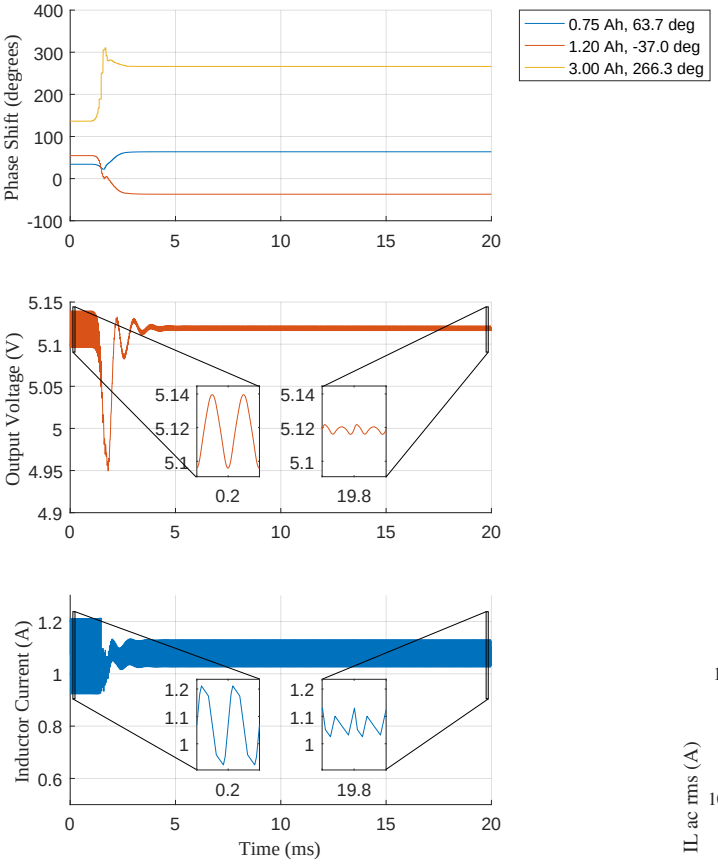
This subsection describes the testing of the phase controller implemented in Section 5.1.1 with a number of different system configurations, using "continuous time". The term continuous time is used in this context to describe a system of smart cells not limited by hardware sampling rates and resolutions, something that will be explored in the next subsection.

Four configurations were considered for this study: 3, 5, 10, and 20 smart cells in series. For each configuration, two plots are shown: 1) a time evolution plot; and 2) a bar chart comparing the ac rms ripple current reduction in the inductors. The common system configurations are listed in Table 5.1, recalling that X_u is a random number uniformly distributed between 0 and 1.. The cell capacities simulated for each configuration are listed in the legend of each time evolution plot.

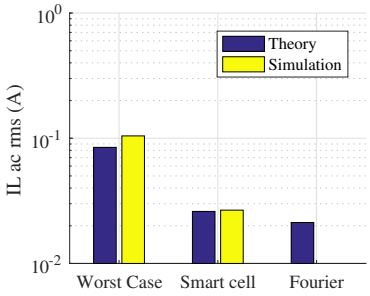
Table 5.1: Parameters used throughout the continuous time simulation studies of the smart cell phase controller.

Description	**Parameter**	**Value**
Module inductance	L_{sc}	100 µH
Output capacitance	C_{out}	54.7 µF
Switching frequency	f_s	20 kHz
Switching period	T_s	50 µs
On resistance of module MOSFETs	R_{DS-on}	10 mΩ
Nominal cell voltage	V_{nom}	3.6 V
State of charge	SOC_k	100%
Phase controller activation time	t_{ph-on}	1 ms
Cell capacity	C_k	$X_u \times 4$ Ah
Maximum cell capacity	C_{max}	4.0 Ah
Phase controller gain	K	2.0

3 smart cells



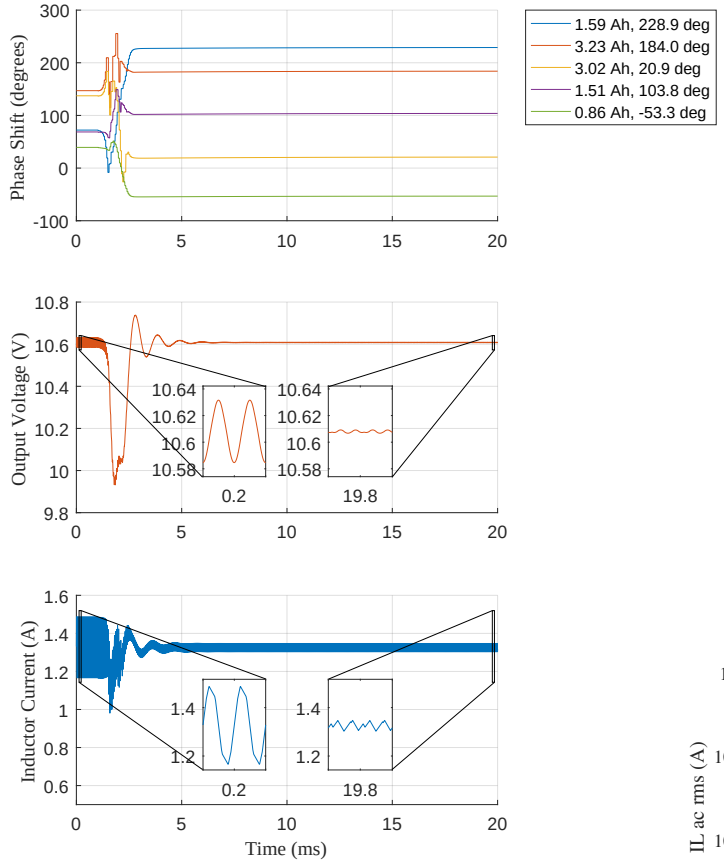
(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 44 mV to 6 mV. The ac rms current in the inductor is improved from 104 mA rms to 26 mA rms.



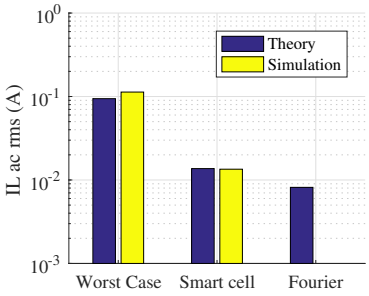
(b) A comparison of $I_{Lac\text{-}rms}$ values of a three smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled “Fourier”.

Fig. 5.2: Continuous time simulation results of a three smart cell system.

5 smart cells

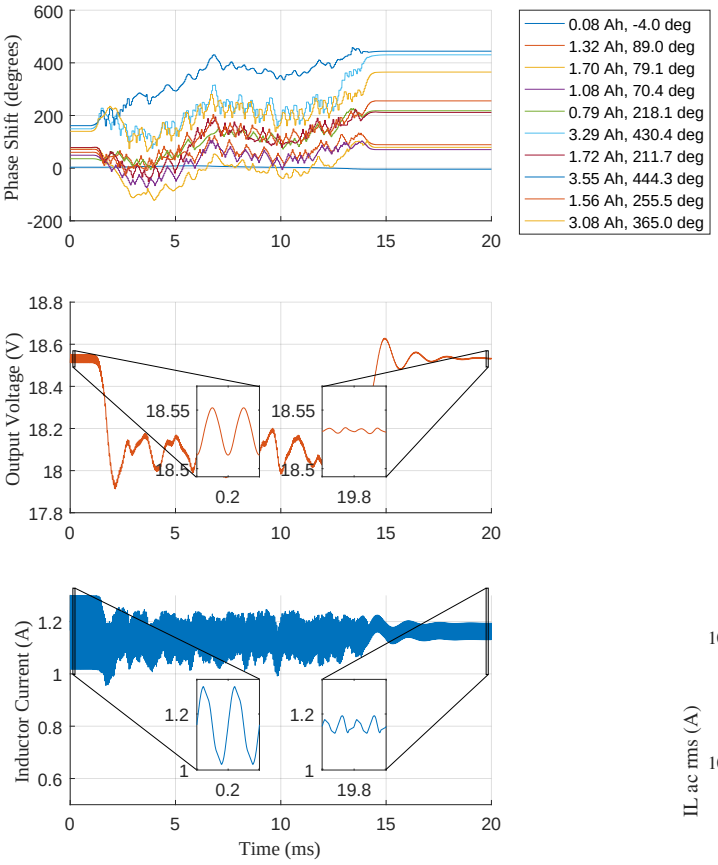


(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 47 mV to 2 mV. The ac rms current in the inductor is improved from 113 mA rms to 13 mA rms.

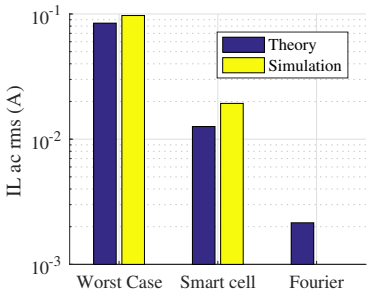


(b) A comparison of $I_{Lac\text{-}rms}$ values of a five smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.3: Continuous time simulation results of a five smart cell system.



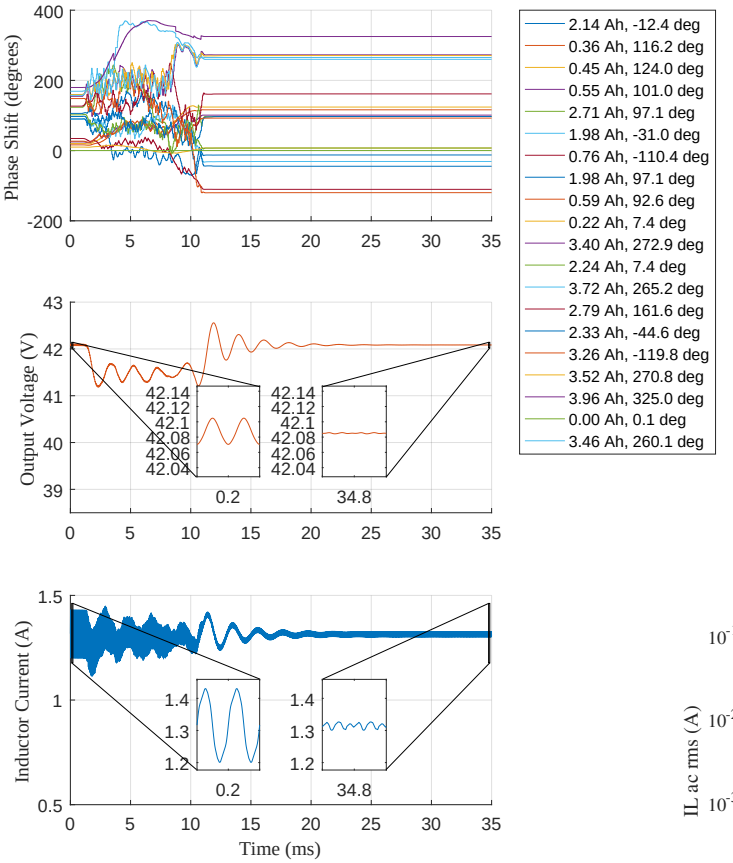
(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 40 mV to 5 mV. The ac rms current in the inductor is improved from 97 mA rms to 19 mA rms.



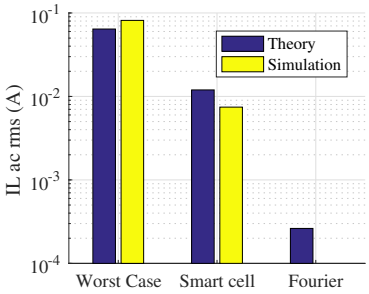
(b) A comparison of $I_{Lac\text{-}rms}$ values of a ten smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.4: Continuous time simulation results of a ten smart cell system.

20 smart cells



(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 35 mV to 2 mV. The ac rms current in the inductor is improved from 81 mA rms to 7 mA rms.



(b) A comparison of $I_{Lac\text{-}rms}$ values of a twenty smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.5: Continuous time simulation results of a twenty smart cell system.

Summary and discussion

In the simulation results of Fig. 5.2, Fig. 5.3, Fig. 5.4, and Fig. 5.5, each smart cell within each set was operating completely independently of each other. At the start of the simulation, the cells were configured into their worst case switching pattern, where all of their weighted vectors (defined by (4.12) and (4.13)) were in phase with each other. The phase controller was turned on 1.0 ms into the simulation. A value of $C_{MAX} = 4.00$ Ah was pre-programmed into each smart cell, in order for each smart cell to calculate its local duty cycle according to (4.1). Table 5.2 summarizes the improvements to the peak-to-peak output voltage ripple and ac rms ripple current in the inductor made when the smart cell phase controller was engaged during the phase controller simulation study. These improvements can also be seen in the inset graphs from each simulation result.

The elegance of the phase controller comes from its fairly simple task of calculating its reference phase shift according to (4.20). When all smart cells were executing this control algorithm, they were effectively solving the minimization problem of (4.14) together.

In all four cases, the system of smart cells was able to stabilize around a local minima. The local minima found by the simulations is sometimes different from the theoretical results in the bar graphs. This is because the theoretical results use the interior point algorithm implemented by MATLAB's `fmincon` function to minimize (4.14) and is therefore able to find better solutions more easily. The simulation results are more likely to settle into a local minima depending on their starting state, as the system evolves smoothly over time. The smart cell controllers are like a ball rolling over the solution space together: when they find a valley, they stay there. In contrast, an interior point algorithm is able to move around the solution space more easily, before converging to a final solution.

The bar graphs also included a theoretical result labelled "Fourier". This result was calculated using MATLAB's `fmincon` function, but it minimized (4.11) using the first 500 harmonics. Therefore, this theoretical result is an indication of how much more of an improvement to the ripple voltage and current can be achieved if the simplification of using only the fundamental harmonic was not undertaken. As expected, the theoretical "Fourier" result is increasingly superior as the number of cells increase. In Fig. 5.2 and Fig. 5.3 the ripple current of the smart cell controller is very similar to the Fourier result. However, in the 20 cell simulation of Fig. 5.5 the Fourier result is almost 10 times better than the smart cell result. This is because the high frequency components of (4.11) are necessary to capture the increasing number of switching events. Even so, there is an order of magnitude improvement in the ripple current by just using the first harmonic. Furthermore, not only is there a ripple current reduction by using the phase controller, the ripple current is also stable and predictable. In a real system where the switching frequencies will not be exactly the same, the ripple current will fluctuate during operation, which is undesirable. This will be discussed further in Section 5.2.2..

The amount of ripple current and ripple voltage reduction will depend heavily on the duty cycles of the smart cells, thus a different group of smart cells may have less or more ripple reduction than shown here.

Table 5.2: Summary of performance improvements using the smart cell phase controller.

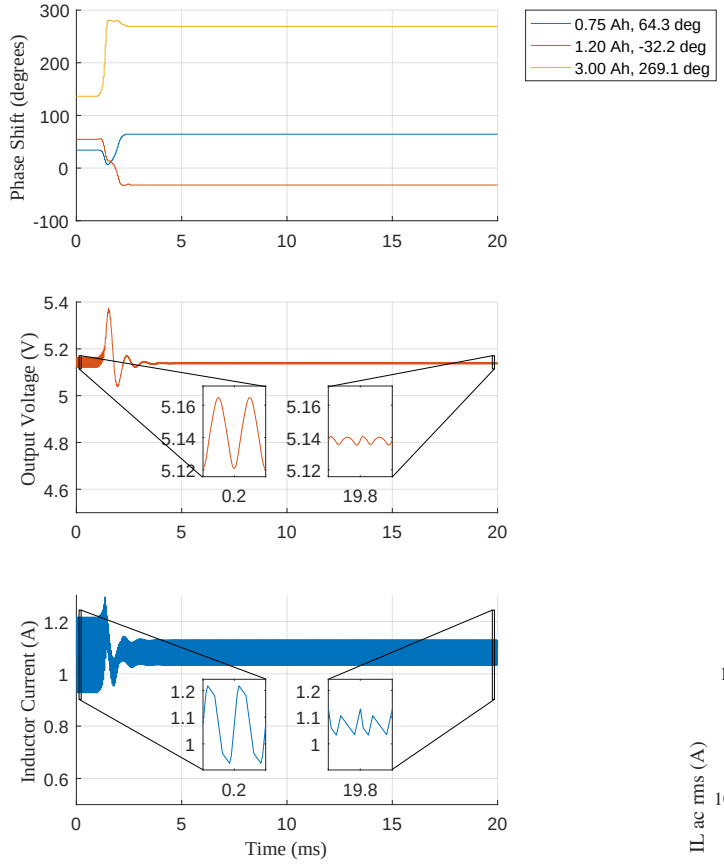
Number of Cells	**Worst Case**		**Smart Cell Control**	
	$V_{out\text{-}pp}$	$I_{Lac\text{-}rms}$	$V_{out\text{-}pp}$	$I_{Lac\text{-}rms}$
3	44 mV	104 mA rms	6 mV	26 mA rms
5	47 mV	113 mA rms	2 mV	13 mA rms
10	40 mV	97 mA rms	5 mV	19 mA rms
20	35 mV	81 mA rms	2 mV	7 mA rms

5.1.3 Discrete time simulation study of the phase controller

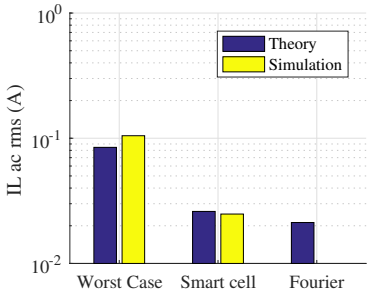
Practical systems will be limited by the sampling hardware when implementing the smart cell algorithms. Therefore, this subsection explores the effects of discretisation on the sampling of the voltage across L_{sc}. For these simulations, the same parameters of Table 5.1 are used, with the exception of, and in addition to, those found in Table 5.3. The additional parameters of Table 5.3 are based off of the hardware that is used in the experimental results later in this chapter.

Table 5.3: Parameters used in the discrete time simulations of the smart cell phase controller.

Description	**Parameter**	**Value**
Phase controller gain	K	2.0
ADC resolution	ADC_b	12 bit
ADC sampling rate	ADC_{fs}	2.4 Msps

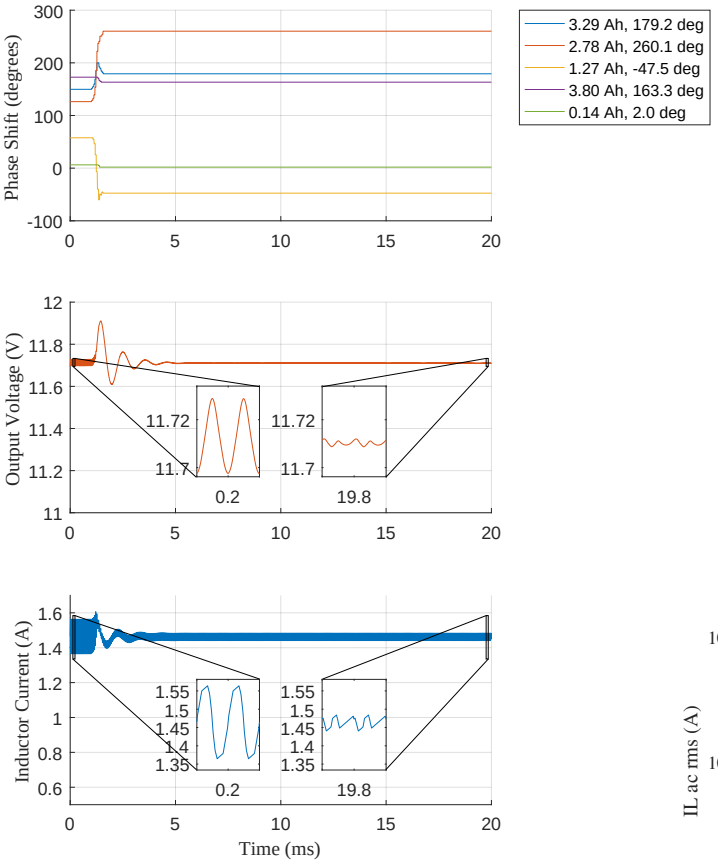


(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 44 mV to 5 mV. The ac rms current in the inductor is improved from 105 mA rms to 25 mA rms.

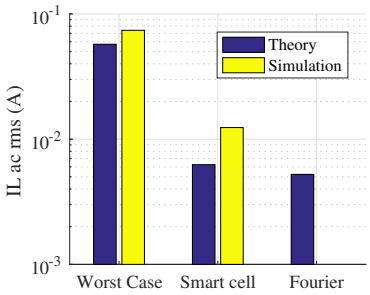


(b) A comparison of $I_{Lac\text{-}rms}$ values of a three smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.6: Discrete time simulation results of a three smart cell system.



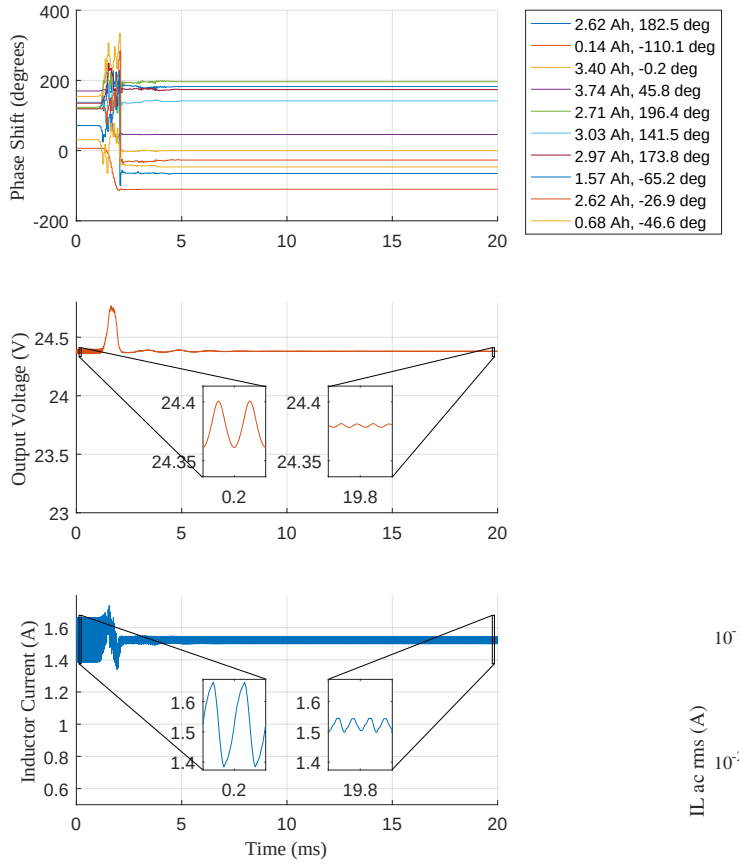
(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 5 mV to 2 mV. The ac rms current in the inductor is improved from 74 mA rms to 12 mA rms.



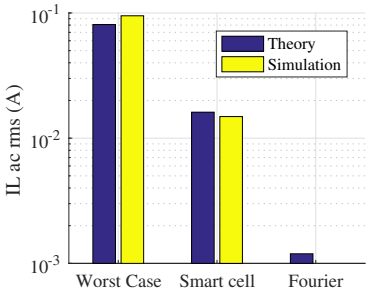
(b) A comparison of $I_{Lac\text{-}rms}$ values of a five smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.7: Discrete time simulation results of a five smart cell system.

10 smart cells



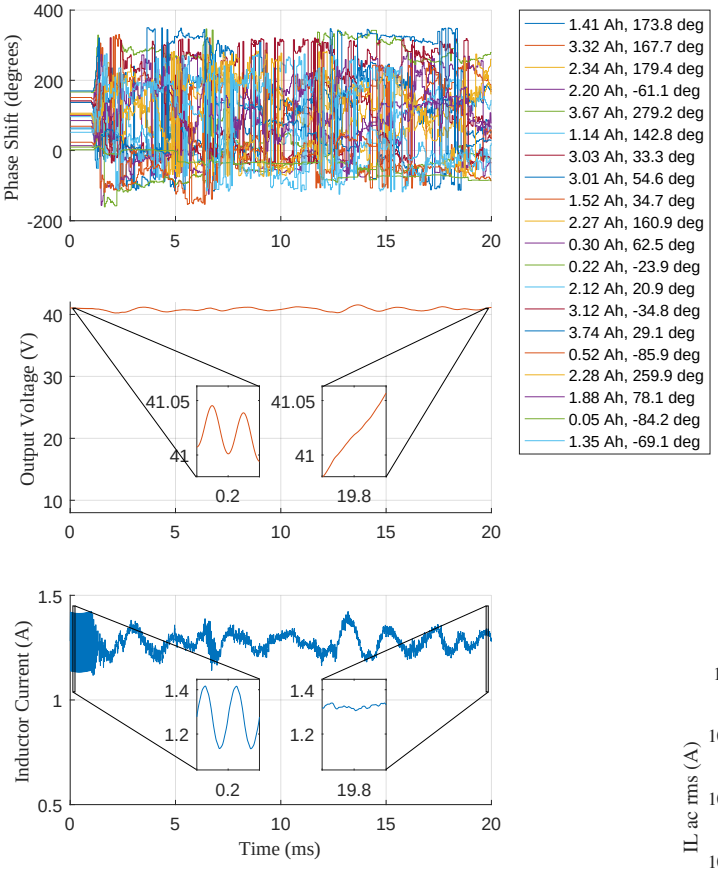
(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 7 mV to 2 mV. The ac rms current in the inductor is improved from 95 mA rms to 15 mA rms.



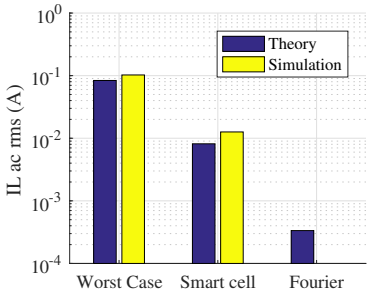
(b) A comparison of $I_{Lac\text{-}rms}$ values of a ten smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.8: Discrete time simulation results of a ten smart cell system.

20 smart cells



(a) Time evolution of the system. The smart cell controllers are turned on at 1.0 ms. The peak-to-peak ripple voltage on the capacitor is improved from 3 mV to 1 mV. The ac rms current in the inductor is improved from 103 mA rms to 13 mA rms.



(b) A comparison of $I_{Lac\text{-}rms}$ values of a twenty smart cell pack in the worst case switching pattern and the smart cell switching pattern. The theoretical minimum $I_{Lac\text{-}rms}$ is also calculated, and labelled "Fourier".

Fig. 5.9: Discrete time simulation results of a twenty smart cell system.

Summary and discussion

In the discrete time simulations of Fig. 5.6, Fig. 5.7, Fig. 5.8, and Fig. 5.9, each smart cell operated completely independently of one another. The phase controller was turned on 1.0 ms into the simulation. A value of $C_{MAX} = 4.00$ Ah was pre-programmed into each smart cell, in order for each smart cell to calculate its local duty cycle according to (4.1). Table 5.4 summarizes the improvements to the peak-to-peak output voltage ripple and ac rms ripple current in the inductor made when the smart cell phase controller was enabled. These improvements can also be seen in the inset graphs from each simulation result.

Table 5.4: Summary of performance improvements using the smart cell phase controller in discrete time simulations.

Number of Cells	**Worst Case**		**Smart Cell Control**	
	$V_{out\text{-}pp}$	$I_{Lac\text{-}rms}$	$V_{out\text{-}pp}$	$I_{Lac\text{-}rms}$
3	44 mV	105 mA rms	5 mV	25 mA rms
5	5 mV	74 mA rms	2 mV	12 mA rms
10	7 mV	95 mA rms	2 mV	15 mA rms
20	3 mV	103 mA rms	1 mV[1]	13 mA rms[2]

The smart cell controller was implemented as a MATLAB function block in Simulink. This block has multiple inputs and outputs that were used to configure the smart cell controller. Details of the smart cell Simulink model can be found in Appendix B.

The discrete time smart cell controller developed for these discrete time simulations was implemented in hardware using MATLAB's coder toolbox. Using this tool, the MATLAB code was directly converted to C++ code, which could be compiled in the smart cell hardware. This yielded to large advantages during the development process: 1) the smart cell controller could be debugged in simulation and 2) potential errors from importing the code from MATLAB to C++ manually were eliminated.

[1]Phase controller stability not achieved.
[2]See footnote 1.

As compared to the continuous time smart cell simulations, the discrete time simulations performed similarly in terms of the ripple reduction and were able to reduce the inductor's ripple current by about a factor of 10 in all cases. The one difference was in the 20 cell case. In the discrete time simulation, stability was not achieved. This is because the limited sampling frequency could not decipher all of the information necessary at all times. The following subsection discusses this in more detail.

5.1.4 Stability of the phase controller with limited sampling rate

As Sections 5.1.2 and 5.1.3 showed, the ability of the phase controller to find a stable operating point depends heavily on the sampling rate of v_L, or more accurately, the number of samples of v_L during each smart cell switching period. Define this as N_{sample}:

$$N_{\text{sample}} = \frac{f_{\text{sample}}}{f_s} \tag{5.1}$$

In this subsection, an upper bound on the number of smart cells that can be put in a series string given a system's N_{sample} will be calculated. In order to calculate this upper bound, the processing of the v_L waveform must be better understood.

Fig. 5.10 shows a schematic representation of the ADC sampling the v_L waveform during a transient event (when a smart cell is switching). Using this figure as a guide, the process by which the smart cell algorithm finds levels and edges in the v_l waveform is described as follows:

1. A large dv_L/dt event is detected between samples 4 and 5.

2. The two samples preceding this event are used to calculated the value of the level prior to the switching event. Thus, samples 2 and 3 are averaged to become the "front" level calculation.

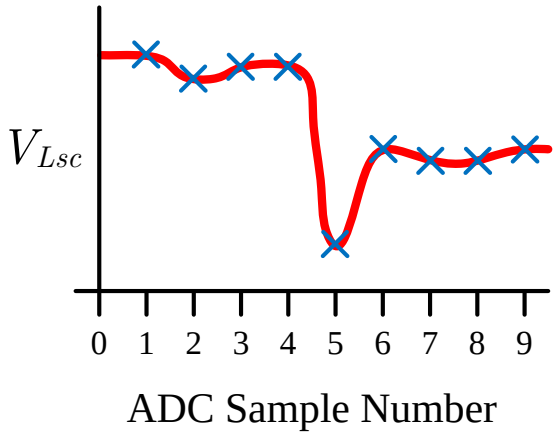


Fig. 5.10: Schematic example of sampling the v_L waveform.

3. Another large dv_L/dt event is detected between samples 5 and 6. However, since this event came right after the first one, it is ignored.

4. The two samples following the initial switching event and its glitches are used to calculate the value of the level. Thus, samples 7 and 8 are averaged to become the "back" level calculation.

The number of samples used to calculate the levels (2 in the above example), and the glitch threshold (1 in the above example) can be configured in software. See Appendix B for more details. However, a minimum of 6 samples are required around each switching event in order to properly sense the switching event *and* the levels around it. In Fig. 5.10, 7 samples were used due to the glitch measured in the v_L waveform.

In an ideal scenario using the same smart cell controller settings of the simulations of Section 5.1.3, where each switching event is captured with two samples, and the switching events are evenly spaced so that there are 2 samples between each switching event (thus the "front" and "back" level measurements will be identical), 4 samples are required for every switching event. Therefore, keeping in mind that there are two

switching events for every smart cell, the theoretical maximum number of smart cells that can be sensed in a series string is:

$$\frac{N_{\text{sample}}}{2 \times 4} = \frac{140}{2 \times 4} = 17.5. \tag{5.2}$$

Equation 5.2 represents the absolute upper bound on the number of smart cells in a series string given the controller and hardware settings and is the reason why the discrete time simulation of 20 smart cells in Fig. 5.9 was unable to find a stable operating point. However, 5.2 does not take into account:

- **Glitches:** Measuring and removing glitches will effectively reduce the number of cells in a string that can be measured.
- **SOC control:** During operation, the duty cycles of the smart cells may vary in order to synchronize their SOCs. In the above idealized example, any change in duty cycle of a single smart cell will perturb the perfectly spaced switching events and, thus, not all levels will be able to be accurately measured.

A more generalized expression for the maximum number of smart cells in a series string can be derived:

$$N_{sc\text{-}\max} = \frac{N_{\text{sample}}}{N_{\text{level}} + N_{sw\text{-}avg}} \tag{5.3}$$

where:

$$N_{\text{level}} = \text{Number of samples required per level,} \tag{5.4}$$

$$N_{sw\text{-}avg} = \text{Average number of samples per switching event.} \tag{5.5}$$

Equation (5.3) limits the control scalability of a smart cell system.

5.2 Experimental Results

5.2.1 Hardware Set-up

The theory developed in this work was tested in the laboratory with an experimental set-up consisting of three smart cells in series, as shown in Fig. 4.1 using the parameters listed in Table 5.1. The hardware was built around ARM's *mbed* platform, where each smart cell was implemented with the NUCLEO-F401RE board and a custom printed circuit board (PCB) containing the power stage. The inputs of each smart cell PCB was connected to a small pack of parallel connected 18650 lithium-ion cells, in order to simulate battery cells of varying capacities. Table 5.5 lists the capacities of the equivalent cell connected to each smart cell, as measured by a Neware battery tester 8 channel 5V20A-NTFA. The cells used were manufactured by Samsung, model number INR18650-29E [111]. The outputs of the smart cells were connected in series, and attached to a 4.8 Ω resistive load. Fig. 5.11 shows a photograph of the three smart cells built in the laboratory.

Table 5.5: Cell capacities used to test three smart cell PCBs in the laboratory.

Cell	Number of 18650 Cells	Measured Capacity
1	3	7.97 Ah
2	3	8.10 Ah
3	2	5.31 Ah

The NUCLEO-F401RE board was chosen for its relatively powerful micro-controller, the STM32F401RET6, in order to focus attention on how the smart cell controller could be implemented in hardware. The STM32F401RET6 is based on the ARM 32-bit Cortex-M4 CPU and has a floating point unit. The analogue to digital converter of the STM32F401RET6 was configured to its highest sample rate of 2.8 MHz while

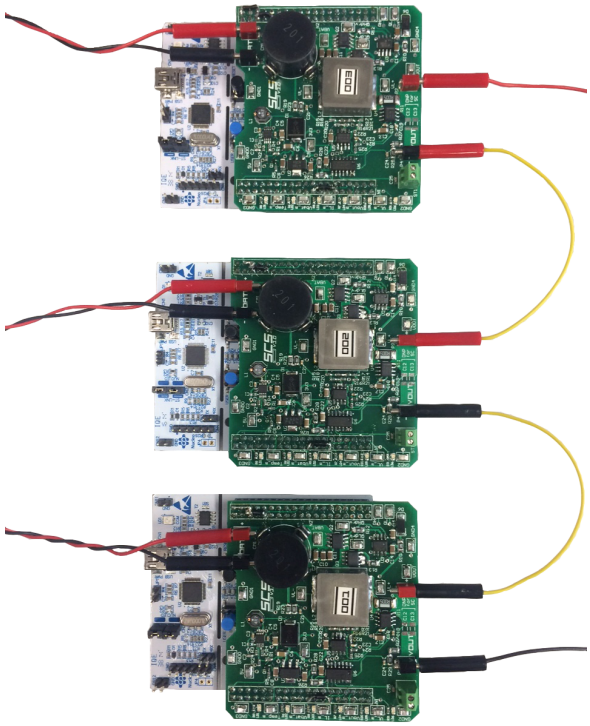


Fig. 5.11: A photograph of the three smart cell system operating in the laboratory. The battery cell connections are on the left and the output is on the right. The smart cells were connected to a variety of cells.

maintaining 12 bit sampling resolution, to capture the details of the v_L waveform. The sampling rate and resolution of the ADC determine the accuracy of the phase controller and SOC controller, respectively. The ADC used in these experiments was able to detect changes in phase of 2.6 degrees and 3.6 mV change in terminal voltages. Using the same ADC, tighter phase regulation could be achieved by decreasing the switching frequency.

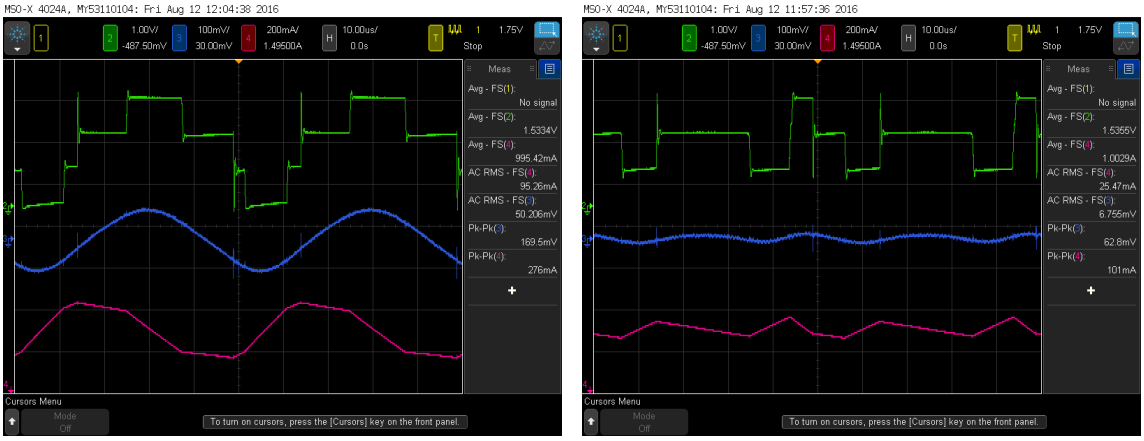
5.2.2 Phase Controller Performance

A first experiment using the pre-programmed capacities of Fig. 5.2(a) was carried out to verify the performance of the phase controller, whose role is to reduce the ac-rms current through the series string of smart cells.

Fig. 5.12(b) shows an oscilloscope screen shot of the three smart cells operating and finding their optimal switching pattern. The peak-to-peak voltage ripple from the experiments was reduced to 23 mV from 145 mV and the ac-rms L_{sc} ripple current was reduced to 25 mA rms from 95 mA rms. The worst case switching pattern is shown in Fig. 5.12(a), where the difference in ripple voltage and current is clearly visible. Note that the peak to peak values calculated by the oscilloscope (shown in Fig. 5.12) includes some switching noise, which was ignored for the peak to peak output voltage measurements.

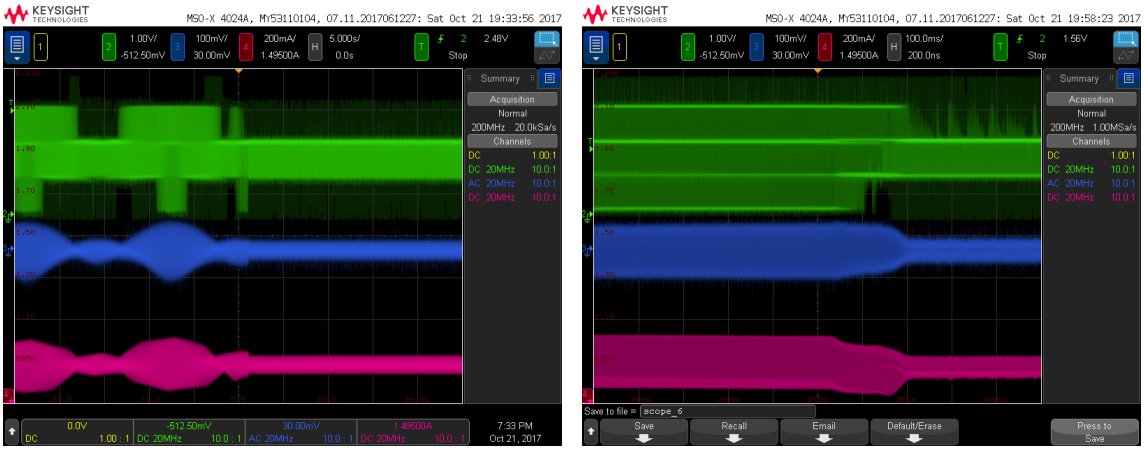
Fig. 5.13 shows the transient behaviour of the phase controller. Fig. 5.13(a) shows how the ripple current in the inductor and output ripple voltage vary slowly over time due to the small discrepancies in the switching frequencies of the smart cell hardware. This is because each smart cell generated its own clock and there *was not* a global timing signal, or any signal, running to every cell. In this figure, the phase controllers were turned on at about 1 s and they were able to overcome the discrepancies in switching frequencies by continually phase shifting themselves so that they all remained in their optimal phase position within the string. As shown in the latter half of the oscilloscope screen shot of Fig. 5.13(a), the smart cells maintained their stable switching pattern until the end of the capture and beyond. The stability analysis of Section 4.5 assumed all of the switching frequencies of each smart cell were identical (Equation (4.23)) which was a reasonable assumption for small discrepancies that are found in real systems such as the experimental set-up used in this chapter as shown by Fig. 5.13(a).

Fig. 5.13(b) shows the point at which the phase controller is turned on at a higher time resolution. The phase controller was turned on at about 40 ms and it took about 150 ms to reach a steady state value. The transition to the steady state value is executed in a smooth manner, with a gradual reduction in output voltage ripple.



(a) Worst case switching. (b) Controller active.

Fig. 5.12: Oscilloscope screen shots of the phase controller on and off. Averaging applied with 8 samples. Channel 2, top green trace, is the voltage across L_{sc} of the first smart cell with a capacity of C_1. Channel 2, middle blue trace, is the output voltage ripple. Channel 3, bottom pink trace, is the current in the smart cell inductors. Time scale: 10 µs per division.



(a) Phase controller turned on at about 1 s. Time scale: 5 s per division.

(b) Phase controller turned on at about 40 ms. Time scale: 100 ms per division.

Fig. 5.13: Oscilloscope screen shots of the transient behaviour of the phase controller. Channel 2, top green trace, is the voltage across L_{sc} of the first smart cell with a capacity of C_1. Channel 2, middle blue trace, is the output voltage ripple. Channel 3, bottom pink trace, is the current in the smart cell inductors.

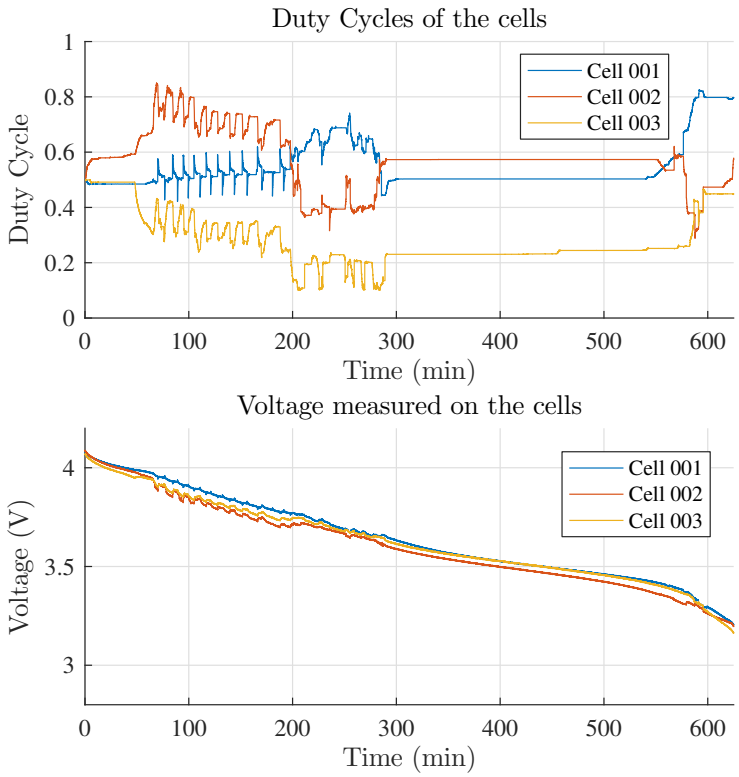


Fig. 5.14: The evolution of the duty cycles and cell voltages during the SOC controller test. "Steps" in the duty cycle are generated by the SOC controller when an average string voltage measurement cannot be obtained.

5.2.3 SOC Controller Performance

A second experiment to verify the performance of the SOC controller was also conducted. Each smart cell was connected to a fully charged set of cells, as listed in Table 5.5. Each smart cell began operation with a duty cycle of 0.5. It became the role of the SOC Controller to correct the mismatch in duty cycles to ensure all three smart cells discharged in proportion to their capacity.

During operation, the SOC controller estimated the average string voltage by calculating the difference in levels as described in Section 4.6. Fig. 5.14 shows how the cell voltages and duty cycles evolved over time during the experiment.

As shown in Fig. 5.14, the duty cycles vary quite a bit during operation. This is due to the operation of the SOC controller, attempting to yield accurate voltage

information from the string of switching smart cells. Since the controller relies on measuring the difference between levels to measure the average string voltage, there are moments during operation where these levels are non-existent. For example, when all of the duty cycles sum to a positive integer. Therefore, to counteract this possibility, if a cell senses that it has not been able to measure the string voltage for more than 2.5 minutes, it increases or decreases its duty cycle by a fixed amount. This will introduce levels into the voltage measured across L_{sc} and the cells will be able to measure the average string waveform. This is exactly what is happening from about 75 minutes to 200 minutes in the experimental results of Fig. 5.14. Cell 001 was modifying its duty cycle to get a better string measurement.

Due to the limited sampling resolution of the analogue to digital converter, each cell implements a ±10 mV dead zone [112] around its reference voltage.

At the end of the experiment, the cells were allowed to rest for 10 minutes and their voltages were measured. The results are shown in Table 5.6 and they are all within 50 mV of each other. This was a very good result considering there was no communication between any of the smart cells. Furthermore, if the SOC controller had not been operating, the string imbalance would have been much greater as shown in Fig. 5.15, where the smallest capacity cell discharges in around 450 minutes, clearly limiting the pack performance compared to the SOC controlled case.

Table 5.6: Cell voltages at the end of the SOC controller experiment after 10 minutes of rest.

Cell	**Voltage (V)**
1	3.162
2	3.140
3	3.113

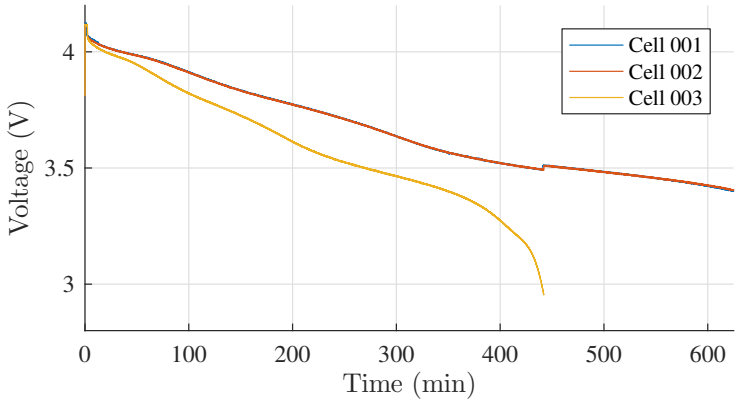


Fig. 5.15: The evolution of the cell voltages when the SOC controller is disabled, and a constant duty cycle of 0.5 is used by all cells.

5.3 Challenges

Accurate phase and SOC control is only possible through an accurate measurement of the v_L waveform. However, this waveform can be perturbed by parasitic capacitances from every smart cell to ground.

Fig. 5.16 shows the switching actions of two smart cells connected in series. In this case, there was a large parasitic capacitance from each cell to ground caused by the laboratory power supply that was used to emulate each electrochemical cell. The bottom trace of this figure shows the output of the v_L sensing circuit and two things are immediately striking: 1) the crisp "staircase" waveforms that were seen in the simulations are no longer present, and 2) the switching action of the second smart cell (measured by channel 1, yellow, top), is not captured by the inductor being measured by channel 2 (green, bottom).

This parasitic effect can be greatly reduced by introducing a common mode choke at the input of every smart cell. Fig. 5.17 shows three smart cells in series gating, each cell connected to a channel of a dSPACE Battery Emulator. Although the staircase nature of v_L has returned, it is not as crisp as the simulations. As a consequence, smart cells that use a common mode choke are able to implement the phase controller, but

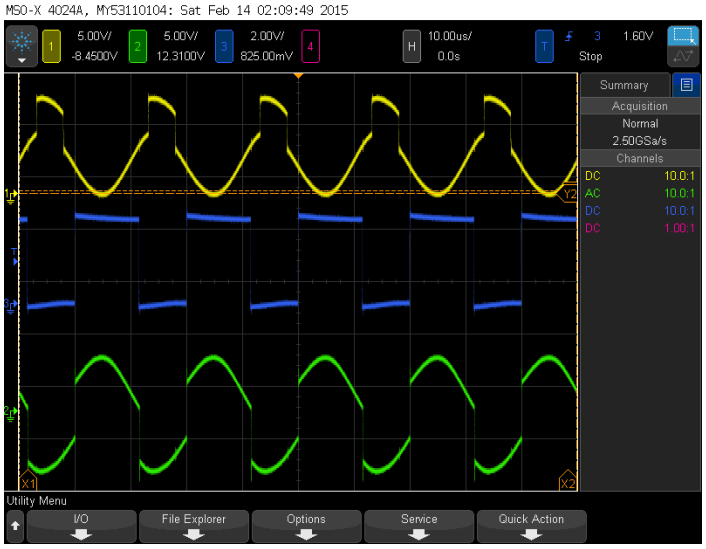


Fig. 5.16: Oscilloscope screen shot of two smart cells in series gating with a large parasitic ground capacitance between each smart cell and ground. Channel 1, yellow, top: gating signal of the upper smart cell. Channel 2, green, bottom: voltage across L_{sc} of the bottom smart cell, after the analogue sensing circuit. Channel 3, blue, middle: gating signal of the lower smart cell. All oscilloscope probes were referenced to ground. Time scale: 10 µs per division.

the SOC controller does not work because the voltage measurements at each switching action are not accurate enough.

In the experimental results of this chapter, each smart cell was connected to a small group of battery cells. The battery cells have very little parasitic capacitance to ground. Furthermore, only differential probes were used when taking measurements. The waveforms that were obtained from v_L in this configuration are shown in Fig. 5.18. As shown in the figure, the voltage across L_{sc} is even more crisp than Fig. 5.17. Despite this, the SOC controller measures the average of each level around every switching transition and uses those two averages to determine the cell voltage that just switched in and out of the circuit. Fig. 5.18 graphically shows how the SOC controller measures the voltage of a transition. In this experiment, each smart cell was connected to a small battery pack, and each cell's input was filtered through a common mode choke. The annotations in the figure describe how the string voltages are measured from v_L.

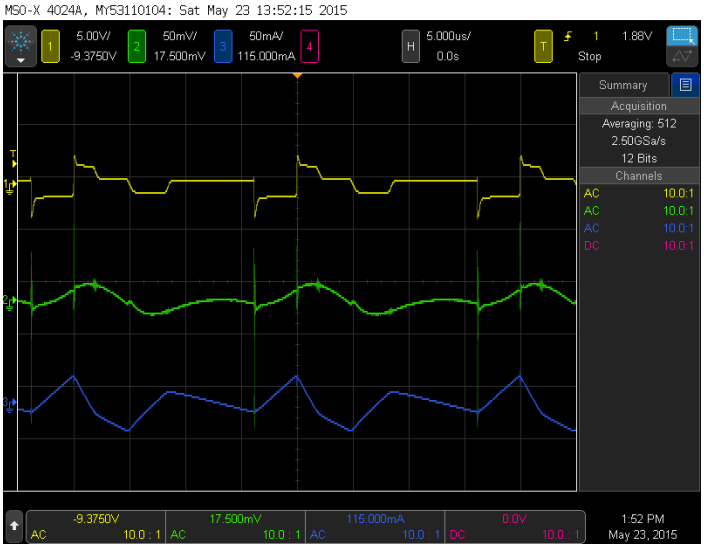


Fig. 5.17: An oscilloscope screen shot of the three smart cells in series gating with a large parasitic capacitance between each smart cell and ground, through each cell's voltage source. In this experiment, all three cells were connected to a dSPACE Battery Simulator, and each cell's input was filtered through a common mode choke. Channel 1, top yellow, is the voltage across L_{sc} of the first smart cell. Channel 2, middle green, is the output voltage ripple. Channel 3, bottom blue, is the current in the smart cell inductors. Time scale: 5 µs per division.

Fig. 5.18: An oscilloscope screen shot of the three smart cells in series gating with a small parasitic capacitance between each smart cell and ground. Channel 2, top green, is the voltage across L_{sc} of the first smart cell. Channel 3, middle blue, is the output voltage ripple. Channel 4, bottom pink, is the current in the smart cell inductors. Time scale: 10 µs per division.

Finally, the notion of parasitic capacitances has applications beyond smart cells. In higher frequency MMC converters (switching frequencies greater than line frequency) [113, 114], the issue of parasitic capacitances to ground could introduce losses that could be mitigated by a common mode choke between the energy storage source and switching network. To date, this has not been addressed, most likely because the switching frequencies are still low (350 Hz in [113], and 1 kHz in [114]), as compared with the smart cells (20 kHz).

5.4 Summary and discussion

The simulation results focused on the phase controller and showed how a digital system with a finite sampling frequency places an upper bound to the number of smart cells that can be theoretically in a series string.

The experimental results of this chapter showed that a completely decentralized load management system is possible, paving the way towards a completely decentralized battery management system. The experimental results of Fig. 5.14 worked well to synchronize the terminal voltages of the three smart cells. During the mid-point of the experiment, the duty cycles of the two larger cells, Cell 001 and Cell 002, were larger than Cell 003, as expected.

Despite the theoretical maximum of 17 smart cells with the current hardware set-up, the current hardware set-up was never operated with more than 4 cells. In particular, the SOC controller operated reliably with up to three cells. This was due to difficulties in measuring the average string voltage by analysing the v_L waveform. One large challenge with yielding good measurements of v_L was the parasitic ground capacitance between each cell and ground.

The magnitude of the difference between the levels of the v_L waveform is determined solely by the ratio of the voltage of the cell that is switching and the number of smart

cells in the string. Therefore, the magnitude of this signal will decrease at a rate inversely proportional to the number of cells in the string. In a practical system, this means that the v_L sensor could be built with a variable gain that is increased depending on the number of cells is senses. A detailed study of the how the signal to noise ratio of the voltage across v_L changes with an increasing number of smart cells would need to be carried out to determine the absolute maximum number of cells that is possible in a string with conventional hardware.

As the number of smart cells increases, the filtering requirements of L_{sc} also change. Adding a smart cell to a string has a two fold effect: 1) it increases the filtering inductance and 2) it increases the effective switching frequency. Therefore, in an ideal scenario the L_{sc} should be redesigned if the same ripple specifications are required for a different number of smart cells. This is not desirable, thus a proposed control method of "transitions per second" is presented as future work in Section 6.2.2. In the experimental results of this chapter, the smart cell hardware was implemented with large inductances for L_{sc}. In a practical system, L_{sc} can be as small as possible as long as it is still operating in its linear region.

Chapter 6

Conclusions

This thesis has a number of significant contributions to the fields of decentralised battery management and battery pack design. This chapter will summarize those contributions and conclude with areas of future work that can be explored.

6.1 Contributions

The main contributions of this thesis are grouped by the two projects presented: the intelligent battery pack and the smart cells, and summarized in the following subsections. The remainder of this section will discuss the scalability criteria created in this thesis and its application to both projects.

Balancing circuit scalability

Section 1.5 introduced a scalability criteria which normalised the performance of balancing circuits and evaluated them on their normalized kVA ratings and normalized passives energy ratings. Within each rating, there were clear "Types" of circuits shown in Fig. 1.5. The scalability Types for a number of balancing circuits presented in the literature were summarized in Table 1.2. Using this metric, the intelligent battery and

smart cell were evaluated with the same criteria, and they were found to be Type A and Type II circuits due to the inverse cubed relationship between peak to peak ripple voltage and number of cells.

Using this scalability criteria, circuits like the intelligent battery and the smart cells are viable options for large battery packs. This is a good result, because these circuits are more effective when used with many cells as there is more likely to be large variations between series connected cells as the number of cells increases.

6.1.1 Intelligent battery pack

Hot-swappable intelligent battery pack design

Chapter 2 introduced a design of a hot-swappable intelligent battery pack, a first of its kind.

A hot-swappable battery pack introduces the concept of battery pack maintenance. Instead of replacing an entire pack when it fails, individual modules can be replaced as the cells eventually fail. This type of system architecture could be useful to companies who have many battery packs spread across a wide area that need maintenance. Instead of equipping a maintenance team with a few new packs as part of their tool kit, they could be equipped with few packs worth of modules, that could be used to maintain several battery packs in the field, instead of just a few. As an example, hot-swappable battery packs could be used as back-up power sources for telecommunication towers, which can be spread over vast areas.

Low latency in digital control

One challenge that has always daunted distributed power electronics, is how to physically manage the electrical signals required for sensing and control. In the intelligent battery, most of the control was done at the module level. Each module was responsible for

managing its own phase shift and state of charge. This was done via the low bandwidth CAN bus and it was not time sensitive - the module could tolerate late and lost data and still accurately manage its phase shift and SOC. The master was responsible for current and voltage control at the output. In order to synchronize the switching events of all of the modules and to provide a low latency, low noise signal to control the output current and voltage, a single wire sync and control signal was developed, as shown in Fig. 2.11. This signal provided a $2 \times T_s$ latency in the current and voltage control loops and synchronizes all of the switching actions of the modules. In summary, the intelligent battery separated the real time signals from the "soft" time signals and distributed the control tasks to better manage all of the electrical signals within the pack.

The low latency of the current and voltage control loops meant that the intelligent battery is closer in similarity to a dc to dc converter than a battery pack. With this type of architecture, the intelligent battery can replace a normally two stage system of a standard battery pack and dc to dc converter with a single, combined stage of the intelligent battery pack. Future work involving this type of system is discussed in the next section.

6.1.2 Smart cells

Broadly speaking, smart cells start to address the practical issues of building intelligent battery packs: intelligent battery packs require a large amount of overhead to control and monitor the entire pack. Therefore, eliminating the need for intra-pack communication can simplify an intelligent pack's design and implementation, further bolstering the case for power electronics integrated into battery pack designs. Smart cells are also a unique approach to battery management: completely decentralised battery management.

Multi-purpose passives

One of the key innovations of smart cells was augmenting the role of the small filtering inductors on each cell to the role of a multi-purpose sensor. As shown in Fig. 4.2(b), by measuring the voltage across the filtering inductor, all of the switching actions in a series string of smart cells are captured. Furthermore, the average terminal voltage of the cells in the series string can also be extracted from analysing the inductor's voltage. These two new roles of the filtering inductor enable the smart cells to synchronize their switching actions and their terminal voltages without any inter-cell communication.

Decentralised phase control

One of the biggest challenges of a distributed power electronics architecture such as the intelligent battery and the smart cells, is synchronizing the switching actions of the power electronic devices. It is important to synchronize these actions in order to have a predictable and constant output voltage ripple. Without synchronized switching, the output voltage ripple could vary randomly between its best and worst values or in the best case, it could vary periodically as was shown in Section 5.2.2.

The decentralized phase controller was built around the theory of Kuramoto oscillators [102]. However, instead of synchronizing the switching actions to be in phase with each other, they were synchronized to a pattern which minimized (4.17). Minimizing (4.17) minimized the first harmonic voltage ripple in a series connection of smart cells.

Section 4.5 theoretically proved the stability of the phase controller around local minima by showing that the Hessian of (4.17) was positive semi-definite. This concluded the thorough theoretical analysis of the phase controller, proving that, in theory, the controller of (4.20) is a viable controller for decentralized phase control.

The phase controller was studied extensively in simulations, first in continuous time in Section 5.1.2, then in discrete time in Section 5.1.3. The continuous time study was conducted to confirm the theoretical analysis of Chapter 4. The discrete time study was conducted to evaluate the effects of using hardware with limited sampling rates and latency on the performance of a string of smart cells. In Section 5.1.4, a method to determine the maximum number of smart cells that is theoretically possible in a series string was derived in (5.3). All of these results confirmed that decentralized phase control is possible in practice.

Section 5.2.2 demonstrated the performance of the phase controller in practice with three smart cells operating together. The phase controllers performed very well to synchronize the switching actions of the three cells to a local minima of (4.17).

Decentralised SOC control

As a further step towards a completely decentralised BMS, a completely decentralised SOC controller was developed in theory and tested in the laboratory. The controller used voltage differences of the v_L waveform to synchronize the terminal voltages of all cells in a series string of smart cells. When the cells are of the same chemistry, this is equivalent to running the cells in parallel, as shown in Fig. 2.23.

The experimental results of Fig. 5.14 showed good SOC control for the three smart cell system that was tested, and clearly outperformed the case without SOC control shown in Fig. 5.15.

6.2 Future work

There are many exciting avenues of research and development that can be explored from the research presented in this thesis. The rest of this subsection will discuss future work that has come out of both projects. Following that, project specific future work

will be discussed. Future work on the intelligent battery focuses on how to exploit its features in new projects. For the smart cells, future work focuses on how to augment the foundation of the decentralized BMS presented here, to a fully-fledged BMS ready for a real world application.

Battery models and machine learning

The SOC controller of both the intelligent battery and the smart cells relied on synchronizing the terminal voltages of all of the series connected cells. The SOC controller from these projects can be further developed using battery models available in the literature. Furthermore, these models could be enhanced with machine learning principles, so that each module or smart cell learns how the cells it is connected to behave, in order to better predict its SOC and SOH.

Battery passport

A battery passport is the idea that every battery pack or cell contains a small microchip which keeps track of the pack's or cell's history. The idea of a battery passport is not new, but something that can be explored with the hardware developed in this thesis. Companies such as Dukosi [115] are developing chips that can be integrated with battery cells to track their performance over their lifetime. Both the intelligent battery and the smart cells could be used as platforms to further develop the battery passport idea and standards to make it a reality. Using these platforms, further research into the type and quantity of information that should be stored can be investigated. Recording a lot of data will yield a very accurate picture of a battery's history, but it will cost more to store this data. The research questions will revolve around how to minimize the quantity of data without comprimising on the accuracy of the battery's history and SOH. This has large ramifications in the second life market of lithium ion cells, a

market that is growing rapidly, because as cells leave their first application they can be easily grouped into appropriate second life applications using their battery passport.

Decentralised phase control, centralised BMS

A project that could further develop the battery management system presented in this thesis into a commercial product is one that takes advantage of the best aspects of the smarts cells and the intelligent battery pack. The project could use the decentralised phase controller from the smart cells in combination with a wireless centralised controller for pack level battery management. Both the intelligent battery hardware and smart cell hardware developed in this work can be used to develop this idea further.

The theory developed for the smart cells also has applicability in other areas such as super capacitors and solar photovoltaics. In both of these applications, series strings of devices need to be balanced and managed over time. A super capacitor application would be similar to the smart cell application presented here. However, for the solar photovoltaic application, further research on how the decentralised controller could be extended to include a maximum power point tracking algorithm is required.

Transitions per second control

Both projects had very low output voltage ripple and due to their topology, the voltage ripple would decrease as more modules were added. Therefore, an interesting research project would involve a new control method which varies the switching frequency inversely proportional to the number of modules or smart cells that are in the series string. This would be similar to controlling the number of transitions, as in module or smart cell switching events, per second.

Implementing this in the intelligent battery would be relatively straightforward since there is a master which synchronizes all of the module PWM modules. However,

as the number of modules increases, the frequency will decrease, and the control loop latency with also increase. Therefore, care should be taken to ensure the desired system performance is still met. At low switching frequencies, the sync and data signal could send two values of $\hat{d}$ during every switching period to reduce the control latency.

The implementation of the transitions per second control on the smart cells will be a greater research challenge. There will need to be a method or controller that can gaurantee that all of the smart cells will end up at the same frequency. The theoretical analysis of this system will also be very challenging, and would involve Kuramoto analysis where each agent, or smart cell, does *not* have the same switching frequency.

6.2.1 Intelligent battery pack

Lifetime enhancement

The intelligent battery adjusts the energy flow through every series connected module to ensure that each module discharges proportional to capacity. This will have a positive impact on ageing, as weaker cells will be loaded less than healthier cells [109, 110]. Therefore, an obvious research question to solve is to verify this hypothesis in a real system. The research should be carried out under different prototypical cycling profiles to determine which applications this technology is best suited for. Using the two intelligent battery packs built for this thesis, such an experiment would be straightforward to conduct. One of the packs could run in a "standard" mode, where the duty cycle of each module is the same, and the other pack could run in "intelligent" mode. Using the two identical packs with different control algorithms will also remove the effects of the extra power electronics in the study, thus the results will be purely an indication of the improvements in battery pack life that can be obtained with module level management.

Intelligent battery as part of an integrated system

As mentioned in Section 6.1.1, the intelligent battery is more closely related to a dc to dc converter than a standard battery pack. An intelligent battery is "more than just a pack". Therefore, future research should investigate new applications where a battery pack and dc to dc converter can be replaced with a single intelligent battery. In addition to a system study, a cost benefit analysis taking into account the increased lifetime of the battery pack would also need to be undertaken.

One such application could be in solar home systems. Typically a charge controller is required to extract the maximum power out of a solar array. An intelligent battery pack could easily integrate the functions of a maximum power point tracker into its master controller and could operate as a solar charger.

6.2.2 Smart Cells

Analysis of the v_L waveform

The largest computational burden on the smart cell controller is the analysis of the voltage across L_{sc}. The algorithm that was used is one that is based on traditional `if`$\{\cdots\}$`else`$\{\cdots\}$ logic. As the number of cells or sample points increase, the execution time of the algorithm also increases linearly. However, analysing the voltage across L_{sc} is similar to analysing photographs. Through machine learning, computers are able to identify individuals and objects in photographs. Further research should be undertaken to determine how machine learning techniques could be applied to the voltage across L_{sc} to extract the average SOC of the string and the switching events, or more directly, the control signals. This research would be very interesting in contrast to the traditional machine vision applications since the data is quite sparse in comparison to a photograph. Instead of inputting a matrix of red, green, and blue values, the

inputs would simply be a vector of voltages. This also implies that the computational power required to compute such an algorithm should be reduced, which is ideal for low power applications such as the smart cell.

Ripple reduction

The phase controller of (4.20) used only the fundamental harmonic to minimize the output voltage ripple. However, in some applications this may not be enough. Therefore, extending the algorithm to higher order harmonics should be considered. A short investigation was done into this early on in the smart cell work, however a simple controller like the one of (4.20) was not stable in simulation.

Computational smart cell algorithm improvement

The smart cell algorithm implemented for the thesis was optimised for debugging purposes only. Therefore, further development into improving its execution time would improve the performance and power requirements of the smart cell algorithm. Since the controller uses the Fourier transform, the same techniques which reduce the discrete Fourier transform algorithm from an order n^2 problem to an order $n \log n$ problem could be applied here.

Measurement of the v_L waveform

Another method to improve the analysis of the v_L waveform is to further develop its measurement hardware. In the current realization, an ADC is used to sample v_L for an entire switching cycle, and the conversion results are analysed later to extract the level and switch timing information. Some of this analysis could be done in hardware. As a first iteration, an FPGA could be programmed to detect the switch timing events.

Fig. 6.1: Artistic impression of the future of smart cell technology.

The hardware would be able to synchronize the conversion of the level information. Together, this would greatly simplify the analysis of v_L.

Hardware

The vision of a smart cell has always been to miniaturize the electronics to a point where is can be integrated onto the electrochemical cell itself. Fig. 6.1 is an artistic impression of what future developments into the smart cell could realize. The rendering depicts an 18650 cell wrapped in a package which includes a small PCB. The PCB would house the MCU and power electronics necessary to implement the smart cell algorithms. There are many cells on the market today which have built-in current interrupt devices which are implemented as a small PCB integrated into the cell's packaging in a similar manner to Fig. 6.1. Therefore, the future of these interrupt devices could also implement the smart cell algorithms.

6.3 Final thoughts

Until humanity develops energy storage devices that do not degrade or can become a safety hazard, there will always be a need for high performing BMS's. This thesis has shown that the tight integration of power electronics can yield improved performance out of series connected battery cells, in one case increasing the energy storage capability of a pack by 46%. It has also introduced a new way of thinking about battery packs: as devices that can be repaired or refurbished, not just replaced. It takes 454 Wh of

energy to produce 1 Wh of Lithium-ion battery storage [116], therefore we should use each cell until it is truly exhausted before it is sent for recycling.

Publications

[I] Damien F. Frost and David A. Howey, Completely decentralised active balancing battery management system, in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 729-738, January 2018. Publisher copy.

[II] Damien F. Frost and David A. Howey, High-Speed Peltier Calorimeter for the Calibration of High-Bandwidth Power Measurement Equipment, in *IEEE Transactions on Instrumentation and Measurement*, vol. 65, no. 1, pp. 155-163, January 2016[1]. Publisher copy.

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[1]During the first year of my DPhil, I designed, built, and programmed a calorimeter for one of my project sponsors, Newtons 4th Limited (N4L). This work is not related to the decentralised BMS work presented in the main body of this thesis.

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Appendix A

Lower Bound on $I_{Lac-rms}$

A lower bound on $I_{Lac-rms}$ will now be derived. This will give an indication of how well a system of smart cells will perform when their phase angles are optimized by minimizing the total sum vector of (4.14), instead of minimizing the infinite harmonic sum of (4.11). Throughout this analysis, the duty cycles of all of the cells are assumed to be less than 1.0 and greater than 0.0.

A.1 Base Cases

The analysis will start by considering some base cases of smart cell systems. It is most interesting to start with a system with at least two smart cells. For this analysis, the duty cycles of each smart cell within each system are considered to be unique, unless otherwise stated.

A.1.1 Two smart cells

In the case of two smart cells, there will be two switching cells. Intuitively, we expect that the optimal switching pattern will evenly space any "on" or "off" times. Setting $M = 2$, equation (4.11) reduces to:

$$I_{Lac-rms}^2 = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} \frac{4}{\pi^2 n^4} \left[\sin^2(\pi n D_1) + \sin^2(\pi n D_2) + 2\sin(\pi n D_1)\sin(\pi n D_2)\cos(\pi n(D_1 - D_2) + n(\theta_1 - \theta_2))\right]. \quad \text{(A.1)}$$

Equation (A.1) can be minimized by minimizing the last term. This means that the cosine term in (A.1) should be set to -1. Since only the relative phase shift between cell 1 and cell 2 is of concern, θ_2 can be set to 0. Now a solution for θ_1 can be found:

$$\cos(\pi n(D_1 - D_2) + n(\theta_1 - 0)) = -1 \quad \text{(A.2)}$$

$$\pi n(D_1 - D_2) + n\theta_1 = (2k+1)\pi \quad \text{(A.3)}$$

$$\theta_1 = \frac{\pi}{n}(2k+1) - \pi(D_1 - D_2), \quad \text{(A.4)}$$

where $k \in \mathbb{Z}$. Since there can only be one solution for θ_1, consider the case where $n = 1$:

$$\theta_1 = \pi(2k+1) - \pi(D_1 - D_2). \quad \text{(A.5)}$$

The solution for θ_1 as defined by (A.5) is consistent with our intuition, for every value of k. To prove that this value of θ_1 is the minimum of (A.1), substitute (A.5), into the first and second derivatives of (A.1). For the first derivative:

$$\frac{d\left(I_{Lac-rms}^2\right)}{d\theta_1} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} \frac{4}{\pi^2 n^4} \left[2n\sin(\pi n D_1)\sin(\pi n D_2) \cdot \sin(\pi n(D_1 - D_2) + n(\theta_1 - \theta_2))\right]. \quad \text{(A.6)}$$

Substitute (A.5) into (A.6) and set $\theta_2 = 0$:

$$\left.\frac{d\left(I_{Lac-rms}^2\right)}{d\theta_1}\right|_{\theta_1=\pi(2k+1)-\pi(D_1-D_2)} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} \frac{4}{\pi^2 n^4}\left[2n\sin\left(\pi n D_1\right)\cdot \sin\left(\pi n D_2\right)\sin\left(\pi n\left(2k+1\right)\right)\right] = 0. \quad \text{(A.7)}$$

Equation (A.7) shows that (A.5) is a local minimum or maximum of (4.11) because the last term, $\sin\left(\pi n\left(2k+1\right)\right)$, is zero for all values of n and k. Now calculate the second derivative of (4.11):

$$\frac{d^2\left(I_{Lac-rms}^2\right)}{d\theta_1^2} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} -\frac{4}{\pi^2 n^4}\left[2n^2\sin\left(\pi n D_1\right)\sin\left(\pi n D_2\right)\cdot \cos\left(\pi n\left(D_1-D_2\right)+n\left(\theta_1-\theta_2\right)\right)\right]. \quad \text{(A.8)}$$

Substitute (A.5) into (A.8) and set $\theta_2 = 0$:

$$\left.\frac{d^2\left(I_{Lac-rms}^2\right)}{d\theta_1^2}\right|_{\theta_1=\pi(2k+1)-\pi(D_1-D_2)} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} -\frac{4}{\pi^2 n^4}\left[2n^2\sin\left(\pi n D_1\right)\cdot \sin\left(\pi n D_2\right)\cos\left(\pi n\left(2k+1\right)\right)\right] \quad \text{(A.9)}$$

$$\left.\frac{d^2\left(I_{Lac-rms}^2\right)}{d\theta_2^2}\right|_{\theta_1=\pi(2k+1)-\pi(D_1-D_2)} = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty} -\frac{4}{\pi^2 n^4}\left[2n^2\sin\left(\pi n D_1\right)\cdot \sin\left(\pi n D_2\right)\left(-1\right)^n\right]. \quad \text{(A.10)}$$

The sign of (A.10) will determine if θ_1 describes a local maxima or minima. The terms $\sin(\pi n D_1)$ and $\sin(\pi n D_2)$ will both be greater than zero since D_1 and D_2 are within $(0, 1)$. Everything else in the expression is constant, therefore, we need only to determine the sign of the infinite sum:

$$\sum_{n=1}^{\infty} -\frac{(-1)^n}{n^2} = \frac{\pi^2}{12}, \tag{A.11}$$

which is positive. Therefore, minimizing (4.14) or (4.11) will yield the same result of in the two cell case because θ_1 was determined using only the first harmonic of $I_{Lac-rms}$, and has also been shown to be a local minimum of $I_{Lac-rms}$.

A.2 Three or more smart cells

In the general case of three or more smart cells, it is very difficult if not impossible, to come up with an analytical solution. Therefore, a lower bound on (4.11) is desired when it is minimized using only the fundamental harmonic, by minimizing (4.14). The analysis will start with (4.11), which is repeated here for convenience:

$$I_{Lac-rms}^2 = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \sum_{n=1}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4}\cdot \left[\sin(\pi n D_i)\ \sin(\pi n D_j)\cos\left(\pi n\left(D_i - D_j\right) + n\left(\theta_i - \theta_j\right)\right)\right]. \tag{A.12}$$

When (A.12) is minimized with (4.14), only the fundamental harmonic is considered. Therefore, separate the fundamental harmonic from A.12.

$$I_{Lac-rms}^2 = \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2 \left[\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2}\left[\sin(\pi D_i)\sin(\pi D_j)\cos\left(\pi\left(D_i - D_j\right) + \left(\theta_i - \theta_j\right)\right)\right]\right.$$

$$+\sum_{n=2}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4}\left[\sin\left(\pi n D_i\right)\sin\left(\pi n D_j\right)\cos\left(\pi n\left(D_i-D_j\right)+n\left(\theta_i-\theta_j\right)\right)\right]\Bigg] \quad \text{(A.13)}$$

$$I^2_{Lac-rms}=\frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2\Bigg[\frac{4}{\pi^2}\left|v'_{\Sigma}\right|^2 + \sum_{n=2}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4}\left[\sin\left(\pi n D_i\right)\sin\left(\pi n D_j\right)\cos\left(\pi n\left(D_i-D_j\right)+n\left(\theta_i-\theta_j\right)\right)\right]\Bigg] \quad \text{(A.14)}$$

A lower bound for $I^2_{Lac-rms}$ can be found by assuming the transcendental functions of (A.14) equal -1:

$$I^2_{Lac-rms} \geq \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2\left[\frac{4}{\pi^2}\left|v'_{\Sigma}\right|^2+\sum_{n=2}^{\infty}\sum_{i=1}^{M}\sum_{j=1}^{M}\frac{4}{\pi^2 n^4}\left[-1\right]\right] \quad \text{(A.15)}$$

$$I^2_{Lac-rms} \geq \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2\left[\frac{4}{\pi^2}\left|v'_{\Sigma}\right|^2+\sum_{n=2}^{\infty}\frac{4M^2}{\pi^2 n^4}\left[-1\right]\right] \quad \text{(A.16)}$$

$$I^2_{Lac-rms} \geq \frac{1}{2}\left(\frac{V_{nom}T_s}{2\pi L}\right)^2\left[\frac{4}{\pi^2}\left|v'_{\Sigma}\right|^2-\frac{4M^2}{\pi^2}\left(\frac{\pi^4}{90}-1\right)\right] \quad \text{(A.17)}$$

$$I^2_{Lac-rms} \geq \frac{1}{2}\left(\frac{V_{nom}T_s}{\pi^2 L}\right)^2\left[\left|v'_{\Sigma}\right|^2-M^2\left(\frac{\pi^4}{90}-1\right)\right] \quad \text{(A.18)}$$

Equation (A.18) is a lower bound for $I^2_{Lac-rms}$, which can be easily computable. However, this lower bound is very conservative, and $M^2\left(\pi^4/90-1\right)$ can be larger than $\left|v'_{\Sigma}\right|^2$.

A.2.1 Three or more smart cells, tighter bounds

The lower bound of (4.11) calculated in (A.18) is too conservative to be of use in many situations, thus a tighter bound in derived in this subsection using a combination of intuition and maths. This will be done by building an equivalent pack of smart cells of

which we can easily calculate a minimum value of $I^2_{Lac-rms}$ without the need of Fourier Series.

First, construct an equivalent pack of M smart cells by setting all of their duty cycles to be the same, such that the duty cycle of every smart cell in the new pack is D_{eq}, where:

$$MD_{eq} = \sum_{i=1}^{M} D_i. \tag{A.19}$$

Intuitively, an M cell pack of smart cells with the same duty cycle will have a minimum value of $I^2_{Lac-rms}$ when the phase shifts of the smart cells are distributed evenly over the switching period, namely:

$$\theta_i = \frac{2\pi}{M} i,\ i \in [1, M]\,. \tag{A.20}$$

In this situation, using the small ripple approximation technique, the inductor current waveform will be a periodic triangle wave with a period of T_s/M as shown in Fig. A.1. Therefore, $I^2_{Lac-rms}$ can be easily calculated by calculating the ac-rms value of this triangular wave. In [117], the ac-rms value of an arbitrary triangular waveform with peaks at $\pm I_p$ is derived, and it is: $I_{Lac-rms} = I_p/\sqrt{3}$. Therefore, using the quantities in Fig. A.1, the $I_{Lac-rms}$ of the equivalent system of smart cells is (note that it is *not* squared):

$$I_{Lac-rms} = \left(\frac{(\lceil MD_{eq} \rceil - MD_{eq})\, V_n}{ML_{sc}}\right)\left(\frac{(MD_{eq} - \lfloor MD_{eq} \rfloor)\, T_s}{2M}\right)\left(\frac{1}{\sqrt{3}}\right) \tag{A.21}$$

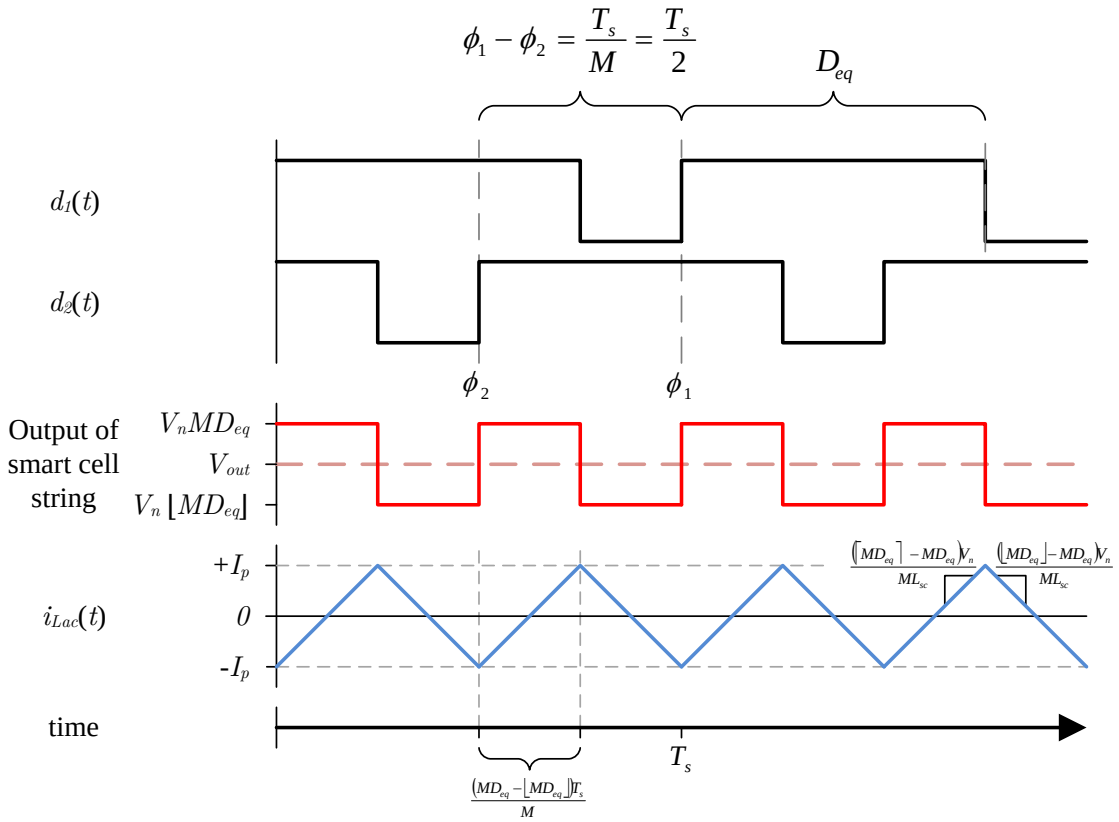

Fig. A.1: An example of a an equivalent smart cell pack composed of two cells, each with a duty cycle of D_{eq}. The $I_{Lac-rms}$ can be easily calculated for this pack, since the ac current through the smart cell inductors is a periodic triangle wave, with a period of T_s/M, and for the 2 cell case depicted here, $T_s/2$.

Appendix B

Smart cell code

This appendix describes all of the inputs to the smart cell controller function that was used in the discrete time simulation results of Section 5.1.3, and in the experimental hardware via MATLAB's coder toolbox.

B.1 Simulink block diagram

Fig. B.1 shows the top level Simulink block diagram used in the three cell, discrete time simulations of Section 5.1.3.The three dark green blocks represent each smart cell. The electrical connections can be traced by following the +Vsc and -Vsc ports of each smart cell block.

Fig. B.2 shows the Simulink block diagram of a smart cell, one of the dark green blocks of Fig. B.1. The orange block, called *SCKDCS1*, contains the smart cell code, implemented as a MATLAB function. The many inputs and outputs of this block are used to fine tune the algorithm.

The yellow block, called *Plot System Vectors*, was used to visualize outputs of the smart cell controller during the simulation. Fig. B.3 shows a screen shot of the figure that is produces by all three of the *Plot System Vectors* blocks. The top row

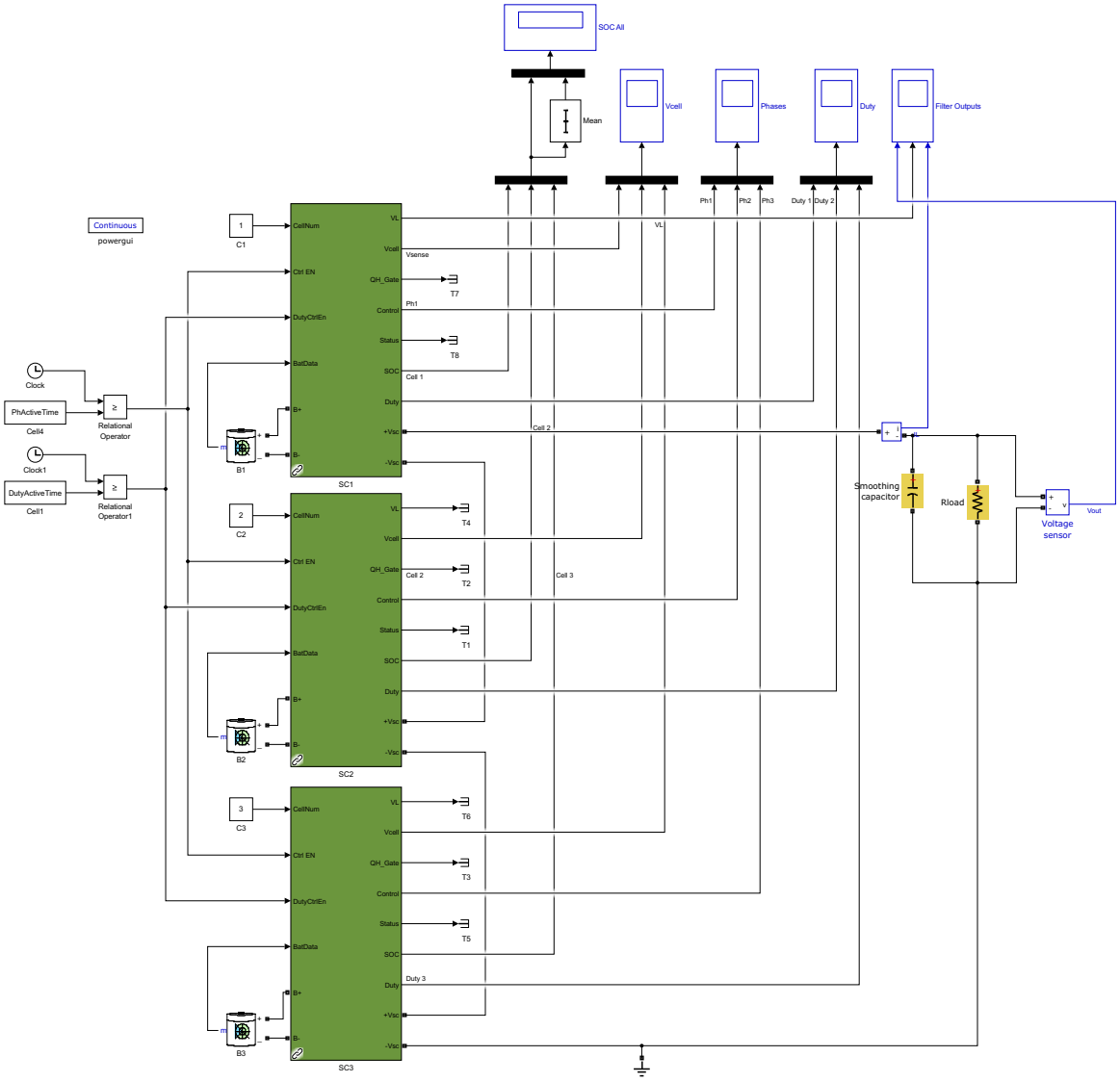

Fig. B.1: Top level Simulink block diagram of a three smart cell system.

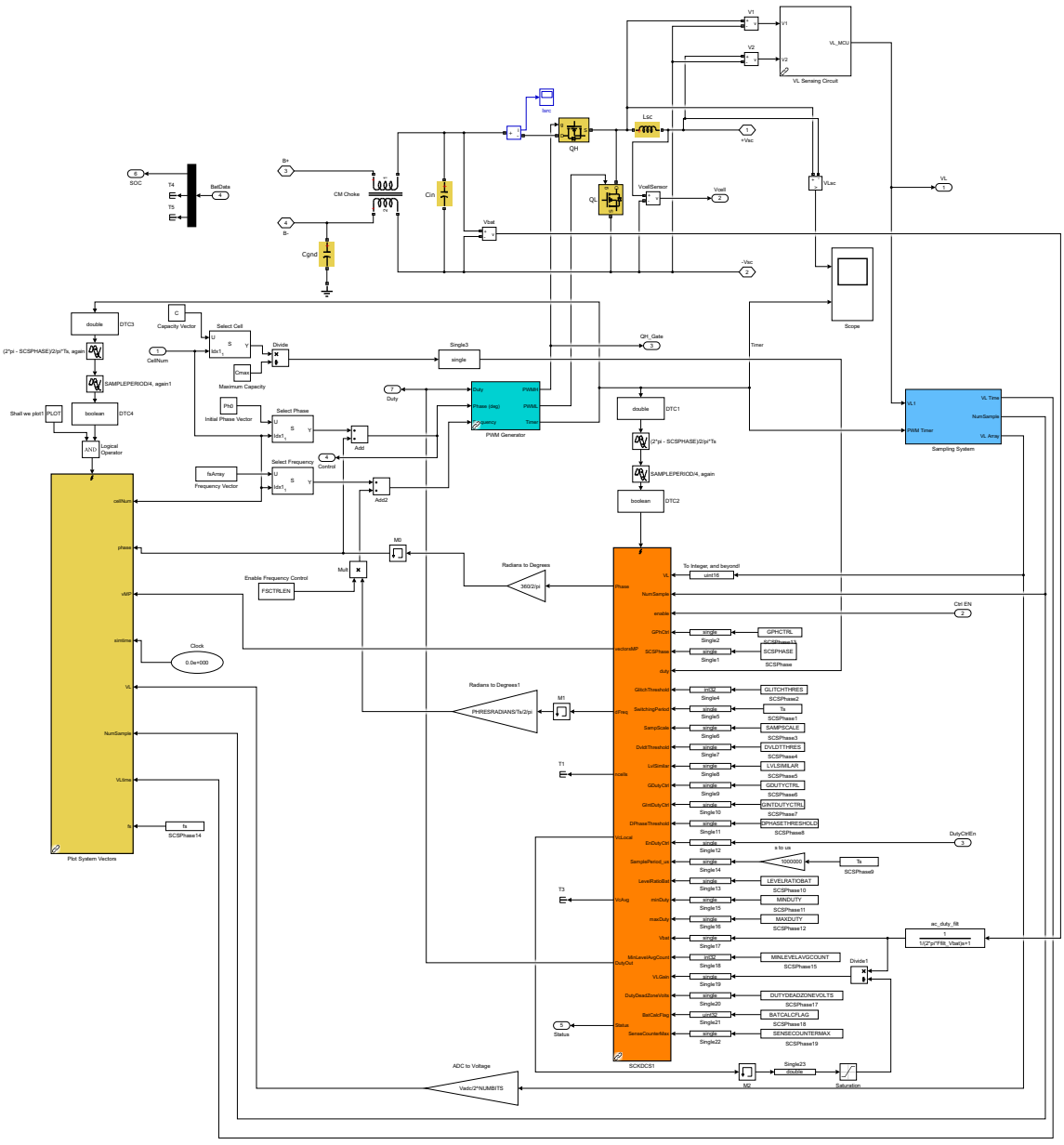

Fig. B.2: Simulink block diagram of SC1, of Fig. B.1.

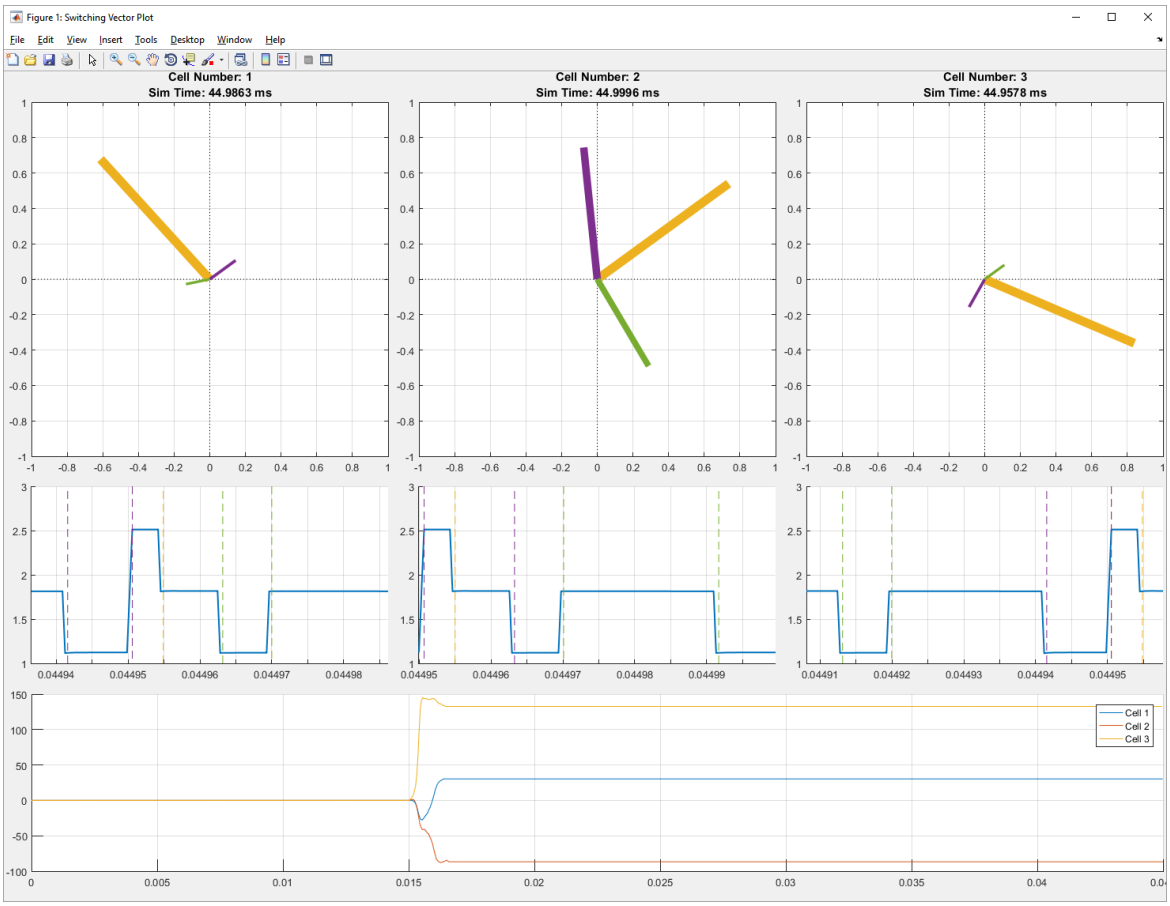

Fig. B.3: Screen shot of the output of a three smart cell simulation. Each *Plot System Vectors* block of each smart cell, plots the cells it detects as vectors in its respective top plot, the voltage measured across L_{sc} in its respective middle plot, and its phase shift in the bottom plot.

of plots visualized the cells sensed by each smart cell. The magnitude of the vector is proportional to the sensed duty cycle, and the angle of the vector is the switching angle of Q_H. These vectors do not represent the transformed vectors as defined by (4.12) and (4.13), simply because this graphical user interface was developed before this concept was discovered. The middle row of plots shows the voltage across each cell's local L_{sc}, as measured by each cell. The bottom plot is the evolution of each cell's phase shift over time.

B.2 Inputs and outputs

The smart cell controller has many inputs, which are used to fine tune several aspects of the controller, and many outputs, which are used for status and debugging purposes. This section will explain each one in detail.

The function call looks like this:

```
1 function [phase, dFreq, vectorsMP, f_ncells, VcLocal, VcAvg, duty_out, int32_Status]
    = SCSController(VL, NumSample, enable, duty, GPhCtrl, switchingPeriod, SCSPhase,
    GlitchThreshold, SampScale, DvldtThreshold, LvlSimilar, GDutyCtrl, GIntDutyCtrl,
    dphase_threshold, en_duty_ctrl, SamplePeriod_us, LevelRatioBat, minDuty, maxDuty,
     Vbat, VLGain, MinLevelAvgCount, DutyDeadZoneVolts, BatCalcFlag,
    int32_SenseCounterMax)
```

B.2.1 Inputs

VL

An array of 16 bit unsigned integers from the ADC of the sampled voltage across L_{sc}. The size of the array should be the same as `MAXBUFF` = 256, which is defined on line 23 of the function.

NumSample

A 32 bit integer that indicates the number of samples that were taken be the ADC.

enable

A boolean value that enables and disables the phase controller. Set to true to enable the phase controller. Set to false to disable the phase controller.

duty

A float value between 0 and 1 that indicates the duty cycle that has been applied to the switching network.

`GPhCtrl`

A float value that corresponds to the gain of the phase controller.

`switchingPeriod`

A float value which defines the switching period in seconds.

`SCSPhase`

A float value which defines the phase angle between the rising edge of Q_H and the first sample of the ADC, in radians. It is used to fine tune the timing between these two events to ensure the phase controller timing is accurate. Normally set to $(10/102)\,2\pi$.

`GlitchThreshold`

A 32 bit integer that indicates the number of samples after a switching event has been detected that must be free of switching events before another switching event is recorded. Normally set to 1.

`SampScale`

A float value which is used to fine tune the number of samples in a switching period, and is used when calculating duty cycles and phase angles from the switching events. Normally set to 0.997. Equation B.1 demonstrates its usage.

$$D_i = \frac{\texttt{abs}\left((\texttt{Index of positive transition}) - (\texttt{Index of negative transition})\right)}{\texttt{NumSample} \cdot \texttt{SampScale}} \tag{B.1}$$

`DvldtThreshold`

A float value indicating the dV_{Lsc}/dt threshold at which to record a switching event. The units are raw ADC values, and it is normally set to 192.

`LvlSimilar`

A float value indicating the minimum difference between two adjacent levels to ensure that the adjacent levels are unique. The units are raw ADC values, and it is normally set to 192.

`GDutyCtrl`

A float value used as the proportional gain of the SOC controller.

`GIntDutyCtrl`

A float value used as the integral gain of the SOC controller.

`dphase_threshold`

A float value indicating the maximum value of change in phase from the phase controller that is permitted while the SOC controller is running. The state of charge controller outputs a constant duty cycle when the change in phase from the phase controller is larger than this value. It is normally set to 0.1.

`en_duty_ctrl`

A float value that enables and disables the SOC controller. Set to 1 to enable the SOC controller. Set to 0 to disable the SOC controller.

`SamplePeriod_us`

A float value of the sampling period. The units are μs. Normally set to 40/111.5, and measured using the oscilloscope.

`LevelRatioBat`

A float value which determines the number of samples between switching events to average. This average becomes the voltage values of that level. When `LevelRatioBat` is less than 1, a ratio of the number of samples is used. For example, if `LevelRatioBat` = 0.5, 0.5 $\times$ (the number of samples between two consecutive switching events) = (the number of samples used in the average). When `LevelRatiobat` is greater than or equal to 1, that many number of samples are used in the average. Normally set to 0.5.

`minDuty`

A float value between 0 and 1 that determines the minimum duty cycle that can be output by the SOC controller.

`maxDuty`

A float value between 0 and 1 that determines the maximum duty cycle that can be output by the SOC controller.

`Vbat`

A float value which is the voltage reading of the local battery cell. Units of volts.

`VLGain`

A float value which is the gain of the V_{Lsc} sensor. It is calculated outside of this function, and is used to convert the raw ADC values to voltage value.

`MinLevelAvgCount`

A 32 bit signed integer which indicates the minimum number of samples that must have been averaged in order to consider a level measurement as valid. Normally set to 2.

`DutyDeadZoneVolts`

A float value which determines the dead zone used for the SOC controller. Units of volts. When the difference between the local cell voltage and the average string voltage is within ±`DutyDeadZoneVolts`, the error fed into the SOC controller is 0. Normally set to 0.01.

`BatCalcFlag`

A 32 bit unsigned integer whose bits are used as flags to determine which level measurements to use when calculating the voltage differences between levels. There are two level measurements (or averages) for each level: 1) a "front" measurement, and 2) a "back" measurement. The length of the front and back measurements are the same, and are determined by LevelRatioBat. Fig. B.4 graphically illustrates the front and back level for one of the levels of the V_{Lsc} waveform. Table B.1 lists what the active bits control. All of the other bits are ignored. Normally set to 257.

`int32_SenseCounterMax`

A 32 bit signed integer used to indicate the maximum number of times the duty cycle controller can execute without being able to make a good measurement. This is used to adjust the time before a large step in duty cycle is introduced so that the SOC controller can make voltage measurements on the string. Normally set to 12000, which corresponds to about 2.5 minutes.

Table B.1: Control bits of `BatCalcFlag`.

Bit	Value	Description
9	1	If the transition is negative, use the front level calculation for the level measurement before the transition.
	0	If the transition is negative, use the back level calculation for the level measurement before the transition.
8	1	If the transition is negative, use the front level calculation for the level measurement after the transition.
	0	If the transition is negative, use the back level calculation for the level measurement after the transition.
1	1	If the transition is positive, use the front level calculation for the level measurement before the transition.
	0	If the transition is positive, use the back level calculation for the level measurement before the transition.
0	1	If the transition is positive, use the front level calculation for the level measurement after the transition.
	0	If the transition is positive, use the back level calculation for the level measurement after the transition.

B.2.2 Outputs

`phase`

A float value which indicates the phase of the PWM module. Units of radians. Its value is restricted to the closed interval $[\pi, -\pi]$.

`dFreq`

A float value which can be added to the switching frequency to synchronize the clock signals of all of the smart cells. Due to the relatively coarse sampling of the hardware used in this thesis, this output was not used.

`vectorsMP`

A `MAXBUFF` $\times$ 2 array of floats which stores the weighted sum vectors, as described in Section 4.2, of all of the smart cells detected in the last execution of the controller.

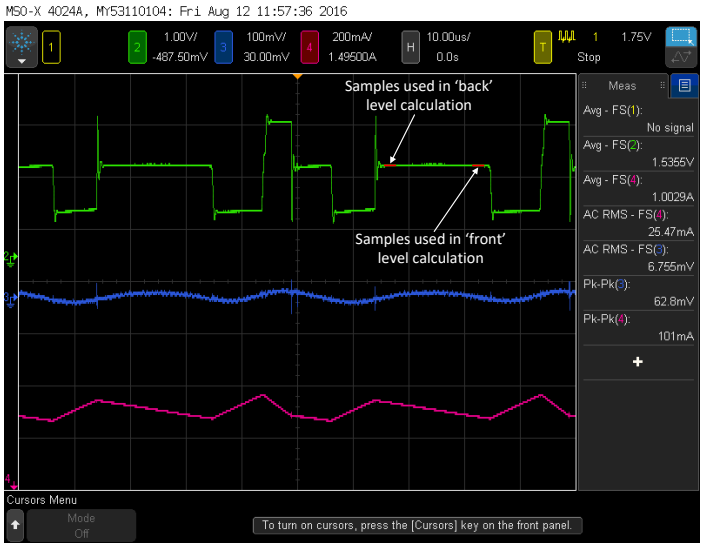

Fig. B.4: Oscilloscope screen shot of the voltage across a smart cell inductor, with the "back" and "front" areas of the level highlighted.

The first column of this array is the magnitude of the vector, and the second column is the phase of each vector.

`f_ncells`

A float value of the number of smart cells detected. This value is filtered by the controller to yield an average.

`VcLocal`

A float value of the local cell voltage as measured across L_{sc}, in raw ADC units.

`VcAvg`

A float value of the average cell voltage in the string, in units of volts.

`duty_out`

A float value indicating the new duty cycle for the PWM module. When the SOC controller is disabled, the input `duty` is passed through to `duty_out`.

`int32_Status`

A 32 bit integer indicating the status of the SOC controller. The possible values and their meanings are summarized in Table B.2.

Table B.2: Summary of `int32_Status` values.

Value	Description
0	Successful execution of the SOC controller.
1	Local cell voltage is out of expected range.
2	Only the turn on time of the local cell was found, and used to calculate the local value.
3	Only the turn off time of the local cell was found, and used to calculate the local value.
4	Neither the turn on or turn off time of the local cell was found.
5	`dphase_threshold` is exceeded.
6	BV_weight = 0, the weight attributed to the local cell.
7	There are too many zero weights, cannot compute the average cell voltage.
8	`f_AvgBatVoltsWeights` == 0.
9	Only the turn on time of the local cell was found, but the gain was zero, or multiple transitions occurred.
10	Only the turn off time of the local cell was found, but the gain was zero, or multiple transitions occurred.
11	Both transition were found, but only the turn on transition can be used.
12	Both transitions were found, but only the turn off one can be used.