Single-Stage Multilevel ac/dc Conversion using Monolithic Bidirectional Switches

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***Abstract*—The recent invention of the Gallium Nitride (GaN) based monolithic bidirectional switch (MBDS) has unlocked new possibilities for power converter topologies and revamped interests in old topologies that have great theoretical merits but were deemed unattractive due to lack of access to MBDSs. This paper experimentally demonstrates a new power conversion topology (called the Cascaded Resonant Bridge or CRB) using such MBDS GaN transistors. The core of this topology is an isolated resonant dc-dc converter with high control bandwidth that can be connected in series/parallel/cascade to synthesise scaled-up ac or dc voltage (and power) as required. Theoretical and experimental works give evidence that the CRB can be a drop-in replacement for the widely used cascaded H-bridge (CHB) circuit with one less power conversion stage.**

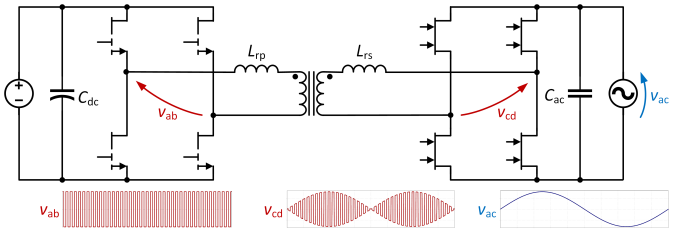
***Index Terms*—cascaded H-bridge, CHB, $CLLC$ converter, MBDS, monolithic bidirectional switch, multilevel converter, resonant converter, single-stage converter**

I. Introduction

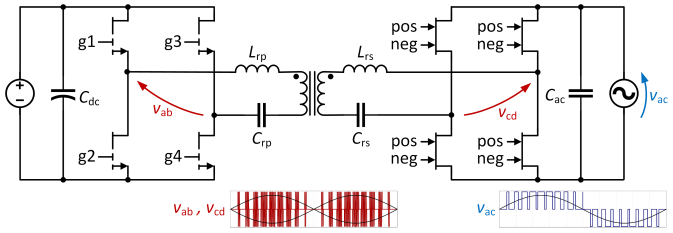
Isolated ac-dc (and dc-ac) conversion is an important part of many systems that connect to the ac electricity grid. In its unidirectional form, it delivers power to dc loads (e.g., data center servers) from the ac grid, or feeds power into the ac grid from dc source (e.g., solar photovoltaic source). In its bidirectional form, it allows a flexible exchange of power between ac grid and dc source (e.g., grid-connected battery storage, solid-state transformer). For high-power (above 1 MW) applications, the system comprises a grid-frequency (50-60 Hz) transformer and an active bridge circuit that acts either as a rectifier or as an inverter based on the direction of power flow. For low and medium power (up to 100 kW) applications, the isolation is usually achieved with a high-frequency power electronics transformer having active bridge circuits on both sides.

The most common scheme uses a high-frequency transformer-isolated dc-dc converter in the first stage, followed by a high-frequency inverter in the second stage [1], [2]. A large dc-link capacitor (usually an electrolytic capacitor) is used in between the two stages to buffer the power ripple.

To improve power density, a quasi-single-stage isolated ac/dc conversion scheme was introduced in [3], [4], where a dual active bridge (DAB) is modulated in such a way that it produces a rectified (folded) ac voltage in its ac-side. This is then unfolded by an unfolder circuit switching at the grid frequency to produce a bipolar ac voltage.



(a) Single-stage ac/dc converter from [5].



(b) Proposed single-stage ac/dc converter.

Fig. 1. Different ways of single-stage ac/dc conversion using bidirectional switches. Voltages are shown at different parts of the converters.

To further push the power density up, reference [6] proposed a single-stage ac/dc converter using bidirectional switches in the ac-side bridge of the DAB. A bidirectional switch is a four-quadrant switch that blocks voltage and allows current in both directions. It can be realised using two MOSFETs in a back-to-back series connection (either common-source or common-drain) that utilises only half of the capacity of each MOSFET. Like many variants of the matrix converter, this converter also stayed only as a research interest for a long time, with underutilisation of devices as one of the primary drawbacks. With the recent development of monolithic bidirectional switches (MBDS), that use the full capacity of the device, there is renewed interest in such topologies [7]–[10].

The modulation scheme for the MBDS-based single-stage ac/dc converter, as shown in Fig. 1(a), is complex and the ac current total harmonic distortion (THD) is poor because of the distortion caused near the zero-crossing of the grid-frequency current [5], [11]. Moreover, the output cannot be cascaded to

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generate multilevel ac voltages needed for medium- and high-voltage ac applications.

This paper presents a novel single-stage isolated ac/dc converter that can be easily cascaded to produce multilevel ac voltages for medium- and high-voltage ac applications. It uses a Gallium Nitride (GaN) based isolated dc-dc $CLLC$ resonant converter, as shown in Fig. 1(b), as the building block [12]. Similar to the topology in [5], the proposed converter has four unidirectional MOSFETs in the dc-side full-bridge and four MBDSs in the ac-side full-bridge (rectifying bridge). However, unlike [5], the MBDSs in the proposed topology are not switched at the high switching frequency. They work in either body-diode conduction mode (GaN reverse conduction mode) or synchronous rectification mode, and are switched only at the grid frequency. Thus, the proposed topology avoids large switching losses in the ac-side bridge. The MHz switching-frequency operation of the GaN-based $CLLC$ resonant converter allows high control bandwidth [13], [14], which in turn allows us to synthesise ac waveforms at grid frequency by enabling and disabling the converters at a few kHz frequencies.

II. Principle of Operation

A. Topology

The proposed single-stage multilevel ac/dc converter topology, which we are calling as 'cascaded resonant bridge' (CRB), is shown in Fig. 2(b). The CRB is conceptually similar to the conventional cascaded H-bridge (CHB) topology, as shown in Fig. 2(a), with one less conversion stage. Each ac/dc module in the CRB is a $CLLC$ resonant converter shown in Fig. 1(b). Three such ac/dc modules are connected in cascade here producing a seven-level ac output voltage. More generally and similar to the CHB, a CRB with n modules can produce an ac voltage waveform with $(2n+1)$ levels.

The dc-side can have either a common dc voltage source for all modules, or an individual dc voltage source per module. Additionally, for a three-phase ac application, three CRB converters can be connected in a star or delta configuration on the ac-side.

B. Modulation and Control

Fig. 3 shows the modulation and control scheme of the proposed CRB converter, where three distinct frequencies are present. The dc-side full-bridge of each ac/dc converter module operates at 1 MHz switching frequency (f_{s}), which is slightly below the resonant frequency (f_{r}) of the $CLLC$ resonant tank [15]. The MBDSs in the ac-side full-bridge work in diode-rectifier mode, and are switched at the grid frequency ($f_{\text{g}} = 50$ Hz). Therefore, the ac-side full-bridge achieves the combined functionality of a full-bridge diode rectifier and an unfolder circuit. Finally, each ac/dc converter module is turned on/off (enabled/disabled) at a frequency (f_{en}) of 1 kHz using a sinusoidal pulse width modulation (PWM) technique.

This type of modulation is possible because of the high control bandwidth of the $CLLC$ resonant converter, which appears as perfect voltage sources at 1 kHz burst-mode operation. Similar to CHB, the multilevel on/off signals for the ac/dc modules can be generated using phase-shift PWM (PSPWM), level-shift PWM (LSPWM), or model predictive control (MPC). PSPWM is chosen in this study owing to its better load-balancing feature compared to LSPWM, and easier implementation compared to MPC.

A proportional-resonant (PR) current control is employed to maintain the desired power factor in the ac-side. It also ensures precise detection of zero-crossing of ac current which is critical to toggle between the 'pos' and 'neg' signals (that control the MBDSs) without causing large current spikes.

III. Design Considerations

A. Power Rating of Each Module

In a single-phase application, under unity power factor, each ac/dc module should be designed for a peak power of

$$P_{\text{m}} = 2P/n, \tag{1}$$

where P is the power rating of the whole converter and n is the number of ac/dc modules used. However, from a thermal design perspective, the average power rating of each ac/dc module is

$$< P_{\text{m}} >= 2P_{\text{m}}/\pi = 4P/(n\pi). \tag{2}$$

B. Output Capacitance

The ac-side capacitance (C_{ac}) must be at least 10 times higher than the resonant capacitance C_{rs} to avoid resonance with the resonant inductance L_{rs}.

$$C_{\text{ac}} \geq 10C_{\text{rs}}. \tag{3}$$

An upper bound of C_{ac} should also be defined as

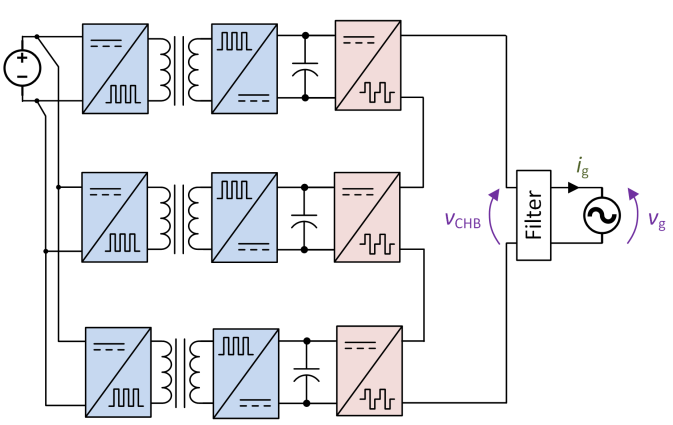
$$C_{\text{ac}} \leq \tau/(3nR_{\text{L}}), \tag{4}$$

where R_{L} is the equivalent load resistance assuming unity power factor operation, and τ is the desired time constant for the discharge of C_{ac} in the worst case (when all n modules are on). The capacitance C_{ac} discharges by 95% in 3τ seconds. If the discharge time is too large, a distortion is observed in the PWM ac voltage (v_{ac}).

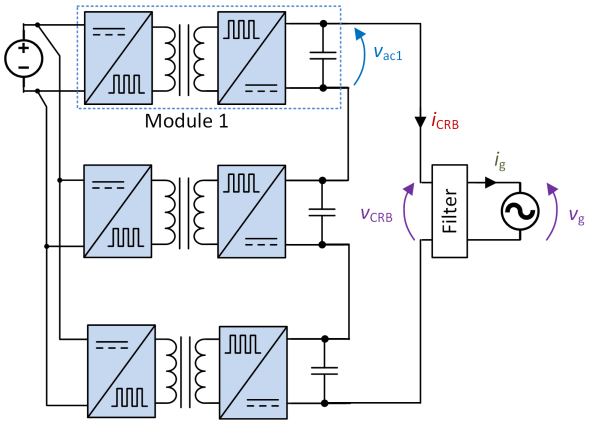
C. Soft Start

High inrush current at startup is a common issue in $CLLC$ converters due to the inherently capacitive nature of the output filter. To mitigate this, techniques such as ramping down the switching frequency or ramping up the duty cycle are commonly employed to enable a soft start and limit inrush current [16].

In our implementation, we applied a duty cycle ramp from 0 to 0.5 over 10 switching cycles. It is important to note that with a frequency ratio of $f_{\text{s}} : f_{\text{en}} = 1000 : 1$, increasing the number of switching cycles for the ramp can result in distortion near the zero-crossing of the 50 Hz voltage/current waveform. This occurs because the modulation index window available for sinusoidal PWM is effectively reduced during this interval.



(a) Cascaded H-bridge (CHB).



(b) Cascaded resonant bridge (CRB).

Fig. 2. Multilevel ac/dc conversion schemes - Conventional cascaded H-bridge (CHB), and proposed cascaded resonant bridge (CRB). The CRB shows one less number of power conversion stage.

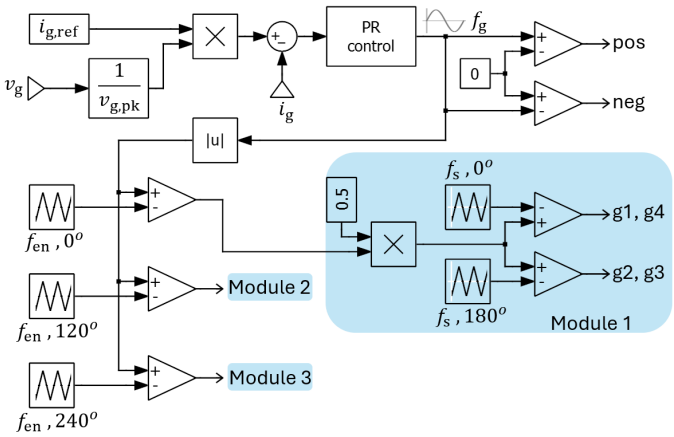


Fig. 3. Modulation and control of the proposed converter. Gate signals 'pos' and 'neg' are common for all modules. Example frequencies: $f_g = 50$ Hz, $f_{en} = 1$ kHz, $f_s = 1$ MHz.

TABLE I
CONVERTER DESIGN PARAMETERS

Parameter	Value
Number of modules (n)	3
Rated power (P)	3 kW
DC voltage (V_{dc})	108 V
Grid voltage (V_g)	230 V (rms)
Grid frequency (f_g)	50 Hz
Module enable/disable frequency (f_{en})	1 kHz
Switching frequency (f_s)	1 MHz
$CLLC$ resonant frequency (f_r)	1.11 MHz
Resonant (leakage) inductance (L_{rp}, L_{rs})	133 nH
Resonant capacitance (C_{rp}, C_{rs})	154 nF
Magnetising inductance (L_m)	3 μH
Transformer turns ratio (N)	1
Deadtime (t_d)	30 ns
DC-side devices	EPC2034C
AC-side devices	GS66516T

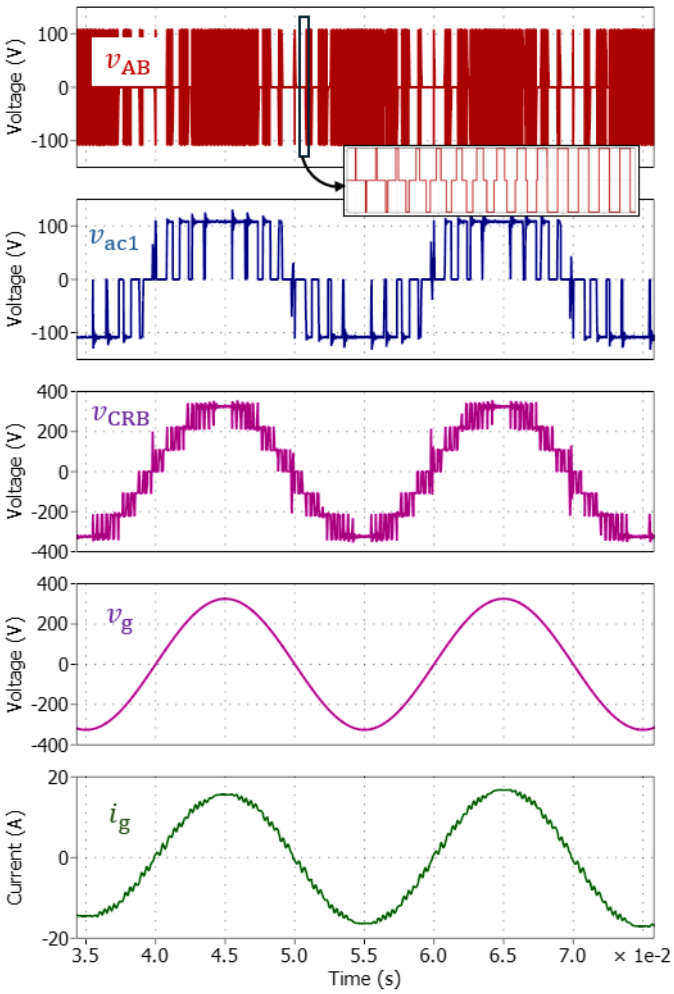


Fig. 4. Simulated multilevel voltage/current waveforms demonstrating arbitrary voltage/power synthesising capability of the proposed CRB topology. Zoomed inset figure showing soft start of the ac/dc module. Note the different frequencies of Hz, kHz, and MHz utilised at different control stages of the converter.

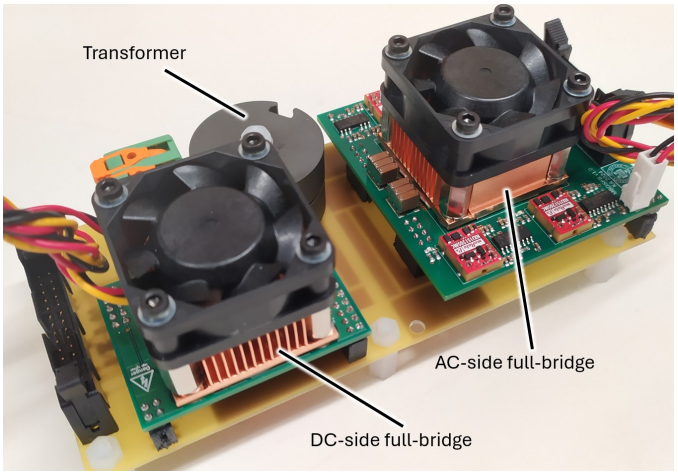
IV. Results and Discussion

A. Simulation

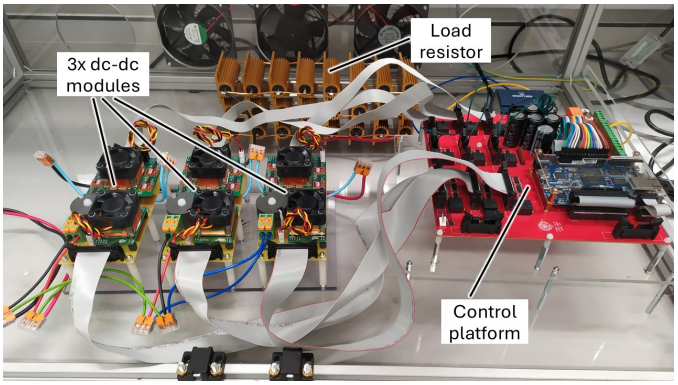
The CRB converter in Fig. 2(b) was simulated in PLECS to validate the proposed concepts. The design parameters of the simulated system are listed in Table I.

Fig. 4 shows the key voltage and current waveforms from the simulation. The close loop control ensures near unity power factor and very low current THD. The output voltage v_{CRB} has seven distinct levels. The voltage v_{ac1} shows the enabled/disabled state of the ac/dc module at frequency f_{en}, and the voltage v_{AB} shows the dc-side full-bridge switching at frequency f_{s}. It also shows in the zoomed inset figure that for the first 10 switching cycles, the duty is ramped from 0 to 0.5 to ensure the soft start of the ac/dc modules at every enable signal.

B. Experimental Setup



(a) One dc-dc module.



(b) Experimental setup.

Fig. 5. Experimental setup for the seven-level dc-ac converter using the proposed CRB concept.

A prototype is also built as per the converter specifications in Table I, and is shown in Fig. 5. It has three $CLLC$ ac/dc converter modules, whose ac-side outputs are connected in series and the dc-side inputs are connected in parallel. A symmetrical $CLLC$ resonant tank with a transformer turns ratio of 1 is designed. The bidirectional device for the ac-side full-bridge is implemented with a common-drain back-to-back connection of two GS66516T GaN high electron-mobility transistors (HEMT). The dc-side full-bridge is implemented with EPC2034C GaN HEMTs. Gate pulses for both dc- and ac-side transistors are generated in an Intel DE-10 FPGA platform.

C. Testing

Some scaled-down preliminary testing was performed on the prototype. Fig. 6 shows the multilevel ac output voltage and current waveforms at 50 Hz frequency. The inputs are connected in parallel to a 50 V dc source and the CRB is tested in open loop with a resistive load (i.e., unity power factor). Seven distinct levels are observed in the waveforms owing to the presence of three modules in the system. No discontinuity is observed at the zero-crossing of the ac current.

Fig. 7 shows the resonant tank current of one of the ac/dc modules for one line cycle (20 ms). The burst mode operation of the module at 1 kHz on/off frequency is apparent in this figure. Note that even with the ramp control of the duty cycle, the inrush current at the enable edges is rather high. This requires further work.

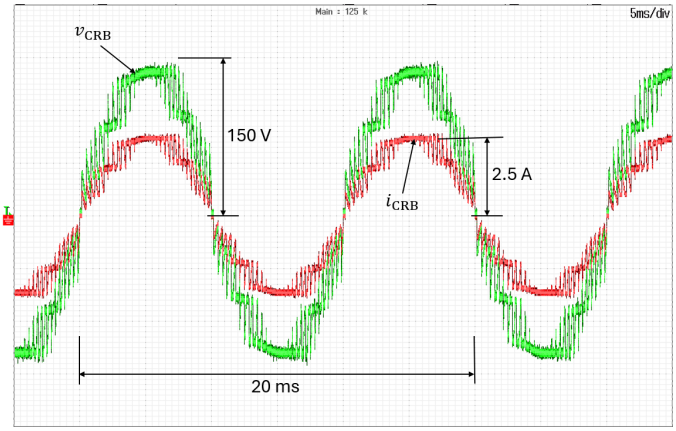


Fig. 6. Multilevel (7 levels) ac voltage and current waveforms generated by the prototype of the proposed CRB converter tested with a resistive load.

D. Power Losses

A major source of power loss is the reverse conduction of GaN HEMTs on the ac-side. This can be reduced by implementing synchronous rectification. The rest of the losses in the converter can be estimated in the same way as for a normal $CLLC$ dc-dc converter [17] with a scaling factor of $2/\pi$ owing to its ac/dc mode of operation.

V. Conclusions

This paper has presented the design and demonstration of a novel power conversion topology – the Cascaded Resonant Bridge (CRB) – that enables single-stage multilevel ac/dc conversion using GaN-based monolithic bidirectional switches (MBDS). Central to the CRB architecture is the $CLLC$ resonant converter, which was chosen as the modular building

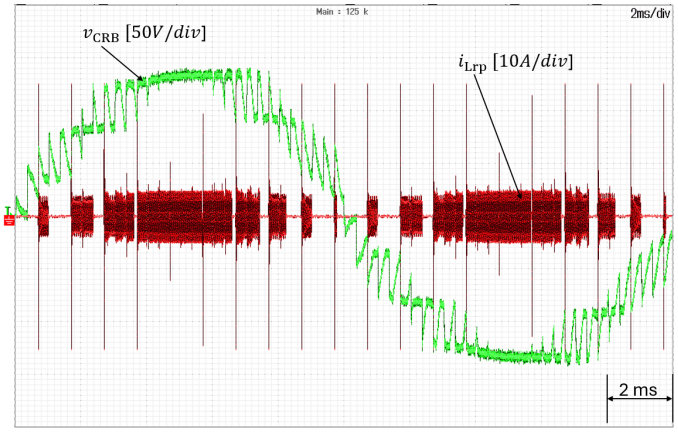


Fig. 7. Red trace showing the resonant tank current of one of the modules. The on/off frequency ($f_{\mathrm{en}} = 1$ kHz) of the module and the inrush current issue are apparent in this scope capture.

block for its exceptional suitability in high-performance power conversion systems.

Several features make the GaN-based $CLLC$ converter particularly effective for CRB implementation. First, its high control bandwidth allows precise and rapid modulation, essential for synthesizing grid-frequency waveforms in real time. Second, the $CLLC$ topology naturally achieves load-independent soft switching, ensuring efficient operation across the full line cycle (grid-voltage period) where the load seen by the module varies widely. Third, its open-loop modulation simplicity achieved through fixed-frequency operation at 0.5 duty cycle (with initial ramp) reduces control overhead and complexity. Finally, when operated near its resonant frequency, the $CLLC$ exhibits ideal voltage-source behavior, a crucial requirement for cascaded multilevel systems where the quality of the synthesized ac output depends on the quality of the dc voltage levels.

The CRB concept is inherently suited to multilevel and three-phase applications. For low-voltage single-phase systems, such as standard 240 V ac residential interfaces, output waveform quality and resolution are limited by the number of practical voltage levels. Given the voltage limitations of GaN devices (up to 700 V) at the time of writing this, realistic deployment scenarios for CRB include medium-voltage applications, such as 400 V dc to 11 kV ac photovoltaic (PV) systems.

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