Hierarchical Distributed Balancing Control for Large Scale Reconfigurable AC Battery Packs

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***Abstract*—This paper presents a hierarchical balancing algorithm for use in large scale reconfigurable AC battery packs. Using a decentralised Battery Management System (BMS) the pack is organised in control layers with each layer controller responsible for a small number of slave controllers, thereby significantly reducing communication and centralised processing requirements. The hierarchical balancing algorithm uses all available voltage steps in the pack ensuring a high quality sinusoidal output voltage while balancing the objects of different layers. Balancing priority can be swapped dynamically between layers according to the maximum SoC variation between the objects of each layer while also ensuring that the output voltage reference is always met even when a cell failure occurs, as long as there are an adequate number of cells available in the pack. An experimental demonstration of the proposed balancing algorithm is presented using an AC battery pack comprising 144 20Ah lithium titanate cells. Cell balancing to within 2 mV of the cell open circuit voltage is achieved between cells with 20% initial State of Charge variation and 5% capacity difference.**

***Index Terms*— Battery management system, cell balancing, distributed, lithium-ion batteries, multilevel converter**

NOMENCLATURE

SoC^{ijk}	State of Charge of element k in module j of bank i
SoC^{ij}	Average State of Charge of elements in module j of bank i, $SoC^{ij} = \frac{\sum_{k=1}^{N_e} SoC^{ijk}}{N_e}$
SoC^{i}	Average State of Charge of modules in bank i, $SoC^{i} = \frac{\sum_{j=1}^{N_m} SoC^{ij}}{N_m}$ (except in Fig.1a where SoC^{i} refers to the SoC of element i since no other layers are used)
V^{ijk}	Voltage of element k in module j of bank i
$V_{\max}^{ij}$	Maximum output voltage of elements in module j of bank i, $V_{\max}^{ij} = \sum_{k=1}^{N_e} V^{ijk}$
$V_{\max}^{i}$	Maximum output voltage of modules in bank i, $V_{\max}^{i} = \sum_{j=1}^{N_m} V_{\max}^{ij}$
$V_{\max}$	Maximum output voltage of the system, $V_{\max} = \sum_{i=1}^{N_b} V_{\max}^{i}$
V_{ref}^{ij}	Voltage reference for the controller of module j of bank i
V_{ref}^{i}	Voltage reference for the controller of bank i
S^{ijk}	Switching signals for the H-bridge of element k in module j of bank i
ΔSoC^{ij}	Maximum SoC variation between elements in module j of bank i i.e. SoC difference between the element with the highest SoC and the element with the lowest SoC in module j of bank i
ΔSoC^{i}	Maximum SoC variation between modules in bank i i.e. SoC difference between the module with the highest average SoC and the module with the lowest average SoC in bank i
ΔSoC	Maximum SoC variation between banks i.e. SoC difference between the bank with the highest average SoC and the bank with the lowest average SoC
N_e	Number of elements within a module
N_m	Number of modules within a bank
N_b	Number of banks in the CHB
V_e	Average element voltage
V_m	Average module voltage
V_b	Average bank voltage
V_S	Voltage step (i.e. the variable used to control balancing priority between layers)
PSU	Power Supply Unit
ADC	Analog-to-Digital Converter

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I. INTRODUCTION

IN conventional battery packs cells are configured in series and parallel in a static manner in order to satisfy a voltage and capacity specification [1]. The total capacity of the pack is limited by the weakest cell i.e. the cell with the lowest capacity or State of Charge (SoC) [2]. Cell capacities naturally vary, initially due to imperfections in the manufacturing process but also due to subtle differences in operating conditions between cells that cause a spread in degradation rates [3-5]. As a result, large-scale *reconfigurable battery packs* along with corresponding Battery Management Systems (BMSs) [6] have been proposed for a wide range of applications [7, 8]. In reconfigurable battery packs, additional power electronics are included in the battery pack allowing cells to be bypassed during operation in case of failure and to achieve active balancing by controlling the duty cycle of each cell according to their relative SoC [9, 10]. Recent work has shown that enhanced reliability can be achieved using reconfigurable battery packs without necessarily increasing the overall cost of the system, typically as a result of better cell utilisation when compared to conventional designs [11-

13]. The BMS architectures used with reconfigurable battery packs are often categorised into two types: *flat* and *modular* [7, 14]. In a flat BMS a centralised controller is responsible for monitoring the states of the individual cells (cell voltage, SoC etc.), processing this information and providing the switching signals for the active switches. This type of architecture is inherently very difficult to scale as the wiring complexity and communication latency increases unacceptably with the number of cells [14]. In contrast, the modular BMS architecture is a decentralised scheme where local controllers are only in charge of a subset of entities. A decentralised BMS can provide several significant practical advantages such a greatly reduced wiring harness [15] and simple scalability which facilitates rapid construction of different sized systems and leading to a reduced time-to-market.

In a typical reconfigurable battery pack, a cell or group of cells are connected in series using half-bridge converters [9]. The output of this battery pack is a DC voltage with a controllable magnitude, according to the number of cells that are connected in series. For grid storage applications however, where the pack is to be connected to an AC grid, an additional monolithic DC to AC converter is required. With the inclusion of some additional power electronics inside the pack, the converter can be subsumed into the pack and the need for a monolithic converter can be eliminated. This results in a battery pack that produces a controllable AC output voltage. One such design uses the Cascaded H-bridge (CHB) multilevel converter [16], this is an attractive topology due to the very high output voltage waveform quality, low-frequency operation and the use of low-voltage MOSFET switches [17]. The CHB provides direct DC to AC conversion and enables individual control over cells (or modules), allowing the implementation of active balancing schemes without additional balancing circuits [18, 19]. As long as redundant cells are included in the pack, failed cells can be bypassed online without affecting overall operation of the system leading to greatly enhanced reliability compared to conventional packs. Although the CHB power circuit is inherently scalable to large numbers of cells and output high voltages, the control of a grid scale system comprising tens of thousands of cells would be very challenging if a flat BMS organisational approach is followed (Fig. 1a). This is principally because in order to produce a stepped voltage waveform that accurately follows a sinusoidal reference and to maintain stability of the grid current controller, switching signals must be updated at a relatively high rate and with low latency. As shown in Fig. 2, each H-bridge must be updated four times in each cycle of the mains waveform: i.e. in each positive and negative half-cycle the H-bridge must be turned on and off, and these events must occur with high resolution in time. For a 50 Hz grid frequency this equates to an average 200 Hz update rate along with better than 100 us time resolution (the former is to ensure a high quality wave-shape and provide adequately low loop delay for a centralised current controller to track the grid voltage). These observations make the flat approach increasingly impractical to implement as cell-count increases. For example, a flat control scheme for a large grid-scale battery pack with 50,000 individually controllable cells (generating 200,000 switching events per grid cycle), assuming 16 bits for the packet address and 4 bits for the H-bridge switching signals results in a data rate at the central controller of 200 Mbits/s for a grid frequency of 50Hz. This implies a very large communication and computational load for the master controller.

A modular BMS following a hierarchical control structure such as that presented in [20] goes some way to addressing this problem. Here, the elements of the CHB are organised conceptually into control layers, labelled *banks*, *modules* and *elements*.

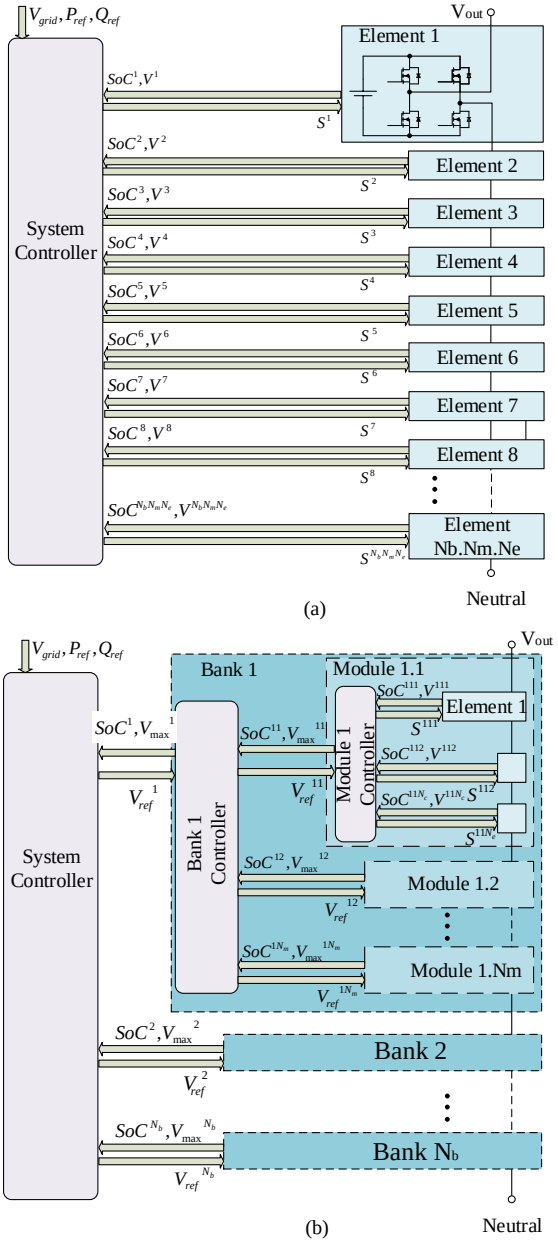


Fig. 1. Different control system design approaches for a CHB AC battery pack comprising $N_b N_m N_e$ elements. a) A flat BMS structure where a central controller gathers information from all elements and produces switching signals for each H-bridge. b) The proposed hierarchical system structure where the BMS is organised in three conceptual control layers: N_b banks, each bank includes N_m modules and each module contains N_e elements.

TABLE I
Comparison of proposed balancing algorithm with existing work in literature.

	Proposed balancing algorithm	**Ooi et al. [20]**	**Young et al. [21]**	**Maharjan et al. [18, 19]**
Advantages	Scalable balancing algorithm. Output voltage limitations are integrated in algorithm. 100 Hz maximum switching frequency. Experimentally validated using single-phase 289-level CHB.	Scalable balancing algorithm. Output voltage limitations are considered. 100 Hz maximum switching frequency. Number of values sent from slaves to master: $2N_S$ (SoCs and voltages for N_S objects).	Harmonics elimination. 100 Hz maximum switching frequency. Experimental validation for a single-phase 7-level CHB.	Balancing achieved by active power control of each converter element. Experimentally validated for a three-phase 7-level CHB.
Disadvantages	Number of values sent from slaves to master: $2N_S + 1$ (SoCs and voltages for N_S objects and maximum ΔSoC, i.e. one more than [20]). Low inter-layer latency required for accurate following of the reference waveform.	Additional peak sharing algorithm necessary. Not all available voltage steps are utilised when cells balanced. Low inter-layer latency required for accurate following of the reference waveform.	High computational complexity (obtain switching angles using Newton-Raphson). Not scalable.	Higher switching frequency (800 Hz phase-shifted pulse width modulation). Output voltage capability of each element is not addressed. Centralised controller needs to provide a voltage reference for each element.

Each *object* in a layer (i.e. the entities that make up a layer, such as the modules in a bank) is equipped with a controller that acts as a master for that layer, receiving the required sensing signals such as voltages and SoC from the slave controllers located in the next lower hierarchical level. Using this information, a balancing algorithm produces the appropriate voltage references for the slave controllers to follow. This hierarchical scheme enables cell balancing by balancing the intermediate layers using the distributed layer controllers. Crucially, by limiting the total amount of information that is transferred between layers, the requirement for a powerful central controller is avoided, making the system inherently scalable. An example of a hierarchical structure is presented in Fig 1.b. The system controller (including the grid current and power controllers as well as higher level balancing control) acts as a master for the bank controllers and each bank controller is a master to a group of modules. Each module controller is responsible for monitoring a group of *elements* (i.e. objects of the lowest layer) and providing the switching signal for the respective H-bridges. The term 'element' is used here to avoid the confusion with the word 'cell': Cells are the individual electrochemical devices used to store energy whereas an element is the combination of cell and H-bridge. An element may in fact be the series connection of a small number of cells along with a passive or active balancing circuit and an H-bridge, as shown in Fig. 2, as this tends to make better use of the voltage blocking capability of the H-bridge MOSFETs. It should be noted that the top-level controller still provides the overall voltage reference for the entire system (which is produced by the grid current controller) but this is communicated only to the next layer down in the hierarchy from where it is propagated down to the next layer and so on. This propagation must still occur with high time-resolution in order to produce a high quality output waveform, but crucially it is not necessary for the central controller to address every element in the system individually: When a system of N elements is organised in l similarly sized hierarchy layers (i.e. each layer comprises the same number of objects) the total number of slaves that each master must address is reduced from N to $\sqrt[l]{N}$.

In [20], balancing of an intermediate layer is performed by distributing the voltage reference for each object of the layer in proportion to that object's SoC deviation from the average layer SoC. A disadvantage of this method is that once balancing is achieved, the voltage reference is equally distributed to the layers such that multiple H-bridges are switched simultaneously. Effectively, the output voltage generated by this control scheme includes steps that are a multiple of the element voltage and so produces a poorer voltage quality compared with what the CHB circuit is fundamentally capable of producing. Moreover, the balancing controller needs an additional level of control (called the 'peak sharing algorithm' [20]) to ensure that the output voltage can be achieved even when certain modules are not able to meet the demand due to cell failure. The effectiveness of this balancing scheme was only tested in simulation.

This paper follows the hierarchical approach of [20] and presents an alternative hierarchical balancing algorithm that addresses some of the weaknesses of prior work. The proposed algorithm can prioritize balancing according to the maximum SoC variation between the objects of each layer and can ensure that the output voltage reference can always be met so long as there are an adequate number of cells available in the overall system, even for varying module voltages caused by element failures. The ability of this balancing scheme to overcome variations in element capacities and initial SoC is examined by simulating the operation of an AC battery pack comprising 1,000 elements. Finally an experimental validation of the hierarchical balancing is presented using a CHB AC battery pack comprising 144 lithium titanate cells. A summary of the advantages and disadvantages of the proposed hierarchical balancing algorithm compared to existing work that can be found in literature is presented in Table 1.

II. PRINCIPLES OF SOC BALANCING USING A CHB WITH NEAREST LEVEL CONTROL

The modulation technique used in the CHB is based on the nearest level control (NLC) [22]. The principles of the operation of NLC are the same for any number of converter elements. Here a 9-level CHB is used in Fig.2 to explain the basic operation of NLC and how it can be used to perform SoC balancing.

NLC is performed by comparing the actual output of the CHB (V_{CHB}) to the voltage reference (V_{ref}) and switching on the appropriate number of converter elements to achieve a good matching between the two. By doing so, a stepped voltage waveform that follows the sinusoidal reference is produced (Fig.2). Each step of the V_{CHB} waveform is equal to the voltage of the respective element (V_e) that is switched on to produce that step. It can be observed in Fig.2 that due to the operation of the NLC each element is switched on at a different instant in time (different switching angles a_i) and it remains on (i.e. operating states P and N for the H-bridge) for a different amount of time ($2d_i$) during each fundamental period. As a result, each pack is (dis)charged with a different average current I_i :

$$I_i = \frac{1}{\pi}\int_{a_i}^{\pi-a_i} I_o \sin(\theta) d\theta \qquad (1)$$

where I_o is the peak value of the CHB output current I (Fig.2).

This inherent ability of the CHB to (dis)charge each element with a different average current is particularly useful in battery applications as it can be used to perform SoC balancing [17]. The switching sequence of the elements is determined using a priority list L. The priority list includes all the available elements sorted based on their relative SoC in ascending or descending order, with respect to whether the system is discharging or charging. Each element's position i in the priority list corresponds to a specific switching angle a_i and thus a different average position current I_i. The term 'position' used throughout the paper describes the position of the element (or object of a layer) in the respective priority list and is equivalent to the effective duty cycle of that element (or object). In general, a higher position (i.e. a position closer to 1) corresponds to a higher duty cycle and thus higher average position current. In the example of Fig.2, where the pack is charging (CHB voltage V_{CHB} in phase with the pack current I), the element at position 1 is charged with the highest average position current (I_1) whereas the element at position 4 is charged with the lowest average position current (I_4). If M voltage steps are required to produce the output voltage and the number of available elements is N, where $N > M$, the $N - M$ lower positions in the priority list correspond to zero position current (elements occupying these positions remain idle with their respective H-bridges always in the Z state). Redundancy is not necessary in order to achieve balancing with the CHB since each element can be operated under a different current by controlling its position. However, generally a higher value of element redundancy will enhance the balancing capability of the CHB by providing additional flexibility in controlling the effective duty cycle of each element.

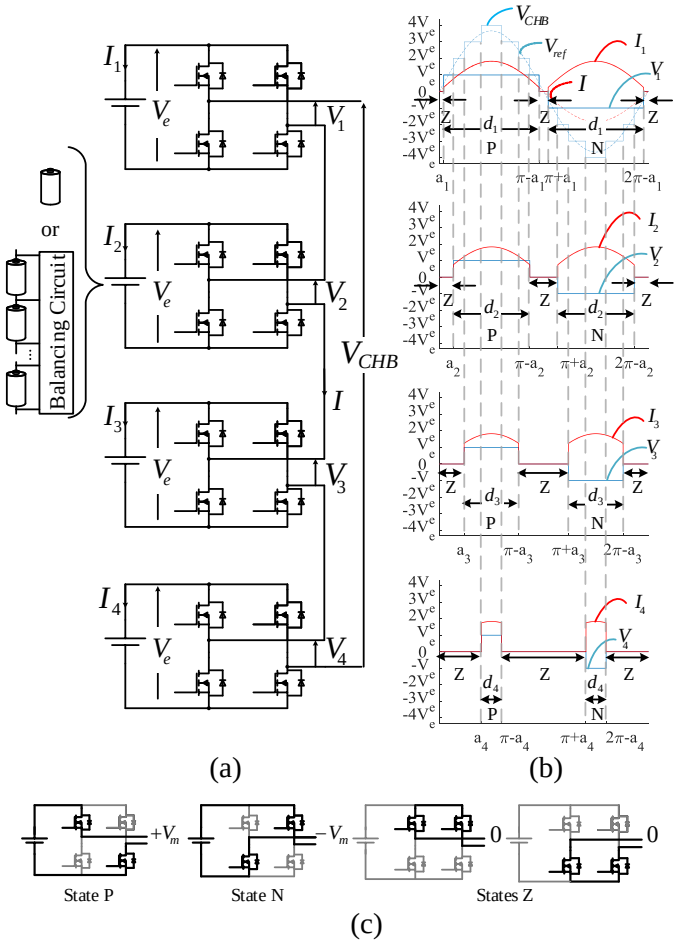


Fig. 2. Demonstration of element balancing using a 9-level CHB.

For a battery pack based on a CHB with a relatively low number of levels and a flat BMS (Fig.1a), balancing can be achieved by using a centralised controller to calculate the SoC of each element, produce the priority list and switch the converter cells accordingly using NLC. In a large scale AC pack based on a hierarchical structure, balancing can also be achieved by controlling the effective duty cycle of the objects of each layer according to their average SoC but over a smaller subset of objects, based on a voltage reference generated for each layer. A detailed description of the hierarchical balancing control is presented in the next section.

III. DESCRIPTION OF THE HIERARCHICAL BALANCING CONTROL

In this paper the hierarchical balancing control is explained using a single-phase CHB AC battery pack with three layers of hierarchy: N_{b} banks (bank layer), where each bank contains N_{m} modules (module layer) and each module contains N_{e} elements (element layer). Although the discussion here is limited to three layers, the control approach can be simply extended to include more layers and be implemented in a three-phase system where balancing between phases is achieved using zero sequence voltage injection [19].

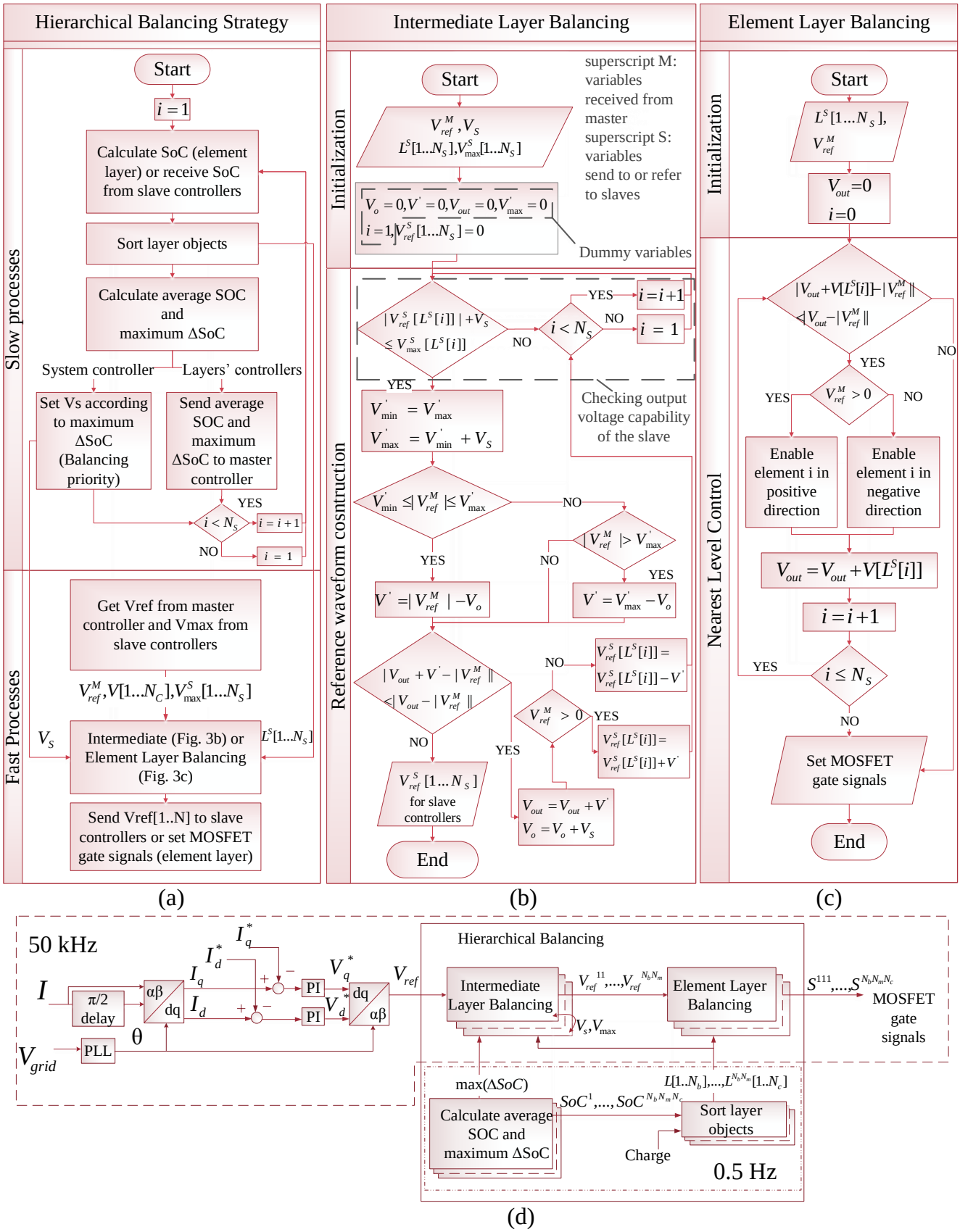


Fig. 3. a) Hierarchical balancing control b) Intermediate layer balancing control c) Element layer balancing control d) Complete control of a single-phase CHB AC battery pack including hierarchical balancing.

The hierarchical balancing control as implemented in the controllers of the different system layers is presented in Fig.3a. The balancing control consists of two parallel processes operating at different rates: a slow process occurring every 2 sec and a fast process occurring at 50 kHz (these frequencies are somewhat arbitrary and will depend on the particular implementation, these values are those used in the experimental work). Due to the different operating frequencies of the two processes, during implementation the appropriate synchronisation signals are used to ensure that the passing of the relevant control variables (i.e. priority lists and V_S) from the slow to the fast processes takes place during the initialisation stages according to Fig.3b and c.

During the slow process, each individual controller receives the average SoC of each object from a group of objects at the next layer down in hierarchy and the maximum SoC variation (ΔSoC) between the objects of the lower hierarchical levels, from the respective slave controllers. Using this information a priority list $\boldsymbol{L^S}$ is produced where the 'slave' objects are sorted based on their average SoC. The average SoC of the current layer and the maximum SoC variation are then calculated and sent to the controller of the next layer up in the hierarchy.

During the fast process, each layer controller receives a voltage reference $V_{\mathrm{ref}}^{\mathrm{M}}$ and a voltage step V_{S} from its master and the maximum output voltage from its slaves ($V_{\mathrm{max}}^{\mathrm{S}}[1 \dots N_{\mathrm{S}}]$) and uses that to calculate the voltage reference that will be sent to the slave controllers ($V_{\mathrm{ref}}^{\mathrm{S}}[1 \dots N_{\mathrm{S}}]$) . The process of deconstructing the voltage reference $V_{\mathrm{ref}}^{\mathrm{M}}$ to produce the slave references $\boldsymbol{V_{\mathrm{ref}}^{\mathrm{S}}}$ is described in Fig.3b and depicted in Fig.4. Each $V_{\mathrm{ref}}^{\mathrm{S}}(i)$ corresponds to a different duty cycle so balancing between layer objects is achieved by assigning a voltage reference at each object based on their position in the respective priority list $\boldsymbol{L^S}$ (i.e. $V_{\mathrm{ref}}^{\mathrm{S}}$ that correspond to higher duty cycles are assigned to the objects with positions closer to 1). The proposed algorithm ensures that the slave reference voltages are constructed in a way so that all available voltage steps are used even when the elements are balanced (in contrast to [20]), by switching the elements on and off at different instances in time and thus avoiding simultaneous switching of the H-bridges. The output voltage capability of the slave objects $\boldsymbol{V_{\mathrm{max}}^{\mathrm{S}}}$ (i.e. the maximum output voltage that the slave can provide) is taken into account during the reference waveform construction and if an object is not able to produce the reference voltage (for example due to an element failure in that module) the next object in the priority list with the ability to satisfy the voltage requirement will be used. It should be noted that the switching frequency of each element's MOSFETs is twice the fundamental frequency of the grid (in this case 100 Hz for a grid frequency of 50 Hz) but the switching events are located with a resolution in time of the reciprocal of the fast process frequency (in this case 20 us).

The waveform of each slave reference voltage $V_{\mathrm{ref}}^{\mathrm{S}}(i)$ is highly dependent on the choice of the voltage step V_{S}. The voltage step should be set equal to the average voltage of the objects in any one particular layer. In this paper the voltage

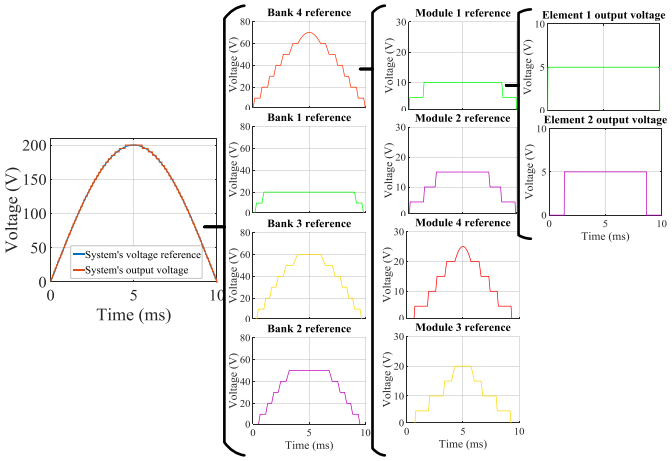


Fig. 4. Demonstration of bank and module layer reference construction from the system reference output voltage. Bank layer reference voltages for $\mathrm{L} = [4\ 1\ 3\ 2], \mathrm{V_{max}} = [20\ 50\ 70\ 70], \mathrm{V_s} = 10$. Module layer reference voltages for $\mathrm{L^4} = [1\ 2\ 4\ 3], \mathrm{V_{max}^4} = [10\ 15\ 25\ 25], \mathrm{V_s} = \mathrm{V_e} = 5$.

step is set equal to either the element voltage V_e, module voltage V_{m} or bank voltage V_{b}. When $V_{\mathrm{S}} = V_{\mathrm{e}}$ the elements of each bank and module are introduced interchangeably in the current path (i.e. element 1 of module 1 of bank 1 is turned on first, then element 1 of module 1 of bank 2 etc.) thus all elements in a module will experience very different duty cycles which will enhance the balancing performance between elements. However the average duty cycles of the higher layer objects (modules and banks) are very similar since the respective slave objects occupy neighbouring steps in the voltage waveform. This is demonstrated using the example of a two layer system in Fig.5. Here, the pack comprises three modules of five elements each. When a voltage step equal to the element voltage V_{c} is used, the elements of module three occupy voltage steps 3,6,9,12 and 15 in the output voltage with the maximum charge difference between the elements depicted in the grey area (the charge difference between elements is directly associated with the ability of the system to perform balancing i.e. the greater the charge difference the wider capacity or SoC differences can be accommodated). When the voltage step is equal to the module voltage all the elements in module 1 are introduced to the current path sequentially (voltage steps 1-5), followed by the elements in module 2 (voltage steps 6-10) and then module 3 (voltage steps 11-15). Here the maximum charge difference between elements is considerably less compared to Fig.5a but this positioning will result to a higher charge difference between the three modules. In general, by setting V_{S} equal to the voltage of a layer's object, balancing priority is given to that layer i.e. the objects of that layer can be operated under very different charges compared to the objects of the other layers. The proposed algorithm is able to prioritise balancing between layers during operation by dynamically setting V_{S} equal to the voltage of the layer where the maximum SoC variation between objects can be found. Balancing priority can be important in some scenarios, for example if the system operator replaces a module after failure, this module may have

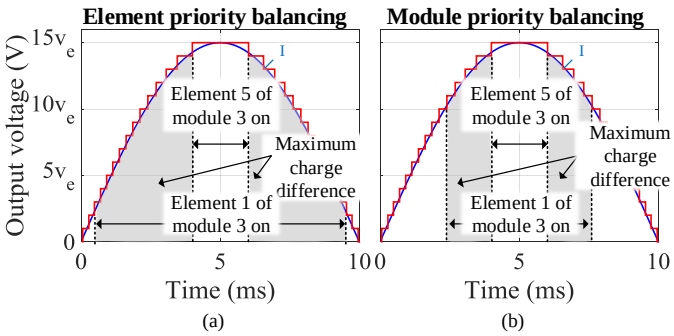


Fig. 5. Maximum charge difference that can be achieved between the elements of a module when a) element priority balancing control is implemented. b) module priority balancing control is implemented.

a very different average SoC compared to other modules but module balancing speed would be limited due to the small variation of average module currents. In a flat system balancing priority is not an issue since any element can be used at any voltage step in the construction of the output voltage so that an optimum charge can be allocated to each element based on their capacity or SoC (i.e. the master controller has a detailed knowledge of the state of every element in the system). This is not the case in the hierarchical control scheme where only limited information is exchanged between layers (i.e. no one controller has detailed knowledge of the state of every element in the system).

The layer balancing control presented in Fig.3b is identical for all hierarchical layers except the element layer. Element layer balancing control is similar to the balancing control of the flat structure [17] discussed above except with the reference voltage provided by the respective master module controller instead the centralised controller (Fig.3c). The complete system control including a single-phase PLL and a dq current controller is presented in Fig. 3d. The output of the current controller is the voltage reference used in the higher level hierarchical controller and the balancing control is performed as described above.

IV. Simulation Results

In order to validate the proposed hierarchical balancing control, the balancing of 1,000 elements during consecutive charging and discharging cycles is simulated in Matlab, assuming 4% redundant elements and $I_{\mathrm{rms}} = 4$ A. The simulated system comprises ten banks, each bank ten modules and each module ten elements. The balancing performance is evaluated for three different cases: 1) when maximum capacity imbalance is observed in the element layer, 2) maximum imbalance in the module layer and 3) maximum imbalance in the bank layer. In all cases, a maximum initial SoC variation of 10% is established between elements and element capacities are normally distributed according to (2).

$$\begin{gathered} Q_{\mathrm{b}} \sim N(\mu, \sigma_{\mathrm{b}}^2) \\ Q_{\mathrm{m}}^{i} \sim N(Q_{\mathrm{b}}(i), \sigma_{\mathrm{m}}^2) \;\; i \in [1, \cdots, N_{\mathrm{b}}] \\ Q_{\mathrm{e}}^{ij} \sim N(Q_{\mathrm{m}}^{i}(j), \sigma_{\mathrm{e}}^2) \;\; i \in [1, \cdots, N_{\mathrm{b}}], j \in [1, \cdots, N_{\mathrm{m}}] \end{gathered} \tag{2}$$

where Q_{b} is the vector of bank capacities, Q_{m}^{i} the vector of module capacities for bank i, Q_{e}^{ij} the vector of element capacities for module j of bank i, μ is the mean of the bank capacity distribution and is equal to 1 Ah. For the other distributions, the mean is equal to the average capacity value of the respective object in the previous hierarchical layer. The variance σ^2 of each layer is equal to 0.06 if this layer has the maximum capacity variation and equal to 0.006 if not (i.e. in the case of maximum capacity variation in element layer, $\sigma_{\mathrm{e}}^2 = 0.06$ and $\sigma_{\mathrm{m}}^2 = \sigma_{\mathrm{b}}^2 = 0.006$).

When any element reaches the upper (95 %) or lower (5%) SoC limit, the cycle ends and the next discharging or charging cycle begins.

The flat system approach is used as the reference case for comparison because it can place any element at any position and thus can provide the best overall balancing performance (i.e. full flexibility in charge redistribution between elements according to their respective capacities). However, a centralised controller is required which would make implementation challenging for large scale systems. The hierarchical balancing approach limits the information exchange between layers but at the cost of reduced flexibility regarding the balancing performance.

The balancing performance of the proposed algorithm is examined for three cases where the dynamic balancing priority between layers is disabled i.e. the system operates with continuous priority in element balancing (V_{s} equal to element voltage), continuous priority in module balancing (V_{s} equal to module voltage) or continuous priority in bank balancing (V_{s} equal to bank voltage for the banks and V_{s} equal to module voltage for the modules). As previously explained, when priority is given in balancing the objects of one layer, the balancing of all other layers is slower.

The results of balancing using the flat system are presented in Fig.6 (system structure, e.g. the bank grouping, is retained here to facilitate comparison between different approaches although the flat system does not require such subdivisions). For all three cases of capacity imbalance, a satisfactory balancing performance is observed (maximum SoC variation between elements <0.5%) and the flat system is able to overcome an initial SoC variation between elements (equal to 10%) after only 5 minutes.

Using the proposed hierarchical balancing algorithm, a balancing performance close to that of the flat system can be achieved with limited information exchange between layers. In that case, the system overcomes the initial SoC variation again at 5 minutes and the SoC variation between all elements is maintained below 0.5 % throughout operation. The importance of prioritising balancing of different layers dynamically according to their respective SoC variation can be observed by comparing the proposed algorithm, where the prioritised layer is chosen dynamically, to the cases where priority is fixed to a specific layer. From all three cases it can be seen that if the layer with the maximum capacity variation happens to be different than the layer which is given balancing priority, then the system is not able to overcome that capacity

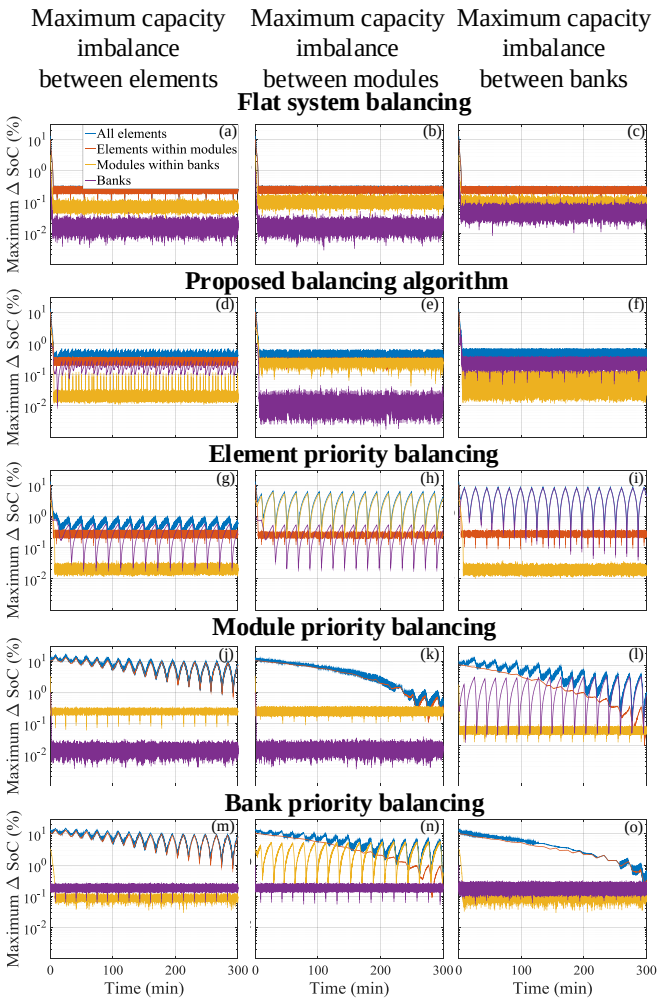


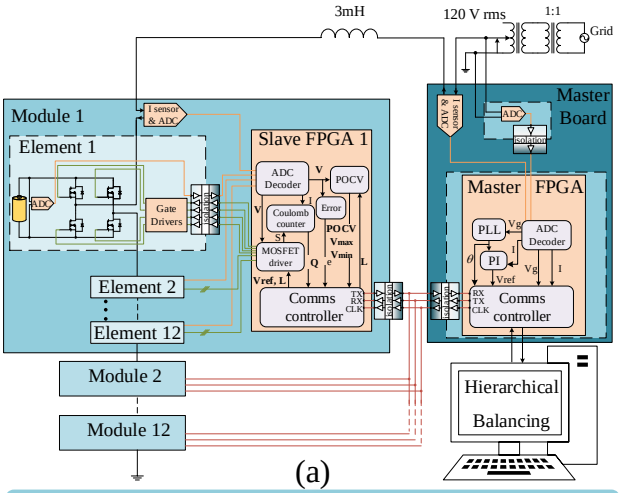
Fig. 6. Balancing using a flat system approach under maximum capacity variation a) at element level b) at module level, c) at bank level. Balancing using the proposed balancing algorithm under maximum capacity variation d) at element level e) at module level, f) at bank level. Element priority balancing under maximum capacity variation g) at element level h) at module level, i) at bank level. Module priority balancing under maximum capacity variation j) at element level j) at module level, l) at bank level. Bank priority balancing under maximum capacity variation m) at element level n) at module level, o) at bank level.

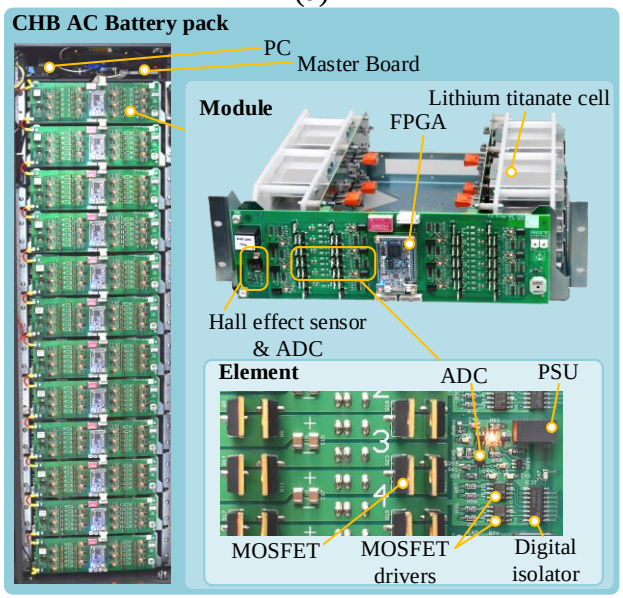
variation resulting in a decreased balancing performance, e.g. in Fig.6i where element balancing is given priority but the maximum capacity variation is observed between banks. The swings in the maximum SoC variation observed here are due to the capacity variations between banks. In steady state, the ΔSoC reaches a peak value due to the limited ability of the algorithm to redistribute charge between the objects of a layer according to their capacities. In the following cycle after the maximum ΔSoC is reached, the objects start at a different initial SoC at which point the objects have very similar available capacities (i.e. the capacity that corresponds to the available SoC range for this cycle) and thus balancing will from then on be more effective resulting to a lower maximum ΔSoC. This process will be repeated resulting in these swings being observed in the maximum SoC variation between objects of different layers, as shown in Fig.6.The deteriorated balancing performance in case of module and bank balancing priority is also evident in the fact that it takes more than 250 min for the system to overcome the initial SoC imbalance between elements (in this case the system is restricted to placing elements in neighbouring positions which have similar average position current and therefore only a very weak balancing effect).

V. Experimental Validation

The experimental CHB AC battery pack comprises 144 lithium titanate cells with a 20 Ah nominal capacity. Each cell is connected to an H-bridge forming an element and the elements are organised in twelve physical groups of twelve elements each, referred to as modules (Fig.7a). Each module is equipped with a PCB including twelve ADCs to measure cell voltages and a current sensor that is used to calculate cell charge by coulomb counting. Cell monitoring and control is performed locally at each module using an FPGA. The element layer balancing control is performed in the FPGA which performs priority list sorting and generates the switching signals for the MOSFET drivers. A daisy-chain communication link connects these twelve slave FPGAs to a master FPGA. The power controller (including single-phase PLL and current dq controller) is implemented on the master FPGA (the system is coupled to the grid using a single inductor that serves as a low pass filter and as an impedance for the current controller to work against). The master FPGA also coordinates communication between the slave FPGAs and a lab PC that runs a MATLAB GUI where the hierarchical balancing control is implemented. The GUI allows the user to set a grid current reference and monitor cell voltages and SoCs which are broadcast by the slave FPGAs and collected by the master FPGA. The hierarchical balancing control is performed in MATLAB and once the reference voltages are produced from the upper layer balancing controller they are sent to the master FPGA that distributes them to the respective slave FPGAs where the element balancing is performed.

In order to demonstrate hierarchical balancing control, the AC battery pack is divided in three virtual layers as follows: three banks including four modules of twelve elements each. During the test, the voltage at the input of the CHB is set at 120 V RMS. The actual output voltage of the CHB depends on the operation (i.e. higher than 120 V when discharging and lower when charging due to the voltage drop across the grid coupling inductor). As a result, the redundancy ratio (the peak number of elements in-circuit divided by the total number of elements in the system) of the CHB varies accordingly during operation due to the varying element voltages: as element voltage increases during charging, less elements are required to synthesise the output voltage and thus an increased balancing performance can be achieved. During this test, the AC battery pack is operated in three consecutive charging (current reference -10 A RMS) and discharging (current reference 10 A RMS) cycles of 1 hour duration each. After the end of the second charging cycle, the elements are left to rest for 30 min in order to accurately measure the OCV.





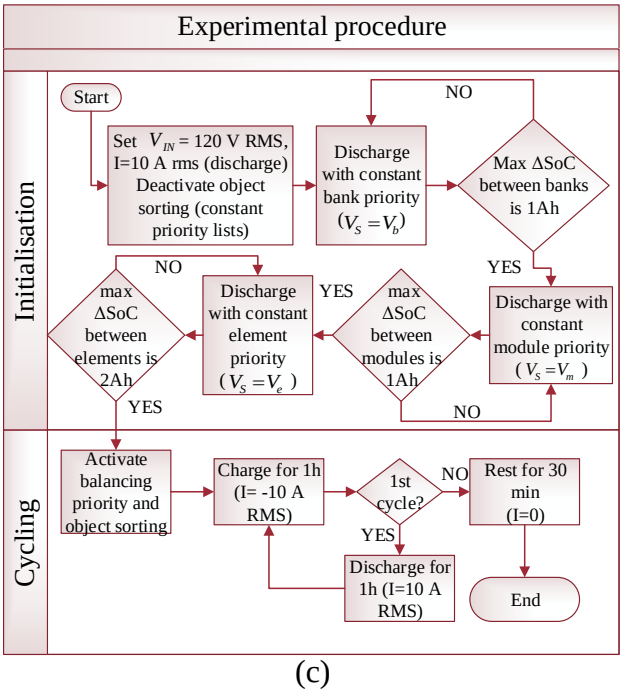


Fig.7 a) The experimental CHB AC battery pack including control blocks b) CHB AC battery pack including twelve modules of twelve elements each c) Flowchart of the experimental process.

To evaluate the balancing performance of the proposed algorithm, before the beginning of the test the elements are unevenly discharged (see initialisation process in Fig.7c) so that a maximum initial SoC variation equal to 7% is introduced between the banks and between the modules of the system. The maximum initial SoC variation between the elements of a module is equal to 10% and the maximum initial SoC variation between all elements of the system is equal to 20% (element 1 of module 1 compared to element 12 of module 12). To evaluate the ability of the system to accommodate elements with different capacities, the cell of element 1 of module 9 is replaced with a cell that has been cycled over 3,000 cycles so that its capacity is decreased by 5% (19 Ah). All the steps followed during the experimental validation (including the initialisation process) are presented in detail in the flowchart of Fig.7c. Here, balancing is performed using pseudo-OCV (POCV) measurements that can be used as an accurate indication of relative SoC difference between elements [17]. In order to obtain a POCV measurement, one cell from each module is bypassed every two seconds. The sorting of elements, modules and banks is thus performed every two seconds after a new POCV measurement is made. The POCV update rate is restricted by the system's communication protocol. For C rates up to 3C however, the SoC variation of an element in 24 seconds is less than 2 %, so this lag in measurement between the first and last elements in a module does not significantly affect balancing performance in this test. The balancing priority is updated every two minutes by calculating the maximum POCV variation between the objects of each layer using the average POCV during this period.

VI. Results and Discussion

The balancing of the objects in the three conceptual layers (i.e. banks, modules and elements) is presented in Fig. 8. In order to smooth the experimental data (POCV and element position) a moving average filter is used, taking the average of 50 samples from the POCV data and 500 samples from the position data. An increased number of samples is required for the position data since element position is updated every 2 s (discrete values ranging from 0-12 for the elements, 0-4 for the modules and 0-3 for the banks) so the average value of the position is required in order to produce a relatively smooth line that enables us to comment on the behaviour of the algorithm. The voltage difference of the POCV measurements between subsequent samples is limited to a few millivolts so a lower number of samples are used in the average filter. The system is able to overcome the initial SoC variation and achieve balancing within the first charging cycle, demonstrating the ability of the system to effectively allocate charge between elements and to overcome a capacity imbalance between objects of a layer.

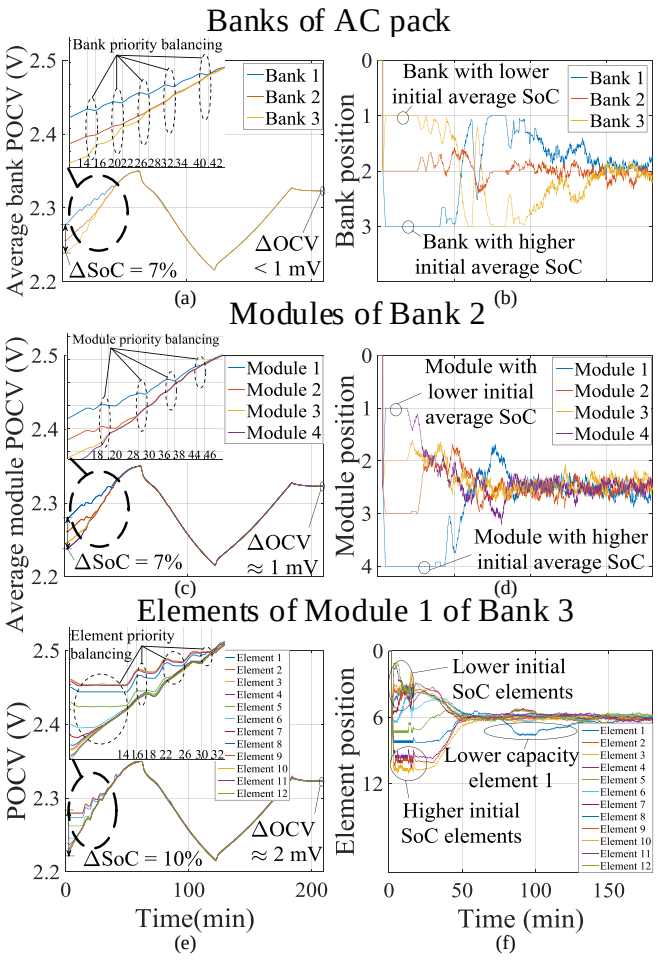


Fig. 8 a) POCV balancing of the banks of the AC pack. b) Average bank position. c) POCV balancing of modules in bank 2. d) Average position of modules in bank 2. e) POCV balancing of elements in module 1 of bank 3. f) Average element position in module 1 of bank 3.

Balancing within the objects of a layer is more noticeable when balancing priority is given to that layer. From Fig.8a it can be seen that the average POCVs of the three banks converge when priority is given to bank balancing (see subplot in Fig. 8a). When priority is given to any other layer, the POCVs of the banks vary with almost the same rate (balancing is slower due to the smaller average current variation between banks). Similar behaviour can be observed in the other two layers as can be seen in the respective subplots in Fig. 8c and Fig. 8e. After balancing is achieved at around 50 mins, balancing priority is given to the element layer in order to overcome the variation in element capacities observed mainly in module 9 (module 1 of bank 3) where the lowest capacity element is located (cell in element 1, 19 Ah compared to 20 Ah nominal capacity).

The position of the objects of each layer in their respective priority list is also presented in Fig.8. Since the system is initially charging, the objects with a higher SoC are placed in positions closer to '1' – this position corresponds to a higher average current compared to higher-numbered positions. After POCV balancing is achieved and since all three banks have essentially equal average capacities, balanced operation is achieved by operating all banks equally as indicated by the close matching of their average position (average bank position close to 2 for all banks) in Fig.8b. Similarly, the modules in bank 2 remain balanced since all of them are operated with an average position close to 2.5. Regarding the elements in bank 3 (Fig.8f) it can be observed that all elements have an average position equal to 6 except element 1 which has a lower average element position (between 7 and 8). Since this is the element including the cell with the lowest capacity, it is operated with a lower effective duty cycle (average current decreases as element position moves from 1 to 12) so that elements will remain balanced. The successful balancing is also highlighted by the close agreement of the OCVs after the end of the test when the cells are left to rest.

The CHB output voltage and current waveforms are presented in Fig.9. Due to the relatively large number of voltage steps (~80) the high frequency distortion of the output voltage (and therefore grid current) is very low. Some odd-numbered low frequency distortion components are visible; these are caused by the distortion of the grid voltage (the grid controller is a dq PI controller operating at the fundamental frequency only). A direct comparison of a variation of the NLC that is used in this paper with an alternative high frequency phase disposition pulse width modulation (PD-PWM) scheme is presented in [23], where the two methods are tested under the same conditions. A 20% lower THD was achieved with the NLC, with the main disadvantage being the dispersed low frequency harmonic content, in contrast to PD-PWM where the harmonic content is concentrated around multiples of the carrier frequency. A key advantage of the NLC is the low switching frequency operation which reduces switching losses.

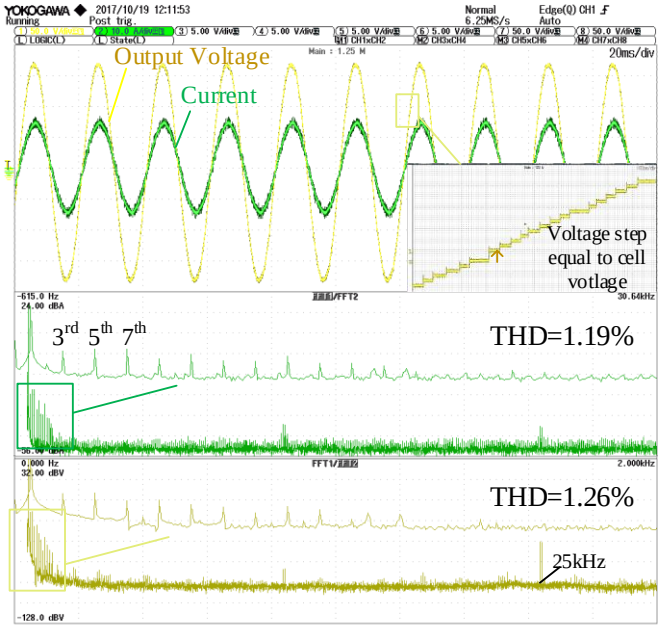


Fig. 9. Output voltage and current of the CHB AC battery pack with FFT of voltage and current waveforms.

VII. Conclusions

This paper presents a decentralized BMS architecture following a hierarchical structure for the control of large scale AC power-electronics enhanced battery packs. Elements are organised in conceptual control layers and the objects of each layer are equipped with a local controller that acts as a master for the controllers of the next lower hierarchical level. Although a high update rate and time resolution is required in order to produce a high quality output voltage, the signal processing and bandwidth requirement of the local controller communication interface is dramatically decreased when compared to the centralised control (flat organisation) approach because the relevant control signals need only be sent to a relatively small number of slave controllers. In this context, a hierarchical balancing algorithm is developed that enables balancing the elements of the battery pack by balancing the objects of the different layers.

The proposed algorithm monitors the maximum SoC variation between the objects of each layer and can dynamically adapt its balancing performance in order to effectively overcome capacity variations within different layers. Another important feature of the proposed algorithm is the ability to fully utilize the available voltage steps of the pack thus increasing output voltage quality whilst also ensuring that the output voltage reference can always be met given that an adequate number of cells are available in the pack. The hierarchical balancing algorithm was validated in simulation for a 1,000 element system (organised in three symmetrical layers of ten objects each) and was successful in retaining SoC variation between all elements below 0.5 % throughout operation, for different cases of element capacity distributions and up to 10% initial SoC variation between elements. The algorithm was experimentally validated using a CHB AC battery pack comprising 144 lithium titanate cells organised into three layers (non-symmetrical layer configuration i.e. three banks, four modules per bank and twelve elements per module). Balancing to within 2 mV of the cell open circuit voltage was achieved between elements with a 20% initial State of Charge variation and 5% capacity difference.

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