Probing the Interface State Densities Near Band Edges from Inductively Coupled Measurements of Sheet Resistance

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Abstract. In this work, we report a new approach to characterise interface state density (D_{it}) near the band edges. Interface defect states are known to trap charge carriers via SRH statistics. At dielectric-silicon interfaces charge in the dielectric layer is neutralised by a layer of mirroring carriers in bulk Si, resulting in an accumulation or inversion layer. Since the interface state density increases exponentially towards the band edge, these states can store large concentrations of charge and alter the carrier concentration at the semiconductor surface. This dramatically influences the operation of devices based on surface carrier manipulation, including field effect passivation, inversion layer pn junctions, and field effect transistors. Unlike capacitive techniques, our method allows a very sensitive detection of the concentration of donor- or acceptor-like states in the unavoidable band-tails. Device simulations show that the conductivity of the charge-induced layer is highly sensitive to D_{it} near the band-tail but is insensitive to D_{it}-midgap. Therefore, the wafer resistance detected by inductively coupled measurements is used as a metric to detect band-tail D_{it}. The wafer resistance is recorded while monitored amounts of surface charges are introduced. The band-tail D_{it} is extracted by fitting the observed resistance dependence to an accurate model of the system. This method allows probing band-tail D_{it} near both the conduction and valence band edge on either n-type or p-type silicon substrates. Since a lifetime tester is used to record wafer resistance, this technique provides an easy and accurate detection of band-tail D_{it}. This technique is highly relevant for analysis of photovoltaic devices since it provides a route to better understand the properties of semiconductor-dielectric interfaces crucial to cell operation.

IMPACT OF INTERFACE STATES ON SPACE CHARGE LAYER RESISTANCE

The interface defect state density (D_{it}) is a key property of Si-dielectric interfaces for Si-based solar cells. The interface states act as recombination centres, however, they are also able to store charged carriers due to their occupancy statistics. According to the Shockley-Read-Hall statistics, the states near midgap are the more effective recombination centres [1, 2]. Their characterisation and passivation are therefore intensively studied [3–5]. However, while the shallow states in the band-tails are inefficient for recombination, their density increases exponentially towards the conduction and valence band edge (CB and VB) [6–13]. Therefore, in the cases of strong band bending where the Fermi level reaches the band-tail, the interface states can store large concentrations of charge carriers, and can hence alter the carrier distribution near the interface significantly, along with the space charge layer. This can influence device performance based on surface carrier manipulation, like inversion layer solar cells, whose emitter is a potential alternative to diffused emitters with inherently reduced Auger losses and lower cost [14], [15]. This mechanism is also strongly used in field-effect surface passivation [16], which is utilised to minimise recombination at the rear of commercial PERC cells [17–19]. In the TOPCon structure, it is demonstrated that heavy doping from the poly-silicon layer can enhance conductivity and reduce recombination at the passivating contact [20], [21]. Recent work has also shown that in TOPCon further field effect passivation can be attained via charge in the tunnelling oxide [22]. In our previous work [23], the Van der Pauw method was used to measure sheet resistance, with the disadvantage

of requiring additional metal contacts, and local doping underneath them when measuring an inversion layer. In this work, we use a Sinton lifetime tester to monitor the conductivity of the space charge layer, with no additional sample processing required, providing a fast and versatile method to characterise both band-tails on either n- or p-type substrates.

Fig. 1 shows a schematic energy diagram of n-Si near the Si-SiO_2 interface in the presence of (a) charged donor and acceptor interface states, and in the presence of (b) positive, and (c) negative dielectric charge. The allowed energies for electrons at the interface decrease when positive dielectric charge is introduced, so that the Fermi level lies closer to the conduction band edge and states at the band-tail acquire a high charge density since acceptor-like interface states below the Fermi level are occupied by electrons. In the presence of negative dielectric charge the inverse process occurs so that the Fermi level lies closer to the valence band edge, allowing the interface to accommodate holes. In the space charge region, charge-induced carriers are partially trapped into the interface, while the others stay in bulk Si and contribute to wafer conductivity. Wafer conductivity can therefore be used as a metric for characterising the distribution of interface states.

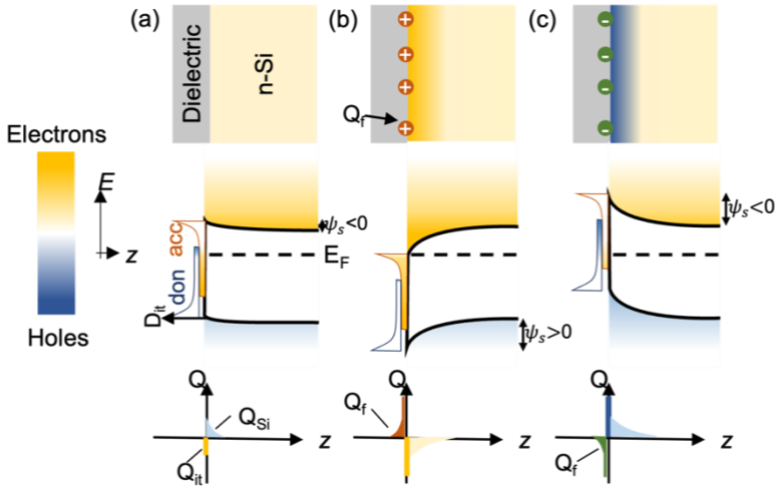


FIGURE 1. Schematic energy diagram at Si-SiO_2 interface (a) in the presence of charged donor and acceptor interface states, in the presence of (b) positive, and (c) negative dielectric charge.

We developed a model in Sentaurus TCAD [24] to better understand the effect of D_{it} on the charge-induced carriers. The model comprises a 200 µm thick, 1 Ω·cm n-Si wafer, with a passivating oxide layer on both sides. Dielectric charge was defined at the front Si-SiO_2 interface. The interface was defined following the same parametrisation in [25], with D_{it} at midgap and band-tails as primary parameters. The Lombardi mobility model was used to account for changes in carrier mobility throughout the sample bulk and in the space charge layer [26], [27]. A density gradient quantum-mechanical model was used to account for the confined carrier distributions occurring near semiconductor–insulator interfaces [28, 29]. The equilibrium state was calculated, and the carrier density and mobility were extracted as a function of the distance from the Si-SiO_2 interface. These were then integrated over the entire sample depth (w) to calculate wafer sheet resistance as $R_{sh} = \left(\int_w qn\mu_n + qp\mu_p dw\right)^{-1}$. Wafer sheet resistance of the model as a function of both positive and negative charge density was simulated with D_{it} varied at both midgap and tail states. The exponential increase in D_{it} towards both band edges is modelled following equations (1) and (2):

$$D_{it}(CB, acc) = D_{it}(max, CB, acc) \times e^{-\frac{(1.12\ eV - E)}{E_{0,CB}}} \quad (1)$$

$$D_{it}(VB, don) = D_{it}(max, VB, don) \times e^{-\frac{E}{E_{0,VB}}} \quad (2)$$

where D_{it} (CB, acc) and D_{it} (VB, don) describe the acceptor/donor band-tail interface state density. D_{it} (max, CB, acc) and D_{it} (max, VB, don) are the maximum interface state density at conduction/valence band edge, and E is the energy of the states from valence band edge in eV. $E_{0,CB}$ and $E_{0,VB}$ represent the slope of the tail, indicating its dependence on energy. Here $E_{0,CB}$ is set to 0.028 eV and $E_{0,VB}$ to 0.024 eV to reflect average values extracted from previous works [6, 7, 10, 12, 13, 30]. Since the band-tail states originate from termination of the periodicity of the bulk silicon, and that the energy slope has been demonstrated to be a function of overall bulk defect density [31], the D_{it} profile at the band-tails reflects the level of disorder in the bulk near the interface. Therefore, for single crystalline silicon substrates

with passivating dielectric layers at similar level of disorder, we assumed $E_{0,CB}$ and $E_{0,VB}$ to be constant. Since the energy slope may vary with different bulk defect density, we calculate N_{it} (acc/don) as the integration of the interface state density provided for each band-tail, which is defined following equation (3):

$$N_{it}(acc/don) = \int_{E_C}^{E_V} D_{it}(acc/don)dE \quad (3)$$

N_{it} (acc/don) is controlled by the maximum state occupation the tail can take. We then use N_{it} (acc/don) as the primary metric for characterising the impact of the tail state concentrations. In Fig. 2a and Fig. 2b, D_{it} (max, CB, acc) was set to 4.2×10^{14} $eV^{-1}cm^{-2}$ and D_{it} (max, VB, don) to 2.3×10^{14} $eV^{-1}cm^{-2}$ [32], while D_{it}-midgap was varied and sample sheet resistance plotted as calculated from our model. In the case of both positive and negative dielectric charge, it is evident that D_{it}-midgap has a minor effect on R_{sh}, as long as D_{it}-midgap is below 10^{12} $eV^{-1}cm^{-2}$, which is the case for most passivated interfaces. However, in Fig. 2c and Fig. 2d, where D_{it}-midgap was set to 10^{11} $eV^{-1}cm^{-2}$ and N_{it} (acc/don) is varied, large changes are observed in both R_{sh} and its dependence on surface charge density. The relationship between wafer sheet resistance and charge density measurement can therefore be used for determining N_{it} (acc/don).

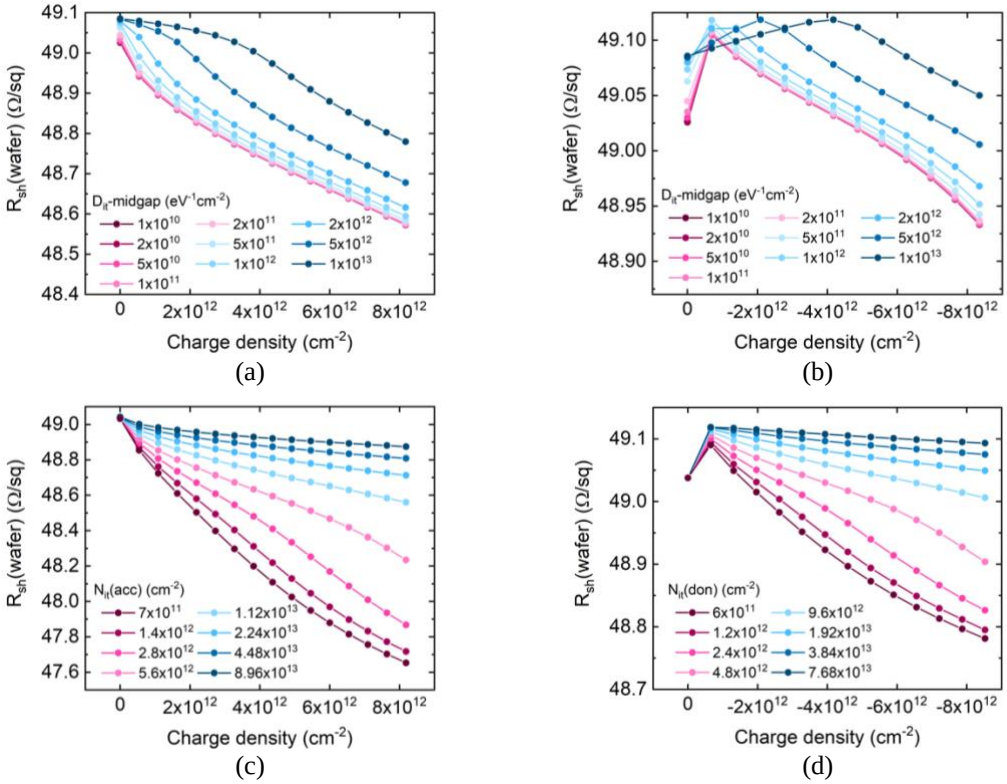


FIGURE 2. Simulated wafer sheet resistance as a function of the fixed charge density defined in the SiO_2 film, deposited on top of a 200 µm thick, 1 Ω·cm n-Si at various (a), (b), D_{it}-midgap (c) N_{it} (acc), and (d) N_{it} (don).

The reliability of this method is evaluated by calculating the reduction in wafer sheet resistance at a charge density of 8×10^{12} cm^{-2} as opposed to when no charge is applied, which reflects the proportion of charge-induced electrons that contribute to conductivity in the entire silicon sample. Fig. 3 shows the results simulated from a 200 µm thick, 1 Ω·cm n-Si substrate, with D_{it} (midgap) set to 10^{11} $eV^{-1}cm^{-2}$ and N_{it} (donor) set to 3.54×10^{12} cm^{-2}. Fig. 3a shows the reduction in R_{sh} as a function of N_{it} (acc). Here it is clear that a large change occurs in the range from N_{it} (acc) = 10^{12} to 4×10^{13} cm^{-2}, indicating that this method is most sensitive to N_{it} (acc) within the range. For N_{it} (acc) below 10^{12} cm^{-2}, the amount of interface states to accommodate the induced electrons is too low to be differentiated in this method. For N_{it} (acc) above 4×10^{13} cm^{-2}, the proportion of charge-induced carriers that stay in the bulk silicon is too small to cause a significant reduction in wafer sheet resistance. This method is therefore less reliable for N_{it} (acc) out of the 10^{12} to 4×10^{13} cm^{-2} range. Wafer resistivity is also varied to show its effect on the reliability. Fig. 3a shows that a

change of wafer resistivity by 0.04 Ω·cm will cause an evident shift of the curve, especially at the region with low N_{it} (acc), meaning that the accurate extraction of N_{it} (acc) depends strongly on the accuracy of the wafer resistivity. Since the non-uniformity in wafer resistivity is unavoidable, the simulated and experimental R_{sh}-Q relations require fitting in y-axis for correct base resistance, and subsequent extraction of N_{it} (acc). D_{it} (midgap) is varied in Fig. 3b where it has a minor effect on the curve. According to this analysis, N_{it} (acc) can be determined with this method with no evident artifacts originating from wafer resistivity variations, or variation in D_{it} (midgap).

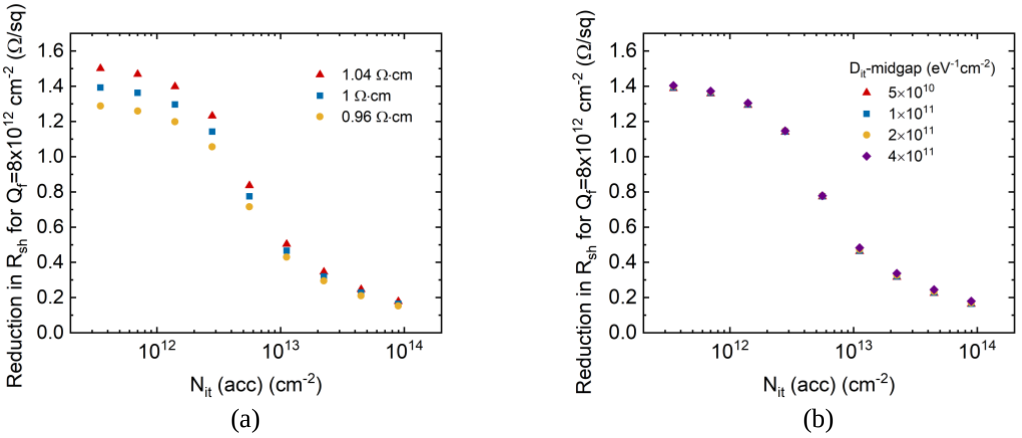


FIGURE 3. Reduction in simulated wafer sheet resistance at a charge density of 8 × 10^{12} cm^{-2} as a function of N_{it} (acc) of a 200 µm thick, 1 Ω·cm n-Si substrate with variation in (a) wafer resistivity, and (b) D_{it} (midgap).

One additional point to note in the simulations is the choice of mobility model. The mobility model has a large impact on the quality of the fitting, and therefore the accuracy of N_{it} extracted. Fig. 4 includes the carrier mobility profiles within 0.1 µm from the Si-SiO_2 interface in the presence of 10^{13} cm^{-2} of positive dielectric charge simulated with various mobility models. PhuMob considers phonon scattering, impurity scattering, and carrier-carrier scattering [33]. Using PhuMob as a basis, the IALMob [26, 34] and Lombardi [26], [27] models include the effect of acoustic surface phonons and surface roughness. However, the two models show significant difference in mobility near the interface. The 'Interface Charge' model also includes the effect of Coulomb scattering by interfacial charge, which abruptly reduces the mobility to ~0 within 0.025 µm from the interface. In the process of fitting simulated curve with experimental data, no fitting was possible using IALMob and the Interface Charge model. IALMob model has been mainly tested in MOSFETs that use base dopant density of the order of >10^{16} cm^{-3} with completely self-contained parameters, while a typical dopant density in this work is 5 × 10^{15} cm^{-3}. The interface charge model appears to underestimate the mobility near the interface and lead to unrealistic R_{sh}-charge density curves. Therefore, in this work, Lombardi model was used in all simulations. It is noted however that improvements in the reliability and quantitative prediction of this method would require a revision of the mobility models used to describe accumulation and inversion layers for dopant densities specific to silicon solar cells.

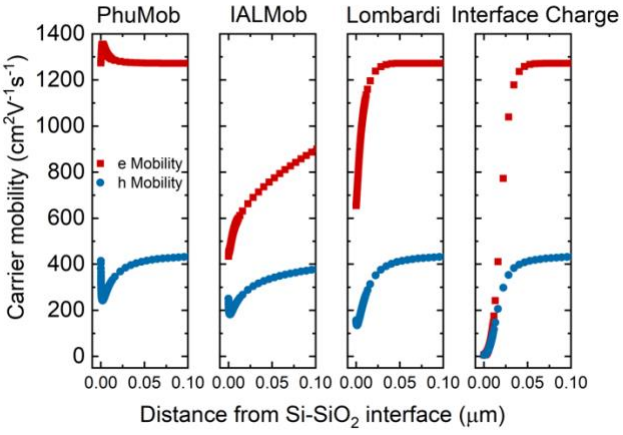


FIGURE 4. Simulated carrier mobility profile near Si-SiO_2 interface in various mobility models.

PROBING INTERFACE STATE DENSITY PROFILE NEAR BAND EDGES

In order to experimentally record changes in R_{sh} as a function of surface charge density, we apply corona discharge in both polarities to the surface of an n-type, and a p-type Si wafer with a SiO_2 dielectric layer on both sides. This generates an electric field and induces an accumulation layer, or an inversion layer, in the silicon near the interface, as illustrated in Fig. 1. Here we use 200 µm thick, 1 Ω·cm n-type/p-type FZ silicon wafers with 100 nm thermal oxide on both sides grown at Fraunhofer ISE. The sheet resistance of the wafer was monitored using a Sinton lifetime tester. The amount of corona ions deposited as a function of corona discharge time was calibrated by Kelvin Probe measurements. The recorded wafer sheet resistance is shown in the dotted symbols in Fig. 5. The uniformity of corona charge deposited was tested in our previous work [35] by constructing a 3 × 3 cm^2 map of surface potential using Kelvin Probe measurements, showing a standard deviation of 3.5% in charge density. An error bar is included in charge density in Fig. 5. The effect of temperature variation on sheet resistance measurements is primarily attributed to the dependence of carrier mobility on temperature. According to PV Lighthouse, at room temperature, the resistivity of a phosphorus doped n-type c-Si at a doping level of 5×10^{15} cm^{-3} can vary by 0.6 to 1.3% by a variation in temperature of 1 to 2 °C, respectively. This demonstrates the importance in precisely controlling the temperature. In this work, the measurements were taken at room temperature (20-24 °C) on a Sinton lifetime tester with standard temperature heated stage controlled to 30 °C. In order to test the accuracy of the sheet resistance measurements in this work, Fig. 6 displays the sheet resistance measured 25 times upon deposition of corona ions for up to 160 s in both polarities, corresponding to charge densities ranging from -1.1×10^{13} to 8.7×10^{12} cm^{-2}. Each data point was taken after a re-positioning of the sample to take into account the error introduced by sample handling. Each group of 25 points were taken within a total of 10-15 min. During the resistivity measurements, the light was blocked to eliminate the error introduced by injection of carriers. The standard deviation was calculated from the last 20 points to eliminate the transient effects that arise from the application of an eddy current to the sample causing a change in defect occupation [14]. This resulted in an error of 0.02-0.05% to the value of sheet resistance characterised. An error bar of 0.05% is thus included in the wafer sheet resistance in Fig. 5. The calculated error is one order of magnitude smaller than the error introduced by 1 °C temperature variation, which implies a minor temperature variation during the measurements. However, the mismatch between the actual sample temperature and the temperature set in the model (25 °C) can cause a shift in y-axis in Fig. 5. Despite the temperature mismatch, the effect of formation of an accumulation or inversion layer on the change in sheet resistance is more pronounced than that given by the temperature variations. To compensate the mismatch, a precise control and monitoring of the sample temperature will be included in future work.

In the numerical model, wafer resistivity and N_{it} were varied so that the simulated curves (solid lines in Fig. 5) fit the experimental data. D_{it}-midgap of the n-type wafer was obtained by an analytical fitting of effective lifetime of the sample as a function of surface potential. Fig. 7a shows the sample structure. A transparent PEDOT:PSS gate electrode was applied on both surfaces to monitor the surface potential, while effective lifetime of the sample was recorded as a function of surface potential using the lifetime tester. Fig. 7b shows the analytical fitting, which gives the D_{it}-midgap of 2.8×10^{10} $eV^{-1}cm^{-2}$. A detailed description of this method can be found in [36]. Since D_{it}-midgap has been shown to have a minor effect on R_{sh}, the value was used in simulations for all specimens. The extracted N_{it} for the n-type specimen is 2.94×10^{12} cm^{-2} near CB and 1.2×10^{12} cm^{-2} near VB. The extracted N_{it} for the p-type specimen is 2.24×10^{12} cm^{-2} near CB and 1.2×10^{12} cm^{-2} near VB. The extracted D_{it} profile is shown in Fig. 5e for the n-type and Fig. 5f for the p-type specimen. The base resistivity values quoted in the figure are chosen for the fits in the model. The interface parameters used for the fits are summarised in Table 1. No significant difference is observed in N_{it} near both band edges between the two specimen types. Another point to note is that for both specimens, N_{it} (acc) is larger than N_{it} (don). The dashed lines are simulated as reference of the accuracy of the method, including curves with $\pm 8.4 \times 10^{11}$ cm^{-2} in N_{it} for N_{it} (acc) and $\pm 7.2 \times 10^{11}$ cm^{-2} for N_{it} (don). Such deviation in N_{it} represents an increase in mean squared error of the fits between1.2 to 2.1-fold, suggesting that the quoted values of N_{it} simulated in the solid lines are of sufficient accuracy.

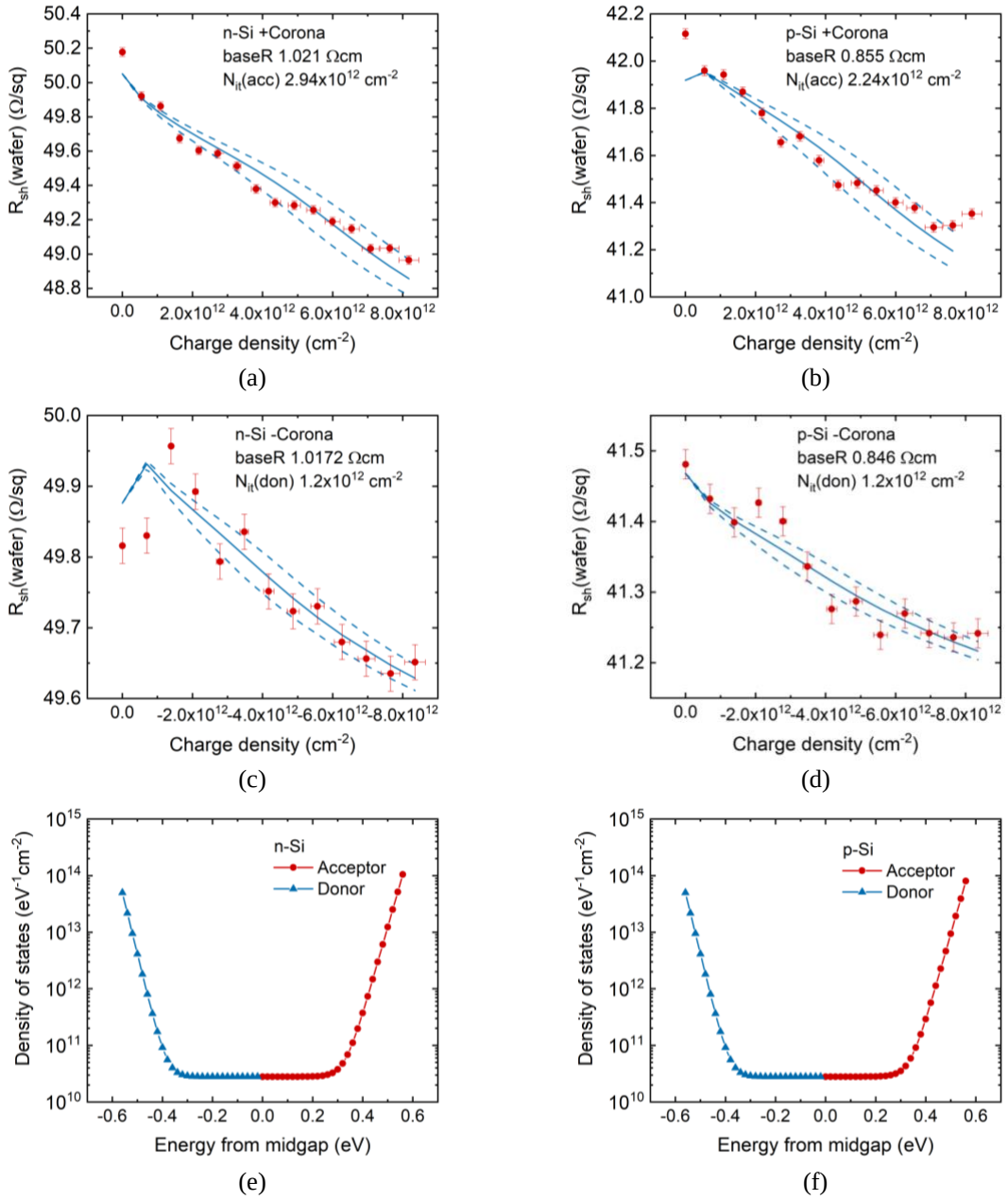
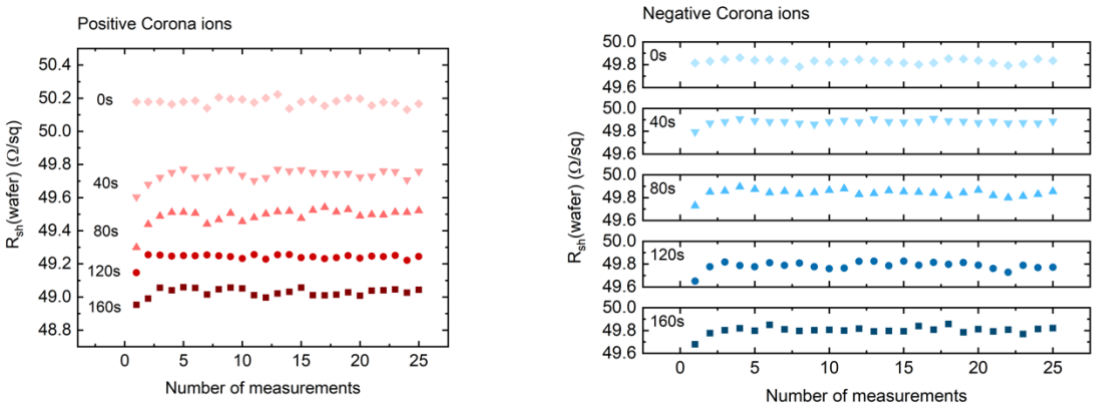


FIGURE 5. Simulated (lines) and experimental (symbols) curves of wafer sheet resistance as a function of corona charge density of an (a), (c) n-type, and a (b), (d), p-type Si wafer. Extracted D_{it} profile across Si bandgap of the (e) n-type, and (f) p-type Si wafer by simulation. The error bars represent the standard deviation of the measurement as displayed in Fig. 6.

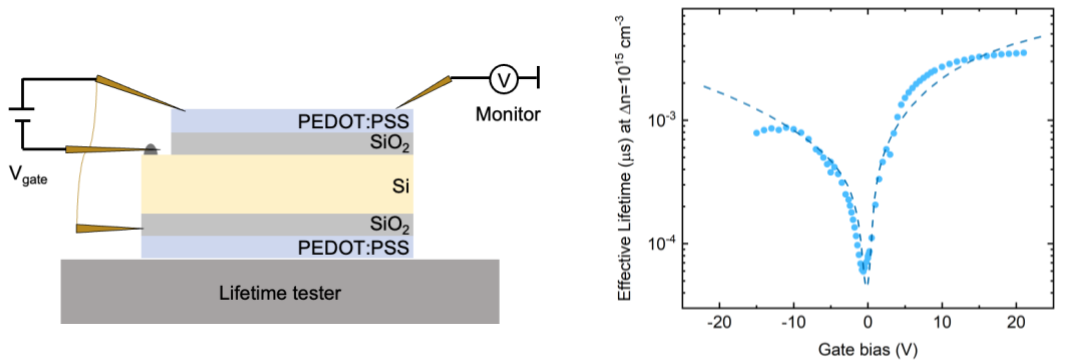


(a) (b)

FIGURE 6. Sheet resistance of an n-type specimen measured multiple times upon deposition of corona ions for up to 160 s in both polarities.

TABLE 1. Details of parameters used in simulations for best fits with the experimental wafer sheet resistance vs. charge density curves.

		Base Resistivity (Ω·cm)	**N_{it} (acc) (cm^{-2})**	**N_{it} (don) (cm^{-2})**	**Mean Squared Error**
n-Si	Fig. 5a	1.021	2.94×10^{12}		6.7×10^{-3}
n-Si	Fig. 5c	1.0172		1.2×10^{12}	1.6×10^{-3}
p-Si	Fig. 5b	0.855	2.24×10^{12}		8.5×10^{-3}
p-Si	Fig. 5d	0.846		1.2×10^{12}	6×10^{-4}



(a) (b)

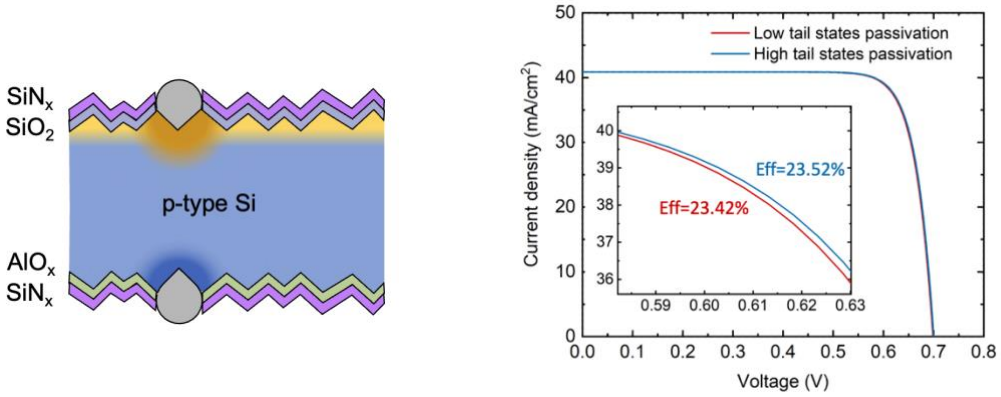
FIGURE 7. (a) Schematic diagram of experimental setup to obtain effective lifetime of a sample as a function of surface potential. **(b)** Experimental data (dotted line) and its analytical fitting (dashed line) of effective lifetime of a 200 μm thick, 1 Ω·cm n-type FZ silicon substrate as a function of gate bias.

Fig. 8 shows an example of the benefit of passivating band-tail interface states in PERC cells. Fig. 8a shows the schematic of a model of a PERC cell developed in Sentaurus TCAD. The relevant parameters of the cell are listed in Table 2. The resistance in the grid is not considered. An equal density of 5×10^{12} cm^{-2} of positive/negative charge was defined at the front/rear surface of the cell for field effect passivation. The simulated IV curves are plotted in Fig. 8b. D_{it} at the band-tails was set to 10^2 lower for the blue curve to demonstrate the effect of passivating the tail states, giving an increase in efficiency by 0.1% absolute. With the characterization method introduced in this work, band-tail interface states can be monitored and used to point to ways for improvement of interface passivation of a PERC cell. The method can also benefit the optimisation of other devices where surface carrier concentration plays an important

role, for example, conductivity of the charge-induced emitter in inversion layer cells [14], and the performance gain by forming an accumulation layer in a TOPCon structure [22].

TABLE 2. Parameters used in the simulations of PERC cells.

Parameter	Value
Cell thickness	170 μm
Bulk base resistivity	p-type, 2 Ω·cm
SRH bulk lifetime	τ_n = 2 ms, τ_p = 20 ms
Finger width	25 μm
Finger spacing	1.4 mm
D_{it}-midgap	10^{11} $eV^{-1}cm^{-2}$
D_{it} (max) at band-tail	CB/VB: $5/2 \times 10^{15}$ $eV^{-1}cm^{-2}$
D_{it} (max) at band-tail (Improved passivation)	CB/VB: $5/2 \times 10^{13}$ $eV^{-1}cm^{-2}$
Grid resistance	0 Ω
Contact resistance (front)	2×10^{-3} Ω·cm^2
Contact resistance (rear)	5×10^{-3} Ω·cm^2



(a) (b)

FIGURE 8. (a) Schematic of a model of a PERC cell. (b) Simulated IV curves of PERC cells with 5×10^{12} cm^{-2} of positive/negative charge defined at the front/rear surface for field effect passivation at different levels of interface state density at the band-tails.

SUMMARY

In this work, we developed an easy and accurate technique to characterise the interface state density profile at a semiconductor-dielectric interface near both band edges. We observed that conductivity of a space charge layer is sensitive to D_{it} near band-tail but is insensitive to D_{it}-midgap by device simulations. We then used wafer resistance as a metric to characterise band-tail D_{it}. The sensitive detection of band-tail D_{it} offered by this approach complements existing interface characterisation techniques to provide a more detailed analysis of the interface. This could lead to a deeper insight into the interfacial properties of a wide variety of optoelectronic devices, especially in techniques where manipulating surface carrier concentration is the key. This includes the use of field effect passivation in PERC, the enhancement of conductivity and passivation in TOPCon, and the formation of an induced emitter in inversion layer cells.

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DATA AVAILABILITY

All data created during this research and published in this article is openly available from the Oxford University Research Archive and can be downloaded free of charge from http://ora.ox.ac.uk.

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