Performance of a Cryogenically Cooled GaN Inverter

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Abstract

This thesis details the development of a cryogenic GaN inverter. It encompasses transistor-level characterisation, inverter system modelling, and finally the design and testing of a GaN three-phase bridge operating at 77 K (−196 °C). This work is motivated by the need for highly efficient and power-dense motor drives for electric aircraft fuelled with liquid hydrogen.

At cryogenic temperatures, there is an eight times reduction in the $R_{\mathrm{ds(on)}}$ of GaN transistors. In principle, this could be exploited to build highly efficient motor drives with a higher power rating than an equivalent operating at conventional temperatures. The extreme operating conditions introduces the possibility of unexpected failure modes which may limit the performance of an inverter, which negate the benifits of cryogenic operation.

The primary research question is therefore: "*Are cryogenically cooled GaN inverters suitable for aircraft applications?*"

To answer this question, a 650 V GaN HEMT failure modes and loss mechanisms are examined at cryogenic temperatures. First, high currents in excess of the rated current, are used to determine its $R_{\mathrm{ds(on)}}$ characteristics, and to test its functionality and performance when subjected to large thermal loads. The switching behaviour is tested using a double pulse test. The switching energies at cryogenic temperatures are measured to decrease by 27 % at 200 K (−73 °C). A simple adaptation to the driver circuit, using −6 V $V_{\mathrm{gs(off)}}$, is found to prevent $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ induced shoot-through that occurred at cryogenic temperatures.

Second, a cryogenic GaN inverter is modelled and used simulate an electric aircraft take-off drive cycle. From this it is concluded that if thermally limited, a cryogenic inverter with the same device type and die area is capable of delivering 6.8 times more power than when cooled using non-cryogenic conventional cooling.

Finally, a 400 V cryogenic GaN inverter is designed and tested up to 11 kVA output, achieving a peak efficiency of 99.79 %, demonstrating operation at power an order of magnitude higher than any cryogenic GaN converter published to date in the literature. The cause of failure at higher powers is found to be interaction between the parasitic source inductance and the increased $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ at cryogenic temperatures. Reducing the gate drive impedance was found to reduce oscillatory behaviour at the turn on switching instance, this allowed higher test power to be achieved.

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Acronyms

2DEG	2-Dimensional Electron Gas
2L	Two Level
ABS	Acrylonitrile Butadiene Styrene
AC	Alternating Current
AlGaN	Aluminium Gallium Nitride
ANPC	Active Neutral Point Clamped
B2B	Board-To-Board
CAD	Computer Aided Design
CHF	Critical Heat Flux
COTS	Common Off The Shelf Parts
CSI	Current-Source Inverter
CT	Cryogenic Temperature
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DMM	Digital Multi-meter
DPT	Double Pulse Test
DUT	Device Under Test
EMI	Electro-Magnetic Interference
ESR	Equivalent Series Resistance

FCML	Flying Capacitor Multilevel Level
FDM	Fused Deposition Modelling
FET	Field Effect Transistor
FOM	Figure of Merit
GaN	Gallium-Nitride
HEMT	High Electron Mobility Transistor
HFC	Hydrogen Fuel Cell
HS	High Side
HTS	High Temperature Superconducting
HX	Heat Exchanger
IC	Integrated Circuit
ID	Inside Diameter
IDC	Insulation-Displacement Connector
In	Indium
LH2	Liquid Hydrogen
LN2	Liquid Nitrogen
LS	Low Side
LVDT	Linear Variable Differential Transformer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OD	Outside Diameter
Pb	Lead
PCB	Printed Circuit Board
PET	Polyethylene Terephthalate
PETG	Polyethylene Terephthalate Glycol

PWM	Pulse Width Modulated
RL	Resistor-Inductor
RMS	Root Mean Square
RMSE	Root Mean Squared Error
RT	Room Temperature
RTV	Room Temperature Vulcanising
SAC	Tin-Silver-Copper
SBD	Schottky Barrier Diodes
SCCL	Switched Current Commutation Loop
Si	Silicon
SiC	Silicon-Carbide
Sn	Tin
SPWM	Sinusoidal Pulse Width Modulated
SSCB	Solid-state Circuit Breaker
THI	Third Harmonic Injection
TIM	Thermal Interface Material
ToF	Time of Flight
UWBG	Ultra Wide-bandgap
VSI	Voltage-Source Inverter
WBG	Wide-bandgap

Nomenclature

Electrical Symbols

$\cos\phi$	Power factor
η	Efficiency
η_{c}	Efficiency measured using a calorimetric measurement
η_{e}	Efficiency measured using electrical measurements
η_{HHV}	Higher heating value efficiency of the hydrogen fuel cell
RRR	Residual-Resistance Ratio
C_{gd}	Miller capacitance or gate-drain capacitance (F)
$C_{\mathrm{o(er)}}$	Effective energy related output capacitance (F)
C_{oss}	Output capacitance of a MOSFET (F)
E_{sw}	Switching Energy (J)
f_{e}	Electrical frequency (Hz)
f_{sw}	Switching frequency (Hz)
g_{m}	Transconductance (S)
L_{s}	Parasitic source inductance (H)
M	Modulation Index
n_{p}	Number of transistors in parallel per switch
Q_{rr}	Reverse recovery charge (C)
$R_{\mathrm{ds(on)}}$	On-state resistance of a transistor (Ω)

R_{g} Gate Resistance (Ω)

$R_{\mathrm{on,sp}}$ Specific on-state resistance (Ω)

S Apparent Power (kVA)

t_{f} Fall time (s)

t_{r} Rise time (s)

T_{sat} Saturation temperature of the fluid (°C)

V_{BD} Breakdown Voltage (V)

V_{bus} Bus Voltage (V)

V_{th} Threshold Voltage (V)

Thermofluid Symbols

α_{f} Bubble contact angle (°)

χ Vapour quality

Δh_{fg} Specific latent heat of vaporisation ($\mathrm{J\,kg^{-1}}$)

$\Delta\chi_{\mathrm{tank}}$ Change in vapour quality of the fuel flow that occurs in the tank

$\Delta\rho$ Change in density between the liquid and the vapour phase ($\mathrm{kg\,m^{-3}}$)

$\dot{m_{\mathrm{HFC}}}$ Mass flow rate required by the HFC ($\mathrm{kg\,s^{-1}}$)

$\dot{m}$ Mass flow rate ($\mathrm{kg\,s^{-1}}$)

γ Surface tension ($\mathrm{N\,m^{-1}}$)

μ Dynamic viscosity (Pa s)

$\boldsymbol{Nu}$ Nusselt Number

$\boldsymbol{Pr}$ Prandtl Number

$\boldsymbol{Re}$ Reynolds Number

A_{c} Cross-sectional Area ($\mathrm{m^2}$)

C_{P} Specific heat at constant pressure ($\mathrm{J\,kg^{-1}\,K^{-1}}$)

h Heat transfer coefficient ($\mathrm{W\,m^{-2}\,K^{-1}}$)

h_{in} Specific enthalpy at the propulsion system inlet ($\mathrm{J\,kg^{-1}}$)

h_{out} Specific enthalpy at the propulsion system outlet ($\mathrm{J\,kg^{-1}}$)

q''_{w} Heat flux at the wall ($\mathrm{W\,m^{-2}}$)

Q Rate of heat transfer (W)

q Specific heat transfer ($\mathrm{J\,kg^{-1}}$)

Q_{con} Conduction losses (W)

Q_{hl} Rate of heat transfer from the ambient air to the cryogenic system, heat-leak (W)

Q_{P} Propulsion system losses (W)

R^* Critical bubble radius (m)

T_{sat} Saturation temperature (K)

T_{w} Wall temperature (K)

w Shaft work ($\mathrm{J\,kg^{-1}}$)

Thermal Symbols

k Thermal Conductivity ($\mathrm{W\,m^{-1}\,K^{-1}}$)

$R_{\mathrm{c-a}}$ Casing to Ambient Thermal Resistance ($\mathrm{K\,W^{-1}}$)

$R_{\mathrm{j-c}}$ Junction to Casing Thermal Resistance ($\mathrm{K\,W^{-1}}$)

R_{th} Thermal Resistance ($\mathrm{K\,W^{-1}}$)

Other symbols

c Convergence criteria threshold

Electrical Subscripts

25 °C The value at 25 °C

cu Copper

DC	Direct-current
ds	Drain to Source
dt	Deadtime
d	Drain
est	Estimated
fail	The value at failure
gd	Gate to Drain
gs	Gate to Source
g	Gate
HFC	Hydrogen Fuel Cell
j	Transistor Junction
ll	Line-to-line
lower	Lower transistor in a half-bridge
max	The maximum value, often in the context of rated maximum
off	Value at the turn-off edge
on	Value at the turn-on edge
ph	Phase of the three-phase bridge
p	Parasitic
RMS	Root-mean-square
s	Source
tot	Total
upper	Upper transistor in a half-bridge
k	Index of switching instance
p	Index for the three phases, $p \in \{A, B, C\}$

Thermal and Thermofluid Subscripts

a	Ambient
b	Base
CHF	Critial Heatflux
dis	Disipated
fin	Fin
f	Denotes that the property is for the liquid state
gen	Generated
g	Denotes that the property is for the gaseous state
HS	Heat sink
init	Initial value
ins	Insulation
TIM	Thermal Interface Material
wet	Wetted surface
w	At the wall

Chapter 1

Introduction

1.1 Motivation

The aviation sector is expected to use liquid hydrogen to fuel carbon-neutral aircraft, with demonstration aircraft expected to fly in the middle of the next decade. In the near term, the majority of long-haul aircraft are likely to be fuelled with sustainable aviation fuels, with properties similar to current aviation fuel i.e. liquid under normal conditions. However, in the long term (2060 and beyond), hydrogen-fuelled aircraft may become dominant as technology develops [1], [2].

Hydrogen can be used to generate electrical power via a hydrogen fuel cell (HFC) or burnt in a gas turbine to generate mechanical work directly. In both cases, it is beneficial for the hydrogen to be evaporated and heated before being consumed in either system. This creates an opportunity for the liquid hydrogen fuel to be used for cooling purposes [3], [4], [5].

It can be seen in Fig. 1.1 that significant reductions in both copper resistance and the gallium-nitride (GaN) transistor on-state resistance are attained at cryogenic temperatures. This may lead to greatly reduced conduction losses in a motor drive, increasing its efficiency.

The use of GaN transistors at cryogenic temperatures in the context of motor drive inverters is therefore the subject of investigation in this thesis.

1.2 Cryogenic Cooling

1.2.1 Properties of Cryogens

A cryogenic fluid (or *cryogen*) is generally defined as a liquid with a very low boiling point. The first component of air that undergoes a phase change at reduced

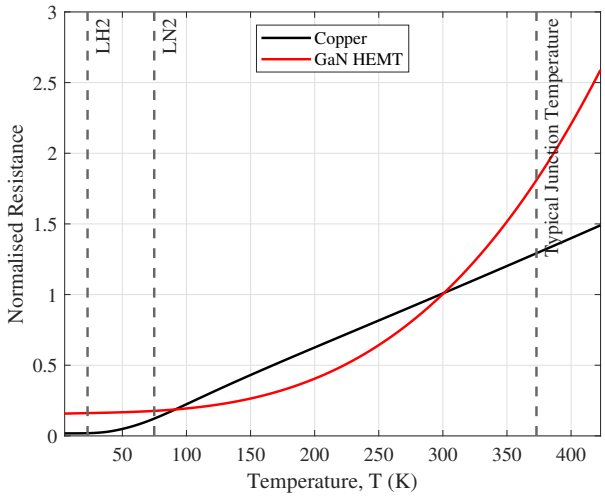


Figure 1.1: Resistance of copper [6] and the on-state resistance of a GaN HEMT against temperature [7], both normalised to their room temperature value.

Cryogen	Saturation Temperature, T_{sat} (K)	Latent heat of vaporisation, Δh_{fg} (kJ kg^{-1})	Liquid density, ρ (kg L^{-1})
Helium	4	20.6	0.13
Hydrogen	20	441	0.07
Neon	27	85.8	1.21
Nitrogen	77	199	0.81
Oxygen	90	213	1.14
Methane	112	510	0.42

Table 1.1: Key properties of common cryogens [8].

temperatures is carbon-dioxide at 195 K, temperatures below this point are often considered to be cryogenic, although others consider the threshold to be 120 K [4].

The key parameters for five cryogens are tabulated in Table 1.1. Nitrogen and oxygen both make up significant fractions of the the atmosphere, 78% and 21% respectively, and are therefore obtained through the liquefaction of air. Neon can also be obtained from liquefied air but constitutes a much smaller fraction of atmosphere, only 1 part in 79000 by mass. Hydrogen and methane (the predominant fluid in liquefied natural gas) are included as they are two fuels which are stored in their cryogenic liquid state to increase their energy density. Helium has the lowest saturation temperature of any cryogenic fluid, only 4 K above absolute zero.

Here, *cryogenic cooling* is defined as being where heat is rejected to a cryogenic liquid that would normally exist in a gaseous state at room temperature. Whereas

conventional or *room temperature cooling* is defined as being where the heat is rejected to ambient air (this might be achieved using intermediate non-cryogenic cooling circuits). The term *conventional* is generally used in the context of aircraft in this work instead of *room temperature*, as the temperature of the air at a typical cruising altitude of 10 km is 220 K [9].

1.2.2 Liquid Hydrogen Fuelled Aircraft

Of the cryogens listed in Table 1.1, nitrogen and helium are the most commonly used as coolants. Hydrogen and liquefied natural gas (predominantly methane) can potentially serve a dual purpose on aircraft; firstly as a fuel and but also secondly as a cryogenic coolant.

Liquid hydrogen fuelled aircraft are being considered as one of the paths to decarbonise the aviation sector [1]. The first commercial aircraft are expected in the next decade and may scale up to account for between 13 and 33% of the aviation market by 2050 [1], [2].

Hydrogen produces zero tail-pipe carbon emissions and no particulates, regardless of whether it is burnt in a gas turbine or reacted in a fuel cell. The combustion of hydrogen also produces 90% less nitrous-oxides than kerosene (zero nitrous-oxide is emitted from a hydrogen fuel cell). Greater quantities of water vapour, which is also a greenhouse gas, will be emitted by using hydrogen fuel. The climate benefits from reducing the carbon-dioxide and nitrous-oxides emissions are significantly greater than the detrimental effects of the increased water vapour [10]. Assuming that the liquid hydrogen is produced using non-carbon emitting sources of energy (such as renewables or nuclear) transitioning to hydrogen aircraft may lead to a reduction in the climate warming effect (radiative forcing) due to aviation, by between 50-60% by 2100 [10].

1.2.3 Cryogenically Cooling an Aircraft Propulsion System

On a hydrogen fuelled aircraft, the liquid hydrogen is drawn from a tank and then requires evaporating and heating before reaching the inlet of either a HFC or gas turbine. This is to avoid freezing the water produced in the HFC reaction or to increase the enthalpy of the fuel for combustion. Notionally, this could be achieved using the heat losses of a cryogenically cooled propulsion system. This process is represented in the high-level system diagram shown in Fig. 1.2 for a system using a hydrogen fuel cell. So that the desired cryogenic temperatures in the propulsion system can be maintained, the efficiency of the system must be sufficiently high that

the liquid hydrogen flowrate can absorb the losses generated by each subsystem, the sum of which are shown in Fig. 1.2 as Q_{P}.

The hydrogen in the tanks is in a thermal equilibrium between the liquid and vapour phases, at a fixed pressure set by the venting pressure of the tank. The liquid hydrogen is drawn from the bottom of the tank, a small fraction of which will evaporate in the transfer lines between the storage tanks and the propulsion system, resulting in a two-phase flow. The fraction of the flow in the vapour phase is the vapour quality, χ, which equals 0 when completely liquid and 1 when it is completely vapour. The specific energy required for the fluid to change phase is known as the latent heat of vaporisation, Δh_{fg}.

The fuel flow is evaporated and heated in at least one heat exchanger used to cool subsystems in a cryogenically cooled propulsion system, HX(1)...HX(N). A final heat exchanger, HX(A), provides any supplementary heat required for the hydrogen to reach the optimal HFC inlet temperature. HX(A) sources heat from the HFC losses, with the remaining excess heat from the HFC rejected to the exterior airflow via HX(B). All the fluid is therefore evaporated before entering the HFC at 3 atm ($\chi_{\mathrm{HFC}} = 1, T = T_{\mathrm{HFC}}$), which is typical for an automotive HFC [11]. Additional intermediate cooling loops between the liquid-hydrogen and propulsion system components, with helium or another inert gas as the working fluid, may be used to separate high-voltage or sensitive propulsion system components from the flammable and reactive hydrogen.

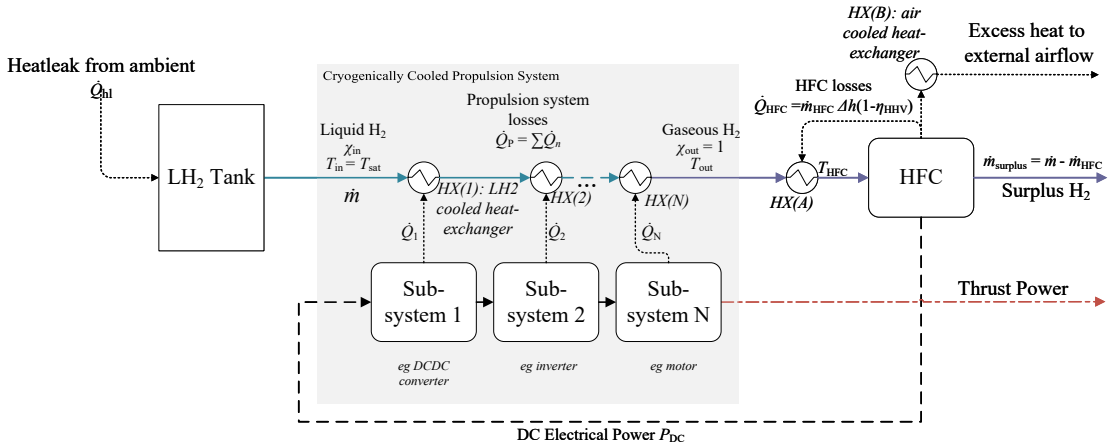


Figure 1.2: System diagram for a liquid hydrogen cooled electric aircraft propulsion system. $n = 1...N$ sub-systems in the cryogenically cooled propulsion system each have an associated loss, Q_n, dissipated in heat-exchanger HX(n). The hydrogen is heated to the required HFC inlet temperature, T_{HFC}, by HX(A) using the heat generated by the HFC. Any additional heat from the HFC is dissipated to the external airflow by HX(B).

To cryogenically cool the propulsion system, the system losses must be dissipated in the colder hydrogen flow. The heat energy causes the flow to evaporate (the latent heat of vaporisation, Δh_{fg}), and to raise the temperature of the flow (the sensible heat of the fluid). The fluid temperature increases from its saturation temperature, T_{sat}, up to the propulsion system outlet temperature, T_{out}. Each subsystem in the propulsion system is cooled in turn by a fluid of increasing quality and/or temperature. Note that a heat-exchanger requires a ΔT to operate, and so the internal temperature of a subsystem will always be greater than the temperature of the liquid hydrogen.

In an open system such as the one described, the fluid enthalpy is used to calculate the change in quality and temperature of the fluid in response to heat input and work done, as described by the first law of thermodynamics given in Eq. 1.1.

$$q - w = h_2(P_2, T_2) - h_1(P_1, \chi_1) \tag{1.1}$$

In Eq. 1.1, h_1 & h_2 are the enthalpy of the fluid before and after the propulsion system heat exchangers ($h_{\mathrm{in}}, h_{\mathrm{out}}$). The work done, w, can be assumed to be small.

$$q \approx \Delta\chi \cdot \Delta h_{\mathrm{fg}} + \int_{T_{\mathrm{sat}},P}^{T_{\mathrm{out}}} C_{\mathrm{p}}(T, P)\mathrm{d}T \tag{1.2}$$

Using this equation the amount of heat that can be rejected to the fluid, q, can be calculated.

The enthalpy-pressure graph for hydrogen is shown in Fig. 1.3, with the inlet and outlet conditions marked to illustrate this.

1.2.4 Cryogenic Cooling in a Laboratory Setting

There are significant challenges regarding the use of liquid hydrogen in a laboratory environment, mainly associated with its flammability. Liquid nitrogen (LN2) and liquid helium are the two cryogens commonly used for cryogenic cooling. Liquid nitrogen is cheap, abundant, inert, and the temperature reduction from room temperature to its boiling point (77.15 K) is 80% of the temperature reduction between room temperature and the boiling point of liquid hydrogen (20 K). Liquid nitrogen is therefore well suited for demonstrating the cryogenic performance of power electronics. More complex and expensive cooling techniques, involving helium or neon cooling loops and cold-heads could be used in future work to demonstrate operation at lower temperature.

Despite being inert, there are significant risks involved with the use of liquid nitrogen. Firstly, the low temperature poses a risk of cold-burns and frostbite. Secondly

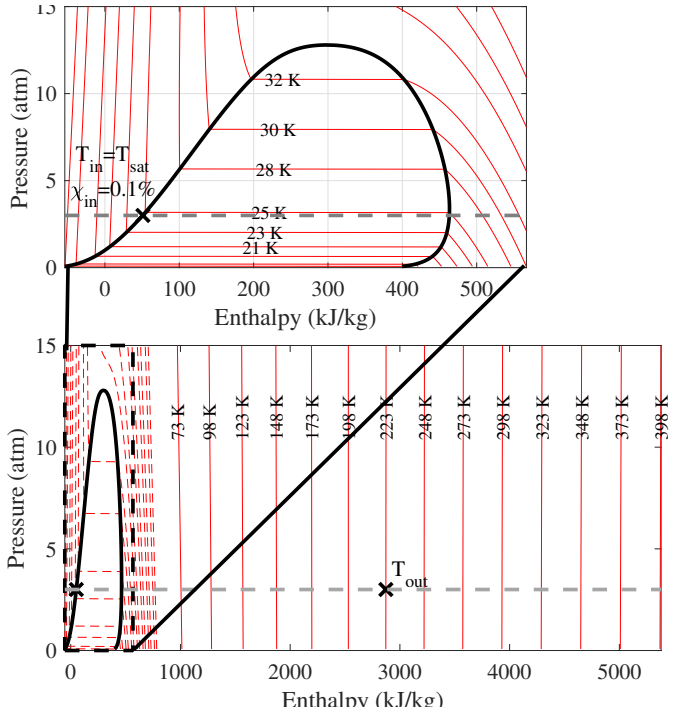


Figure 1.3: Pressure-enthalpy graph for hydrogen, the black curve shows the saturation region, red lines denote isotherms (lines of constant temperature). An enlarged view of the saturation region is shown in the inset. Data from [12].

the large expansion ratio between liquid and gaseous nitrogen (700 times); 1) means a relatively small quantity of liquid nitrogen (tens of litres) evaporating can lead to a fatally low concentration of oxygen in a small room, and 2) will cause over-pressure in a sealed vessel.

Two methods of cooling with liquid nitrogen are 1) directly submerging an assembly in a pool of liquid nitrogen and 2) flowing liquid nitrogen though a cold-plate to which the assembly is thermally attached.

1.3 Aircraft Electrification

Aircraft electrification has the goal of reducing carbon emissions and can take three forms [13]:

- All-electric aircraft (AEA) – all aircraft systems, including the propulsion system, are electrically powered.
- More-electric aircraft (MEA) – increased use of electric power for systems such as flight control, engine starter/generator, and fuel pump. Replacing current systems powered with mechanical, hydraulic or pneumatic power.

- Turbo-electric aircraft (TEA) – electric drives and machines are incorporated into the propulsion system to provide thrust. A conventional kerosene fuelled jet turbine delivers a large fraction of the propulsion power, driving the fans directly and/or a generator to provide electrical power for the machines and drives.

90% of an aircraft's power is used for propulsion [13]. Consequently, limited reductions in emissions with MEA are possible, but may lead to reduced fuel consumption by up to 9% [14], beneficial for aircraft manufactured in the near term. A more significant reduction in fuel consumption can be expected to be achieved by hybridising the propulsion system in TEA [13].

MEA and TEA, while still relying on hydrocarbon fuel for energy storage, can still reduce greenhouse gas emissions by increasing the efficiency of the aircraft. Sustainable aviation fuels are an active area of research and, when combined with electric propulsion systems, may lead to significant reductions in emissions [15].

Fuelling TEA with liquid hydrogen for long-range aircraft would emit less greenhouse gases than hydrocarbon fuels, as explained in Section 1.2.2, and hydrogen fuel cells could be used to power AEA for short range aircraft [10].

Aircraft with electric propulsion systems in all-electric and turbo-electric aircraft enable alternative, more efficient aircraft designs that are not possible with current aircraft propulsion technology. Electric propulsion lends itself well to distributed propulsion, where a greater number of smaller, motor driven propellers are used to deliver the required power. Distributed propulsion systems enable boundary layer ingestion. This is where the slow-moving boundary layer around the aircraft is ingested by the propeller, reducing the overall drag on the aircraft. The low speed of the air also reduces the power required to produce an equivalent thrust to a propeller in the free stream [16].

1.3.1 Aircraft Types

References are made in this thesis to the propulsion system requirements for different aircraft types. These are listed and contextualised below.

- Light aircraft – maximum gross take-off weight of 5670 kg or less [17]. Typically, these might be used as personal aircraft or for small-scale passenger and freight transport. Two examples at the top end of this type are the de Havilland Canada DHC-6 Twin Otter and Beechcraft B200 Super King Air.

- Large aircraft – maximum gross take-off weight greater than 5670 kg [17].
  - Wide-body long range – a twin-aisle aircraft capable of long range flights, such as the Airbus A380 and the Boeing 747. Both have a range of just over 15 000 km and are typically used for long-haul flights.
  - Narrow-body regional – also known as single-aisle aircraft and includes the Boeing 737 and Airbus A320. Typically used for short-haul and domestic flights.

1.4 Inverters and Motor Drives

An inverter is a power-electronics circuit that converts DC power into AC. A motor drive refers to the complete system responsible for converting DC power from a DC power source such as a battery or fuel cell and converting it into three-phase AC, to drive a motor. An inverter is a core component in a motor drive, that may also include input and output EMI filters, DC link capacitors, sensors, a controller, and a thermal management system as shown in Fig. 1.4 [4].

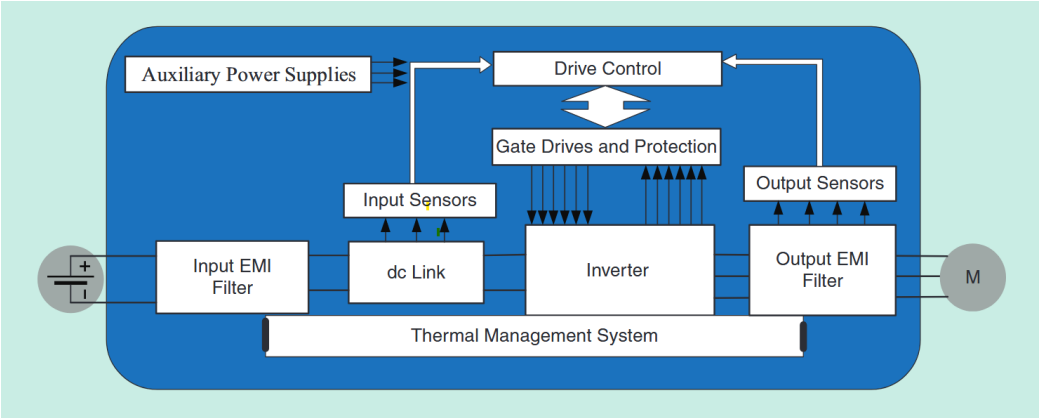


Figure 1.4: Block diagram of a motor drive showing the inverter's function, extracted from [4].

A standard inverter topology used in motor drives is a three-phase bridge, a schematic of which is drawn in Fig. 1.5. It comprises of six semiconductor switches, implementing a two-level voltage source inverter (2L-VSI). In a motor drive inverter, the switches can be expected to generate the majority of the losses [18].

High efficiency is essential for aircraft motor drives, as greater losses increase fuel consumption and therefore decrease the range of the aircraft. The mass of the motor drive is another significant factor that affects the performance of an aircraft. This

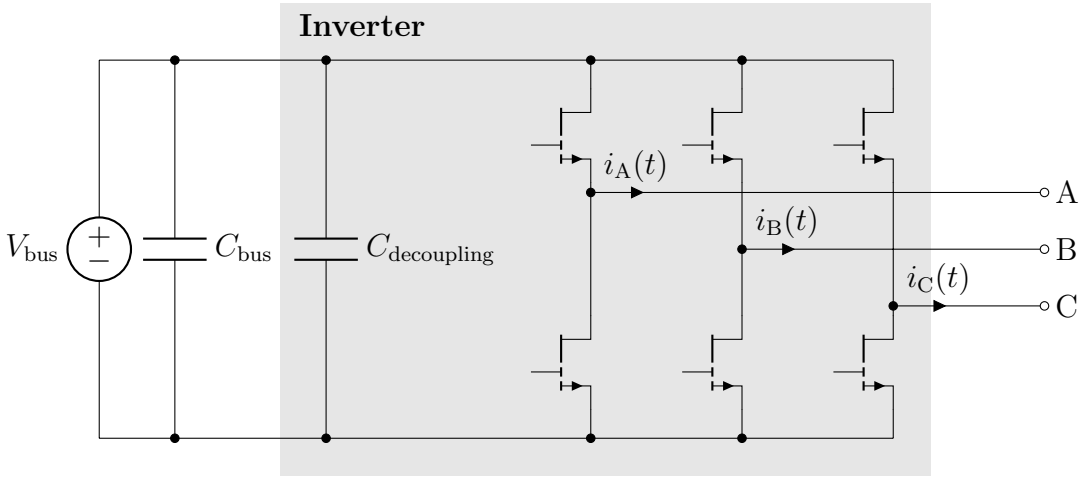


Figure 1.5: Schematic of a three-phase bridge circuit. The components that form the inverter are highlighted.

motivates requirements for specific power, normally given in terms of kW kg^{-1}. NASA Advanced Air Transport Technology Project (2015), set the target of $19\,\text{kW kg}^{-1}$ for a megawatt-level inverter electric aircraft propulsion inverter [4].

Propulsion systems for narrow-body medium-range aircraft typically require multiple megawatt scale inverters [19], [20], [21]. Light aircraft require significantly less power. One demonstration light aircraft requires two 280 kW motors and drives [22]. A possible implementation of a hydrogen fuelled light aircraft propulsion system is shown in Figure 1.6.

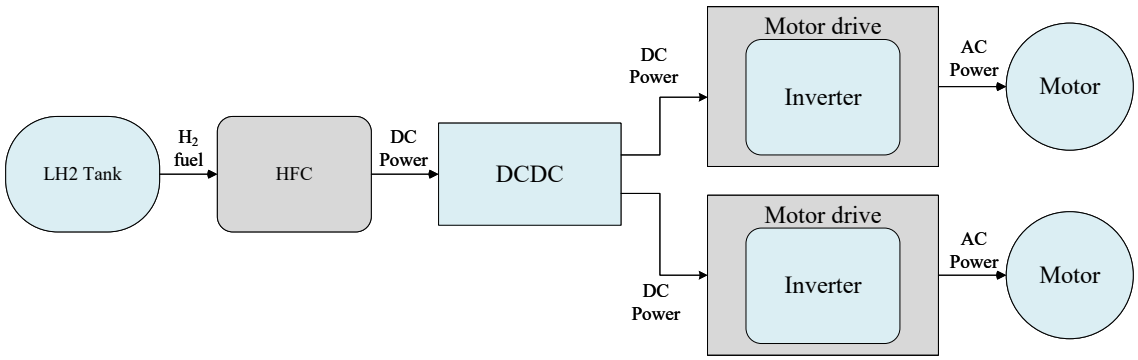


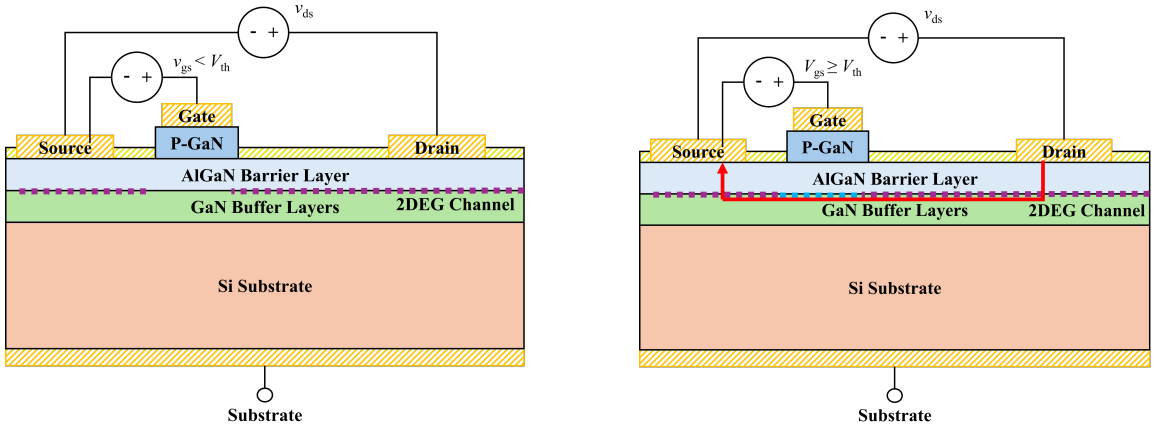
Figure 1.6: Block diagram of a hydrogen fuelled light aircraft propulsion system. Systems that are could be cooled to cryogenic temperatures are shown in blue.

For an aircraft, the peak power required for take-off can be expected to be between 3 and 4 times the cruising power. This is required for up to 20 minutes [20].

1.5 GaN HEMT

Gallium-nitride is a wide-bandgap semiconductor material whose properties, including electron mobility and velocity, maximum electric field strength, and bandgap, result in power-transistors with superior performance compared to Si and SiC. GaN high-electron-mobility-transistors (HEMT) are field-effect transistors (FET) that incorporate a hetro-junction of AlGaN-GaN. A highly conductive two-dimensional electron gas (2DEG) forms at the hetro-junction, creating a channel with high electron-mobility reducing the resistance of the FET [23].

GaN HEMTs are naturally depletion-mode transistors, and therefore conduct with zero gate voltage applied (normally-on). Transistors typically used in power electronics are normally-off enhancement-mode transistors, to achieve this, it is necessary to modify the GaN transistors structure. One method is to insert a positively-doped GaN (P-GaN) layer between the metallized gate contact and the AlGAn barrier layer to form a Schottky contact. The P-GaN depletes the 2DEG below the gate, giving it a normally-off behaviour. This is how the GaN Systems transistor, used throughout this work, operates. The structure is drawn in Fig. 1.7. Other GaN transistor types include gate-injection transistors (GIT), where an ohmic contact is used to inject current into the GaN buffer layer, and CASCODE transistors where a normally-off silicon device is placed in series with a d-mode GaN HEMT to create a normally-off transistor [24].



(a) Blocking (b) Conducting

Figure 1.7: Structure of an enhancement-mode GaN HEMT, shown in the conducting and blocking states [24]. When the gate-source voltage, v_{gs} exceeds the threshold voltage, V_{th}, a two-dimensional electron gas layer forms allowing current to conduct.

1.5.1 Cryogenic Properties of GaN

At cryogenic temperatures, the electron mobility in the 2DEG improves due to reduced phonon scattering. This results in the on-state resistance falling to as little as 1/5 of its value at room temperature.

The improvement in performance of a GaN transistor at cryogenic temperatures is demonstrated in Fig. 1.8. The specific on-state resistance is plotted against the breakdown voltage (a well-known figure of merit) for seven state-of-the-art GaN on Si HEMTs, including the 650 V GaN Systems HEMT [25]. The GaN Systems transistor is plotted both at both room temperature (GS-650) and at cryogenic temperatures (GS-650 Cryo). The theoretical semiconductor limits are calculated and overlaid. The cryogenically cooled GaN Systems HEMT results in a significantly higher figure of merit.

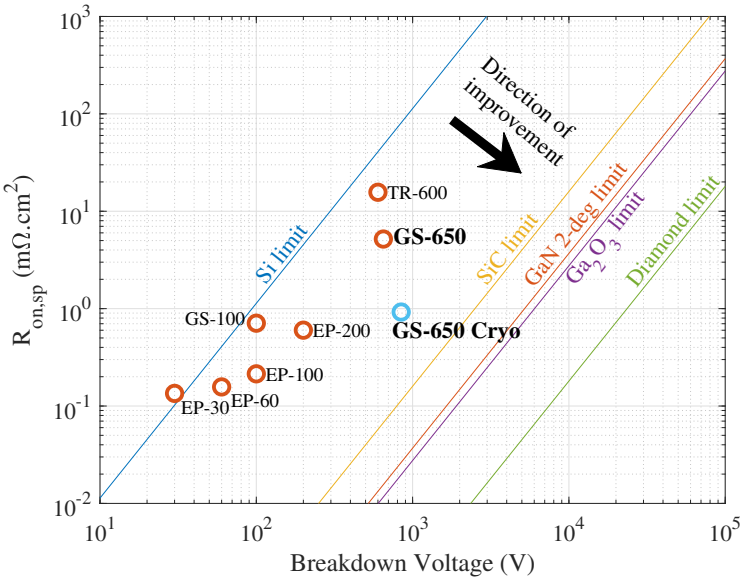


Figure 1.8: $V_B/R_{on,sp}A$ figure of merit for commercial state-of-the-art GaN transistors shown at red circles. The theoretical limits of wide-bandgap (WBG) and ultra wide-bandgap (UWBG) materials are also plotted. Reproduced from data published in [25]. The GaN Systems 650 V (GS-650) transistor technology used in this work is shown with its properties at cryogenic temperatures in blue (GS-650 Cryo), showing a significant improvement in the figure of merit (FOM).

Although GaN HEMTs are currently limited to breakdown voltages up to 650 V, the expectation is that higher voltage GaN transistors, suitable for motor drive applications, will become available in the future [26], with the first 1200 V HEMTs in development [27].

1.5.2 Description of Transistor Parasitics

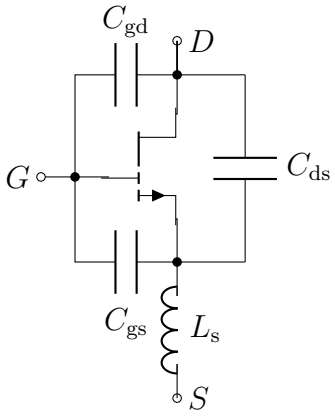


Figure 1.9: GaN HEMT with parasitic capacitances and source inductance.

The main parasitic elements intrinsic to a HEMT are shown in Fig. 1.9. The inclusion of these capacitors and inductor in the model of a HEMT are necessary to understand its switching behaviour and failure modes discussed within this thesis.

The parasitic capacitances result from the internal structure of the transistor. Relatively large metallized areas directly above the semiconductor form capacitances to both the semiconductor and adjacent metallized pads or tracks. The parasitic capacitances are non-linear and are a function of the voltage across them. Values for these capacitances are not given in manufacturer's datasheets, but values for output capacitance, C_{oss}, the input capacitance, C_{iss}, and the reverse transfer capacitance, C_{rss}, to which they are related, are frequently provided ($C_{\mathrm{oss}} = C_{\mathrm{ds}} + C_{\mathrm{gd}}$, $C_{\mathrm{iss}} = C_{\mathrm{gd}} + C_{\mathrm{gs}}$, $C_{\mathrm{rss}} = C_{\mathrm{gd}}$).

The gate-drain capacitance is also known as the Miller capacitance. When a transistor in a half-bridge is switched on, current conducts through the Miller capacitance of the opposing transistor due to the fast change in voltage across it. The Miller current can raise the gate voltage of the opposing transistor, which is in the off-state, above the threshold voltage, switching the transistor on and causing shoot-through. This is where both transistors are simultaneously conducting shorting the DC bus, which can lead to thermal failure due to large conducted currents.

The source inductance originates from the inductance of internal interconnects that connect the transistors external terminals to the die, as well as the inductance of the metallized conductors on the die itself. The source inductance can be critical to the switching performance of the transistor as the voltage across it, caused by the

$\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ during switching transitions ($V = L_\mathrm{s}\mathrm{d}i_\mathrm{d}/\mathrm{d}t$), reduces the voltage seen at the gate, slowing and potentially interrupting the switching transition.

Notably, a HEMT does not have a body-diode but will still reverse conduct when $V_\mathrm{gs} = 0$, if V_gd is greater than the threshold voltage [28]. The source-drain voltage seen in reverse conduction is approximately equal to the threshold voltage minus the gate voltage, which may be negative ($-3\,\mathrm{V}$ is typical) to decrease the likelihood of false turn-on, $V_\mathrm{sd} \approx V_\mathrm{th} - V_\mathrm{gs}$.

1.6 Research Question

Developing GaN HEMT based inverters is critical to achieving higher efficiency and power density in megawatt scale inverters [4]. Currently, there is the lack of availability of high breakdown voltage, high-current GaN power modules, this is one barrier to achieving megawatt scale inverters. It is expected that this will change as GaN technology develops [29]. Improvements to the efficiency and power-density of aircraft propulsion motor drives could then be realised by cooling the GaN switches to cryogenic temperatures, but to date, a cryogenic GaN inverter has not yet been demonstrated at even the kilowatt scale with the currently available discrete GaN transistors. The focus of this thesis is therefore the characterisation of a current best in class GaN HEMT, and the development of best practices for the design of a kilowatt scale cryogenic GaN inverters, with the aim of answering the primary research question: *Are cryogenically cooled GaN inverters suitable for aircraft applications?*

This research question can be answered by resolving a number of sub-questions, which were identified as belonging to two key topics. The first topic focuses on determining if there is an improvement in performance (such as a reduction in losses) of a GaN inverter at cryogenic temperatures. The second topic of questions concerns assessing whether a cryogenic GaN inverter suffers any limitations (such as additional failure modes) due to the extreme operating conditions.

Regarding the losses and efficiency at cryogenic temperatures the following research questions will be answered:

1a. How are switching losses of a GaN HEMT affected by cryogenic temperatures?

1b. What improvements in efficiency and peak power can be achieved by cryogenically cooling a GaN inverter compared to a conventionally cooled GaN inverter for aircraft propulsion applications?

1c. Losses in a cryogenic GaN inverter are expected to be very small compared to the apparent power. How can the efficiency be accurately measured for a cryogenic inverter, in order to quantify the improvement in performance?

On the topic of limitations and cryogenic failure modes the following questions are posed:

2a. Does large heat generation in the transistor junction and resultantly large temperature gradients across the transistor package degrade the performance of a GaN HEMT at cryogenic temperatures, and what determines the maximum thermal dissipation of the transistor at cryogenic temperatures?

2b. Do new mechanisms lead to failure for a GaN transistor at cryogenic temperature or are conventional failure modes exacerbated by the change in the properties of the GaN transistor at cryogenic temperatures?

2c. A cryogenically cooled GaN inverter has not yet been demonstrated in the literature at a power greater than 1 kW. Is a cryogenic GaN inverter suitable for a motor drive application achievable with current technology, and if so, what is its maximum achievable power and efficiency?

Increasing propulsion system efficiency and power density is important to maximise the range of an aircraft and to enable sufficient take-off power. The first topic of questions evaluates if cryogenically cooled GaN inverters will deliver a benefit in this regard, establishing if the technology is therefore suitable for aircraft. The second topic investigates the limitations of a cryogenic GaN inverter in order to identify potential constraints for the development of the technology for aircraft applications.

The thesis is structured as follows. In Chapter 2 the current literature on cryogenic power electronics with an emphasis on GaN technology is reviewed. In Chapter 3 a characterisation of the on-state resistance and switching performance of a GaN transistor is conducted. Chapter 4 sets out a method to model a GaN voltage source inverter, the performance and loss breakdowns of a prototype cryogenic GaN inverter and a hypothetical aircraft propulsion inverter are predicted. Chapter 5 describes the design and testing of a prototype GaN inverter.

Chapter 2

Literature Review

Power electronics is the field associated with the control, conversion and conditioning of electric power [30]. In power electronics semiconductor switches are used in combination with passive components such as inductors and capacitors to control power flow as well to regulate its form, whether that is AC or DC voltage and current. The first semiconductor power switches were thyristors, which were first commercially manufactured in the 1950s [31]. Thyristors do not conduct current until a voltage is applied to the gate terminal, once turned-on they continue to conduct even once the gate voltage is removed, and only return to the blocking state once the conducted current falls below the holding current. This limited the number of applications except in line-commutated converters such as rectifiers and cycloconverters [31].

The bipolar transistor (BJT) and metal-oxide semiconductor field effect transistor (MOSFET) were the next innovation in semiconductor switches for power electronics and were developed over the course of the 1960s and 70s [31]. While both are silicon transistors, the BJT is a current amplification transistor, this is where the current conducted is proportional to the base current supplied. This differs from the MOSFET where the conducted current is controlled by the voltage applied to the gate, this combined with simpler manufacturing methods led to the widespread adoption of MOSFETs in both integrated circuits and for power switches [31].

In the 1980s the insulated gate bipolar transistor (IGBT) was developed to overcome the low current gain of the BJT. By pairing a MOSFET with a bipolar transistor large currents could be conducted with a voltage controllable gate terminal. The IGBT found an application in medium to high power applications [32].

The most recent development in semiconductor switches used in power electronics is the introduction of wide bandgap (WBG) semiconductors. WBG semiconductors such as silicon-carbide (SiC) and gallium-nitride (GaN) have a larger bandgap energy than silicon (3.26 eV and 3.45 eV respectively compared to 1.1 eV for silicon). The

breakdown field in wide bandgap semiconductors is consequently higher as shown in Table 2.1. A larger breakdown field results in a shorter drift region being needed to achieve the required breakdown voltage. Consequently the transistor will have lower resistance. Additional properties such as high drift velocities, which is directly related to switching speed, and high thermal conductivity (in the case of SiC) gives WBG transistors far superior performance compared to conventional Si transistors such as Si MOSFETs and Si IGBTs [33].

Table 2.1: Properties of Semiconductor Materials [33]

Property	Si	6H-SiC	4H-SiC	GaN
Bandgap, E_g (eV)	1.10	3.03	3.26	3.45
Dielectric constant, ε_r	11.9	9.66	10.1	9.0
Breakdown field, E_c ($\mathrm{kV\,cm^{-1}}$)	300	2500	2200	2000
Electron mobility, μ_n ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	1500	500	1000	1250
Hole mobility, μ_p ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	600	101	115	850
Thermal conductivity, k ($\mathrm{W\,cm^{-1}\,K^{-1}}$)	1.5	4.9	4.9	1.3
Thermal expansion ($\times 10^6$ $\mathrm{K^{-1}}$)	2.6	3.8	4.2	5.6
Electron drift velocity, u ($\times 10^7$ $\mathrm{cm\,s^{-1}}$)	1.0	2.0	2.0	2.2

The first SiC power transistor was commercially available in 2011 [34] and Transphorm released a 600 V GaN HEMT in 2012 [35].

2.1 Transistor Cryogenic Characterisation

The discovery of high temperature superconductors in 1986 [36] appears to have initially motivated the investigation of transistor properties at cryogenic temperatures. The first characterisation of a power MOSFET was conducted in 1989 [37]. They noted that the on-state resistance of a Si MOSFET decreased by a factor of 5 at 77 K, at the expense of the breakdown voltage which was seen to decrease by a third. Characterisation has subsequently been performed for various semiconductor switches and has resulted in tens of papers.

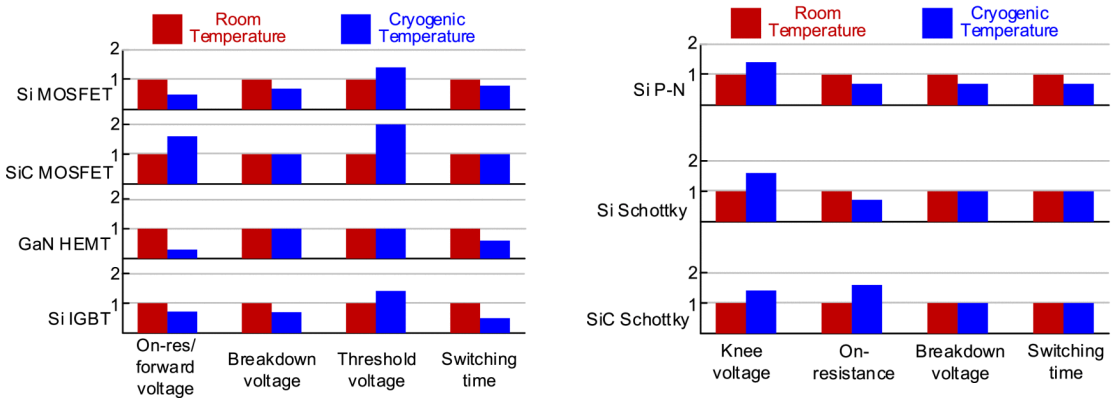
The first paper to report the characteristics of a GaN transistor at cryogenic temperatures was published much more recently in 2016 [38]. In this paper it was found that the on-state resistance of a GaN HEMT fell by 85% at 78 K and it was successfully demonstrated to switch in a double-pulse test. The authors later published a paper reporting the operation of the first cryogenic GaN converter in 2017 [39].

The characterisation work prior to [38] investigated silicon and silicon-carbide transistors. Papers characterising GaN transistors are tabulated in Table 2.3. While

this thesis is focused on GaN based inverters, it is important when determining its suitability for aircraft traction inverters applications to assess alternative power semiconductor materials such as silicon (Si) and silicon-carbide (SiC).

2.1.1 Comparison of the $R_{ds(on)}$ and V_{bd} of GaN, Si and SiC at cryogenic temperatures

A good summary of the work characterising silicon (Si) and silicon-carbide (SiC) power devices can be found in Gui et al. [40]. Fig. 2.1 has been extracted from [40] and summarises the findings.



(a) Comparison of switches.

(b) Comparison of diodes.

Figure 2.1: Comparison of the properties of different power devices at cryogenic temperature normalised by their room temperature value. Extracted from Gui et al. [40]

It has was observed in [40] (2020) and in more recent papers [41], [42], [43] (2024, 2022, 2021) that the on-state resistance of Si devices reduces with temperature with carrier freeze-out only limiting the minimum on-state resistance at 50 K to 100 K. The Si MOSFET suffers from reduced breakdown voltage at cryogenic temperatures due to an increase in the mean free path of carriers and higher impact ionisation. This results in more high-energy electron-hole pairs that contribute to avalanche breakdown [40].

It has been shown that SiC has unfavourable on-state resistance characteristics at low temperatures, experiencing increasing carrier freeze-out with decreasing temperature. This negates any increase in electron mobility, leading to an overall increase in on-state resistance below ~220 K [40], [42], [44], [45], [46], [47], [48], [49], [50]. The negative temperature coefficient of the on-state resistance at low temperatures may make paralleling SiC transistors challenging.

Thirteen sets of results characterising commercial GaN transistors have been published and are tabulated in Table 2.3. They report favourable characteristics at cryogenic temperatures. GaN devices have a monotonically decreasing on-state resistance with decreasing temperature (as low as 4 K) with no appreciable decrease in the breakdown voltage being reported, and [51] reports a 10% to 40% increase in the breakdown voltage. The monotonically decreasing on-state resistance suggests that the increased electron mobility dominates any carrier freeze-out that may occur.

Semiconductor Material	Normalised breakdown voltage $V_{BD}/V_{BD,298\,K}$	Normalised on-state resistance $R_{ds(on)}/R_{ds(on),298\,K}$
Si	↓↓ 78 – 84%	↓↓ 15 – 25%
SiC	↓ 95 – 100%	↑↑ 150 – 350%
GaN	↑↑ 110 – 140%	↓↓ 20 – 30%

Table 2.2: Table showing the magnitude of the change in the breakdown voltage, V_{BD}, and on-state resistance, $R_{ds(on)}$, for Si, SiC and GaN transistors at cryogenic temperature (98 K) with values normalised to room-temperature [40], [47], [51], [52]. Cells shaded in red show a degradation in the performance at cryogenic temperature, while green shows an improvement.

2.1.2 Switching behaviour

Switching transitions are both a source of loss in an inverter and induce voltage and current overshoots that can be potential failure modes as a result. These overshoots occur due to the fast switching speeds and parasitic elements within the transistor and switching circuit. A review of the existing literature on this topic is therefore essential to answer the research question posed in this thesis.

2.1.2.1 Si and SiC switching behaviour

Wei et al. (2023) [53] reports that the switching losses of the Si MOSFET and IGBT characterised decrease fractionally more than the SiC and GaN transistors characterised (turn-off losses in one Si MOSFET fell by as much as 80%). SiC transistors generally had a small changes in the switching losses between room and cryogenic temperatures, though one of the SiC transistor characterised suffered a 2.5 times increase in turn-on losses.

2.1.2.2 GaN switching behaviour

In the literature there is significant uncertainty regarding the effect that cryogenic temperatures have on the switching losses. Measurements from [54] suggest up to a 30% reduction in switching losses down to the minimum temperature measured. In [51] the switching losses are measured to not decrease monotonically and start increasing again below $\sim$200 K. [55] reports that the switching losses of a cascode transistor are unchanged at cryogenic temperatures.

Ren et al. [54] demonstrates two failure modes that can occur for a GaN HEMT at cryogenic temperatures. These are related to miller turn-on, and oscillation due to faster $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ interacting with the source inductance. In [56] it is shown that the increased transconductance makes the GaN transistor characterised more prone to instability, resulting in sustained oscillations.

Table 2.3: Papers characterising GaN transistors.

Paper Details	Power Device Technology	Temperature Range	Findings and Outcomes
Colmenares et al. [38] (2016)	EPC HEMT	78 K to 298 K	On-state resistance measured to reduce by 85% and threshold voltage increase by 16%. Double pulse test measurements are conducted with no change in the switching characteristics observed. The switching energies are not reported.
Mayo et al. [57] (2017)	GaN Systems HEMT	48 K to 300 K	81.7 % reduction in $R_{ds(on)}$ observed at the lowest measured temperature compared to RT. The threshold voltage increased by 6.2 % compared to RT, breakdown voltage was not observed to change.
Ren et al. [58] (2018) [54] (2020), Zhang et al. [59] (2018)	GaN Systems HEMT	93 K to 298 K and 77.15 K	75% reduction in $R_{ds(on)}$ compared to RT, 30% reduction in switching losses. A deskew was required between the voltage and current channels which the result was very sensitive to.
Nela et al. [52] (2021)	Multiple HEMTs	4.2 K to 400 K	Between a 50% and 83% reduction in $R_{ds(on)}$ at CT compared to RT was observed for the four transistors investigated. A reduction in threshold voltage was also observed in two of the transistors.
Mehrabankhomartash et al. [47] (2021)	GaN Systems HEMT	98 K to 298 K	Static characterisation was performed with curve-tracer. 35% higher breakdown voltage measured at cryogenic temperatures. DPT are conducted and switching energy is observed to increase below ∼198.15 K, a SiC freewheeling diode was used rather than a complementary GaN switch in a half-bridge.

Wei et al. [60] (2021) [61] (2022)	GaN Systems HEMT	93 K to 298 K	Conducts static and dynamic characterisation of a 100 V and 650 V GaN HEMT. Dynamic on-state resistance was significantly reduced at low temperatures. Switching energy fell by 20% but no information regarding the circuit is given other than the gate-driver IC.
Wei et al. [55] (2021)	900 V Transphorm Cascode FET	93 K to 298 K	Static characterisation and DPTs conducted. 38% reduction in $R_{\mathrm{ds(on)}}$, V_{th} increases by 16%, switching losses remain constant.
Hossain et al. [62] (2021)	GaN Systems and Panasonic HEMT	78 K to 298 K	100 V and 600 V GaN HEMT characterised and used to inform a Saber model of the transistor to help the design of cryogenic converters.
Hossain et al. [63] (2022)	1.2 kV GaNPower HEMT	93 K to 298 K	63% reduction in $R_{\mathrm{ds(on)}}$, 20% increase in V_{th} , 34% increase in g_{m}.
Wei et al. [64] (2022)	GaN Systems HEMT	77.15 K	DPT conducted at cryogenic temperature, using a current in excess of the rated current. An increase in the saturation current from 160 A to 250 A was reported. The switching energies from the DPT are not reported.
Wang et al. [65] (2023)	Schottky type p-GaN gate HEMT	78 K to 298 K	Examines V_{th} instability at cryogenic temperatures. Found V_{th} changes by less than 0.3 V.
Jiang et al. [66] (2023)	HEMT	15 K to 400 K	Analysis of the gate-leakage mechanism at cryogenic temperatures
Li et al. [56] (2023)	GaN Systems HEMT	4 K to 298 K	Characterisation of a GaN Systems HEMT performed and used to inform a small-signal circuit model. Used to calculate of range V_{bus} for which unstable oscillations will occur.

2.1.3 Experimental Techniques for Cryogenic Characterisation

Testing power-transistors at cryogenic temperatures is not a trivial undertaking. Static measurements with a curve-tracer or dynamic measurements with double pulse test (DPT) circuits, are typically conducted with device under test (DUT) placed in a cryo-chamber. A method of building a low cost cryo-chamber is presented in [67].

Dynamic characterisation is a significantly harder endeavour than static, requiring measurement equipment and gate drivers to also be at cryogenic temperatures, which is the subject of [68].

The time taken to thermally cycle the chamber is also significant. [69] describes how power relays can be used to conduct DPTs on multiple transistors without thermally cycling the chamber, increasing the time efficiency of the experiment when surveying a large number of transistors. In [70] a fully automated test-setup is presented which automates static and dynamic measurements at controlled temperatures between 198 K to 423 K.

2.1.4 Gaps in the literature on the topic of transistor characterisation

The negative-temperature coefficient of SiC's $R_{\mathrm{ds(on)}}$ at low temperatures will cause SiC transistors to incur increased conduction losses at cryogenic temperatures. Si transistors are also compromised at cryogenic temperatures where they suffer from reduced breakdown voltage, which may lead to failure during switching transients if the bus voltage is not sufficiently reduced. Of the most commonly used power MOSFET semiconductor materials it can therefore be concluded, that in the application of cryogenic traction inverters, that GaN based transistors are the most suitable and will lead to the largest increase in converter performance at cryogenic temperatures due to the reduced $R_{\mathrm{ds(on)}}$ and abscense of degradation of V. Despite this outstanding questions and gaps in the literature still remain about the characteristics of GaN at cryogenic temperatures, these include:

1. Measurements of $R_{\mathrm{ds(on)}}$ at cryogenic temperatures are typically conducted using small test currents in most of the papers reviewed, the $R_{\mathrm{ds(on)}}$ behaviour at high current densities has only been characterised in [64] up to the room-temperature 60 A rating of the transistor. Characterisation has not been conducted for a GaN transistor at currents exceeding its room-temperature rating, except in a single recent paper (2024) where double pulse tests were conducted [71]. Double

pulse test measurements are conducted using an oscilloscope which do not have the resolution to accurately measure the small on-state resistance and serve primarily to examine transient switching behaviour. As currents in excess of the room temperature rating are potentially viable operating points with cryogenic cooling, accurate measurements of the $R_{\mathrm{ds(on)}}$ would be a valuable contribution to the literature. An open question remains regarding the validity of the ideal resistance MOSFET model for a GaN HEMT operating at extreme cryogenic temperatures and at higher current densities than it is rated.

2. While double pulse tests have been conducted at currents exceeding the rated current [64], continuous operation at high current densities (either at or above the transistors rated current), generating significant heat at the junction while it is at cryogenic temperatures has not been demonstrated in the literature. There is therefore a gap in the literature regarding the effect that large heat dissipations and the associated temperature gradient will have on the GaN transistor package at cryogenic temperatures, and how this will it effect its ability to operate at these extremes?

3. In [51] it is observed the breakdown voltage of GaN HEMTs increases by 15 % to 36 % at cryogenic temperatures, despite this double pulse tests have not been conducted with bus voltages in this increased range. The gap in the literature therefore exists regarding the operation and switching behaviour of GaN transistors in this expanded region of operation.

4. Of the papers that conduct double pulse tests on GaN HEMTs [38], [51], [54], [61] the trends in switching energies are inconsistent and the methods used are not well described or suggest large sources of error. Conclusive measurements of switching energies with a validated test setup would be a contribution to the literature on this topic.

5. In [54] two failure modes for of a GaN HEMT at cryogenic temperatures are demonstrated and explained (miller shoot-through and $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ induced voltage overshoots). While resolutions are suggested none are implemented and solutions to these issues remain an open question in the literature.

2.2 Cryogenic Power Electronics Components

Two review papers present results not only for a range of power devices, but also the other components required in power electronics, such as capacitors, inductors, and integrated circuits. Rajashekara and Akin [72] provides a broad review discussing applications and the state of the research at the time of publication, 2013. Gui et al. [40] examine the suitability of different power devices, passive components, interconnection, and dielectric materials which are commonly used in power electronics and would be required for a cryogenic converter. Comparisons are made showing whether the component exhibits improved or deteriorated properties at cryogenic versus room temperature. Both papers conclude that, for passive components, including capacitors and inductor cores, a careful selection of the component technology is required. Different technologies exhibit varying degrees of either improved and degraded performance at cryogenic temperatures. Polypropylene bulk capacitors and C0G MLCC capacitors (often used in resonant converters) are unaffected by cryogenic temperatures while other types of MLCC capacitors such as X5R and X7R should avoided due to significant degradation in their capacitance and dissipation factor [40]. PCBs, soft solder alloys and dielectric papers were found to be suitable for cryogenic use. The breakdown voltage of silicone gel encapsulants is degraded by exposure to cryogenic temperatures. Hard solders are also not recommended, as they become brittle at cryogenic temperatures.

2.2.1 Gate Driver ICs

In Wei et al. [73] gate driver circuits are subjected to cryogenic temperatures. It was found that the temperature dependence of the Zener diode voltage, which is commonly used to regulate the output voltage of the isolated DC-DC bias supply, caused the output voltage to fall at cryogenic temperatures. Only one of the two gate drive ICs tested functioned below 230 K, this IC was found to function down to 93 K.

Hassan et al. [68] developed a testing platform for characterising devices, and gave a detailed summary of the gate drive supplies and gate drive ICs used. The ADUM4221 and 2EDF8275F gate driver ICs were shown to operate at 18 K and 17 K respectively. The auxiliary supply from [74] were tested at low temperatures and found to function as low as 25 K.

Table 2.4: Papers reviewing gate driver ICs at cryogenic temperatures.

Paper Details	Power Device Technology	Temperature Range	Findings
Wei et al. [73] (2021)	Silicon Labs Si8271, TI UCC5304	93 K to 298 K	UCC5304 did not function below 233.15 K. SI8271 function down to 93.15 K. The auxiliary power supplies used failed below 133.15 K, the Zener diode was deemed to have failed.
Mustafeez-ul-Hassan et al. [75], [76] (2022)	Silicon Labs SI8271, SI8235AD, TI UCC21540A, AD MAX22702, ADUM4221	77 K to 298 K	AX22702 and Si8235AD failed at 100 K, both are BiCMOS. UCC21540A failed at 93 K. Si8271 and ADUM4221 functioned at the minimum temperature. Numerous samples of each gate-driver were tested and the results were consistent between them.

2.2.2 Magnetic Components

Magnetic cores have been observed to suffer from increased hysteresis loss to varying degrees depending on the core material; this is explored in [77], [78], [79], [80]. These papers are summarised in Table 2.5. While not directly relevant for the VSI topology explored in this thesis, auxiliary isolated DC-DC converters are required both for supplying gate driver circuits and for redundant power supplies for an isolated controller in a motor drive system. Isolated topologies such as LLC and flyback converters require magnetic cores to function and the literature suggests they may have degraded performance including increased core losses at cryogenic temperatures. The power requirements for the gate drive supplies is much smaller than the inverter power in a motor drive and therefore the reduced performance of the gate drive supplies if cryogenically cooled are unlikely to have a significant effect on the overall motor drive efficiency.

Table 2.5: Papers reviewing magnetic components at cryogenic temperatures.

Paper Details	Magnetic Components Technology	Temperature Range	Findings
Gerber et al. [80] (2002)	Ferrite and three powder cores (Molypermalloy, High Flux, and Kool Mu)	93 K to 293 K	Molypermalloy and high flux cores maintained the same inductance across the temperature range. The ferrite had significantly higher losses at 93 K, the other cores remained stable.
Pei et al. [79] (2019)	Low loss non-oriented electrical steel, non-oriented steel with enhanced permeability, grain-oriented electrical steel and nanocrystalline material	20 K to 80 K	Core losses at 21 K was higher than at RT for all the materials examined. The optimal temperature for each material differed. Non-oriented steel with enhanced permeability was found to have a minimum losses at 180 K and Low loss non-oriented electrical steel was a minimum at 131 K. The other materials performed best at RT.
Yin et al. [77] (2021)	Amorphous, nanocrystalline and ferrite	77 K and 298 K	All three cores had an increase in saturation flux density and core loss. Permeability decreased at 77 K. The ferrite suffered a 90% decrease in its permeability and a seven times increase in core loss. A thermal shock test was conducted and found to have no effect.
Wadsworth et al. [78] (2023)	Two nanocrystalline cores and one ferrite	77 K and 298 K	At lower frequencies the change in the relative permeability of the two nanocrystalline cores was similar, at high frequencies one core was found to have a smaller change in relative permeability. All cores had increased saturation flux density at 77 K. One nanocrystalline and the ferrite core had increased hysteresis loss, the other core remained stable.

2.2.3 Gaps in the literature on the topic of power electronic components at CT

Different gate drive IC's have been demonstrated to operate at cryogenic temperatures, while CMOS internal circuitry has been identified as a common factor in the IC that have lowest operating temperature, the cause of the failing IC's has not been identified and a method of constructing a gate driver with a suitable temperature rating has not been presented and remains a gap in the literature.

2.3 Cryogenic Converters

2.3.1 Cryogenic GaN Converters

To date, the design and testing of ten GaN based cryogenic converters have been published. Of those three are a DC/AC inverter topology; a three-level flying-capacitor multi-level inverter [81], and two current-source inverters published by the same author [82], [83]. None of these inverters have been reported to have been tested at cryogenic temperatures with a power greater than 1 kW. The inverters designed in [82], [83] were designed to operate at 20 kVA but were only reported to be tested at 300 W and 950 W at cryogenic temperatures, respectively, thermal limitations being given as the reason for the maximum test power in [82]. This demonstrates the challenges in operating a cryogenic inverter at significant power.

Of the other seven DC/DC converters, three are designed to operate at a power greater than 1 kW and a bus voltage suitable for high power motor drive applications.

The topology of two of these are synchronous-buck converters and the final is a 4-switch buck-boost; both topologies are formed from half-bridges. Although testing a half-bridge in a DC/DC topology allows many conclusions regarding the suitability of the design and the components for an inverter, it is not fully representative. In particular, one switch in the half-bridge when operated as a buck converter will not experience third-quadrant switching. The reported efficiency of a buck converter cannot be translated directly to the expected efficiency of the same half-bridges operated as an inverter, due to the different switching frequency requirements and the asymmetric heat generation in a buck converter.

A 3 kW, 500 V cryogenic GaN half-bridge was designed and tested as a synchronous buck converter Wadsworth et al. [84], [85]. It was cooled by submerging it in liquid nitrogen in [84], and under vacuum on a cryogenic cold-head in [85]. The cold-head facilitated testing as low as 40 K at low power, which was presumably due

to heat dissipation constraints of the cold-head. When submerged in liquid nitrogen the design was thermally limited, the critical heat flux was exceeded limiting the maximum power. The peak efficiency measured was 99.65% with the inductor at room temperature and the GaN transistors submerged in liquid nitrogen. The efficiency was reduced to 99.2% with the inductor also submerged due to increased losses in the core of the inductor.

Two converters are are presented in Wei et al. [71]. A synchronous buck operating at up to 5 kW and a 4-switch buck-boost at up to 2.2 kW. The converters were bolted to a liquid nitrogen cold plate to cryogenically cool them. Using this method, an average temperature of 153 K is measured on the PCB. A maximum efficiency of 98.5% is achieved with the largest reduction in losses believed to be occurring in the air-core inductor, presumably due to the reduced resistance of the copper Litz-wire winding. The converters were tested with a 300 V bus voltage. The paper does not state what limited the power of each converter, although a steep drop in efficiency is shown to occur above 4 kW for the synchronous buck converter.

We consider these two works (Wadsworth et al. and Wei et al.) to be the state of the art for cryogenic GaN power converters targeting high power applications.

2.3.1.1 Cryogenic GaN SSCB

In addition to the GaN converters tabulated in Table 2.6, a GaN solid-state circuit breaker for electrified aircraft applications, capable of breaking a 1 kA fault current, is presented in [86]. The low conduction losses of GaN transistors at cryogenic temperatures without degraded breakdown voltages makes them ideal for this application. This paper is notable for being the first to use 650 V 150 A bare die parts from GaN Systems at cryogenic temperatures. A second T-type SSCB is developed in [87] using lower voltage EPC parts for a lower power application (lunar micro-grid).

2.3.2 Cryogenic Converters Using Si or SiC

A larger number of cryogenic converters have been built with silicon or silicon-carbide transistors; fourteen publications were found that describe a cryogenic converter implemented with either Si or SiC MOSFETs since 2020. The most significant of these for this work were two papers produced by authors from the University of Tennessee, which focus on cryogenic inverters for aircraft propulsion systems.

In Gui et al. (2020) [88] a 40 kVA three-level ANPC inverter using silicon MOSFETs was demonstrated. Series connected Si MOSFETs with an anti-parallel SiC

Table 2.6: Papers discussing cryogenic GaN converters

Paper Details	Power (cont. max demonstrated)	Converter Topology	Power Device Technology	Temperature Range and Cooling Method	Findings
Barth et al. [81] (2020)	1 kW	Three-level FCML Inverter	EPC eGaN-FET HEMT	133 K to 298 K, Cold-plate	150 V bus. Peak efficiency 98.2%. Maximum 16% reduction in losses comparing operation at RT to 213 K.
Büttner et al. [89] (2022)	100 W	Synchronous Buck	100 V GaN Systems HEMT	87 K to 298 K, cooling chamber with forced convection	50 V bus, 100 kHz. Peak efficiency 99.3%. 60% reduction in losses compared to RT.
Hassan et al. [82] (2022)	300 W	2L-CSI	650 V GaN Systems HEMT	77 K	The inverter was designed for 20 kW but paper states thermal constraints prevented testing at power higher than 300 W. Large oscillations in current measurement at switching edges.
Wadsworth et al. [84], [85] (2023)	3 kW	Synchronous Buck	GaN Systems HEMT	77 K to 298 K pool boiling , 40 K to 58 K, vacuum-chamber and cold-head	Losses in GaN switches halved compared to when operating at RT, peak efficiency of 99.6%. A second paper presents results for operation below the temperature of LN2. Lower bus voltage (max. 60 V) used with this cooling configuration. 98% peak efficiency reported. Power limited by cooling capacity of cold-head.

Chen et al. [90] (2024)	100 W	Synchronous Buck	LMG5200 80 V, 10 A half-bridge power stage	123 K to 298 K cryo-chamber	94% peak efficiency is reported. An increase in switching losses at CT and decreased conduction losses reported. Magnetic component's performance was worse at CT
Defaz et al. [74] (2022) , Defaz et al. [91] (2024)	10 W	Flyback	EPC 40 V HEMT	77 K to 298 K Pool boiling	Auxiliary supply for larger cryogenic converter. 5 V to 9 V output. Demonstrates reliable operation of two iterations of the converter at CT. 93% peak efficiency measured. Efficiency increased from 77% (RT) to 81% (CT) at peak power.
Pearce et al. [92] (2024)	17 W	IPT	GaN Systems 650 V HEMT	77 K Pool boiling	Inductive wireless power transfer for HTS motor. Losses lower than modelled.
Hassan et al. [83] (2024)	950 W	2L-CSI	GaN Systems 650 V HEMT	77 K	Appears to be the next iteration of the converter presented in [82] and is also designed as a 20 kW converter. Low power 100 V testing yielded a peak efficiency of 99.2% efficiency at CT compared to 97.5% at RT. Limited information is provided regarding cryogenic operation.
Wei et al. [93] (2022), Wei et al. [71] (2024)	5 kW (buck), 2.2 kW (buck-boost)	Buck and 4-switch buck-boost	GaN Systems 650 V HEMT	153 K to 298 K Cold-plate	Peak 98.5% efficiency, 300 V bus voltage. Cooled using cooling plate flowing LN2.

SBD were used to overcome issues caused by the large reverse recovery charge of the super-junction MOSFETs. A peak efficiency of 98% was measured at 75% of the rated power. This system was a scaled down test for an envisaged 1 MW motor drive.

The second paper, Chen et al. [94] (2020) presents a 1 MW inverter, comprised of 2-interleaved 3-level ANPC inverters. In this system, SiC power modules are used, which have an optimal temperature of 275 K. To achieve this junction temperature, nitrogen gas was chilled by flowing it through a liquid nitrogen reservoir before passing it through the power modules cold plates. The input and output EMI filter inductors were cooled using liquid nitrogen directly, maximising the reduction in the resistance of the copper windings. The paper concludes that the system operated as intended and that the cooling methodology shows potential. This final work [94] represents the state of the art in the field of cryogenically cooled aircraft propulsion motor drives. It achieved a peak efficiency of 99.3% with a reported specific-power of 18 kVA/kg. The inverter was rated to 1 MW continuously. GaN power modules suitable for the power requirements were unable to be sourced, hence the decision to use SiC power modules. The paper does not comment on system reliability and acknowledges with the current design, the motor drive does not demonstrate an improved specific power compared to comparable non-cryogenic systems. This may be because the decrease in $R_{\mathrm{ds(on)}}$ is only 1.32 times, which is small compared to the potential 8 times reduction possible with GaN transistors. Suggesting further improvements in power density and efficiency should be possible in the future if suitable GaN power modules become available.

2.3.3 Cryogenic Cooling Methods for a Converter

There are a number of methods to cryogenically cool a converter. Methods that have been used in the literature include:

1. Attaching the converter to a cold-plate with:
   (a) flowing liquid nitrogen [81], [88]
   (b) a flow of chilled nitrogen gas [71], [94]
2. Submerging the converter in a pool of liquid nitrogen [84], [91], [92]
3. Placing the converter in a cryo-chamber [67], [90]. A cryo-chamber is a thermal chamber that uses either gaseous or liquid nitrogen from a connected dewar to chill the enclosed environment.

4. Attaching the converter to a cryogenic cold-head [85]. A cold-head (or cryo-cooler) is a mechanical device that generates cryogenic temperatures using a refrigeration cycle. Typically, this is either a Joule-Thomson cycle or a Gifford-McMahon cycle with helium as the working fluid.

The lowest temperatures can be achieved with a cold-head, but the heat dissipation capability of the cold-head seems to limit the converter power in [85]. Direct submersion in liquid nitrogen appears to achieve the lowest temperature differential between the transistors and the liquid nitrogen, it is also the simplest to implement. The open pool of nitrogen presents challenges for the converter design, requiring that all aspects of the converter remain functional when in close proximity to the pool of low temperature boiling liquid [68]. A cooling plate with flowing liquid nitrogen does not result in junction temperatures as low as direct submersion in the liquid nitrogen, although it is more representative of a motor drive cooling circuit.

2.3.4 Gaps in the literature concerning cryogenic converters

A number of outstanding gaps remain on the topic of cryogenic converters:

1. A cryogenic GaN inverter has not been tested to a power greater than 1 kVA despite thirteen papers published on the topic of high power transistors. It remains an open question if a cryogenic inverter with a power rating suitable for an aircraft motor drive can be operated.

2. Testing of a high power cryogenic GaN inverter have been attempted [82], the reason that higher power result are stated to be thermal. It is unknown if with a sufficient thermal design a higher power cryogenic GaN inverter is possible or if other failure modes exist that prevent the development of one.

3. A basic loss model of a cryogenic converter is given in [84]. But this model which does not account for the variation in $R_{\mathrm{ds(on)}}$ with temperature is insufficient to predict the performance of a cryogenic inverter. A model that couples junction temperature and temperature-dependent losses would be a contribution to the literature and also are relevant to system analysis of liquid hydrogen fuelled aircraft such as that in [3] where fixed values for efficiency are used

4. A method to measure the losses using calorimetry at cryogenic temperatures has not been seen in any of the publication on cryogenic converters to date. Demonstrating a cryogenic calorimetric loss measurement technique suitable for

inverters would be valuable contribution as it allows electrical measurements to be validated and can be more accurate [95].

Chapter 3

Characterisation of a GaN HEMT at Cryogenic Temperature

This chapter describes the characterisation of top-cooled GaN Systems transistor that was conducted at cryogenic temperatures. In the first half of this chapter, Section 3.1, a method for measuring the on-state resistance at cryogenic temperatures and a characterisation of this property are discussed. The results are presented for an extended range of currents beyond the rating of the transistor and compared to the existing literature. The transistor is operated at high current densities (in excess of the room temperature rating of the transistor) to determine the effect of large thermal loads and determine the failure mechanism at cryogenic temperatures. In the second half, Section 3.2, the switching performance and switching losses of the transistor are characterised. As well as being a significant source of loss in a power transistor, transistor switching involves the fast commutation of current and voltage transients that can cause transistor failure. A good understanding of the switching behaviour at cryogenic temperature is therefore imperative to building a cryogenic GaN inverter as described in later chapters.

3.1 Static Characterisation

The contents of Section 3.1 was presented as a conference paper at the 2023 IEEE Energy Conversion Congress and Exposition (ECCE) [7].

The research conducted in section 3.1 was conducted with the aim of addressing the following research questions introduced in Chapter 1:

1b. *What improvements in efficiency and peak power can be achieved by cryogenically cooling a GaN inverter compared to a conventionally cooled GaN inverter for aircraft propulsion applications?*

2a. *Does large heat generation in the transistor junction and resultantly large temperature gradients across the transistor package degrade the performance of a GaN HEMT at cryogenic temperatures, and what determines the maximum thermal dissipation of the transistor at cryogenic temperatures?*

2b. *Do new mechanisms lead to failure for a GaN transistor at cryogenic temperature or are conventional failure modes exacerbated by the change in the properties of the GaN transistor at cryogenic temperatures?*

As highlighted in the literature review, the on-state resistance of GaN HEMTs decreases with falling temperatures, with results published at temperatures as low as 4 K (−269.15 °C). At 150 K (−123 °C), the $R_{\mathrm{ds(on)}}$ has been observed to fall to approximately 20% of its value at room temperature [40], [52], [57], [58].

The conduction losses in a power converter are directly proportional to the on-state resistance, $R_{\mathrm{ds(on)}}$, of its constituent switches. For most converters, conduction losses will constitute a significant proportion of a converter's losses.

This section includes investigation of the behaviour of GaN HEMT $R_{\mathrm{ds(on)}}$ at currents exceeding the room-temperature rated current, which is a under explored topic in the literature. Continuous operation at high current is possible with a cryogenic junction temperature due to the reduced $R_{\mathrm{ds(on)}}$, which leads to lower heat generation for a given current. The extent to which it is possible to increase the transistor current is an important consideration when answering question 1b. Questions 2a. and 2b. are inherently investigated as a result of operating the transistor to its operating limits at cryogenic temperatures with large conducted currents.

To thoroughly assess the $R_{\mathrm{ds(on)}}$ behaviour, two experiments are conducted. First, standard laboratory equipment and small quantities of liquid nitrogen (LN2) are used to deliver short-duration pulse currents to a GaN HEMT that has been cooled to cryogenic temperatures. The short current pulses (10 µs) result in a negligible rise in junction temperature. This experiment allows for accurate measurement of the $R_{\mathrm{ds(on)}}$ over a range of junction temperatures below room temperature.

In the second experiment, a current is passed through a GaN HEMT that is heat-sunk to an LN2 reservoir, and the resulting $R_{\mathrm{ds(on)}}$ is measured. This experiment aims to assess the effects of high temperature-gradients across the package and to determine if the parametrisation of $R_{\mathrm{ds(on)}}$ found in the pulsed current experiment is valid under these conditions. The current is increased to the point of thermal failure,

and a possible failure mode is modelled to demonstrate that it is consistent with our understanding of thermal instability.

3.1.1 Cryogenic Characterisation Using Current Pulses

3.1.1.1 Setup

In order to characterise the GaN Systems GS66508T HEMT at cryogenic temperatures, liquid nitrogen was used as a coolant.

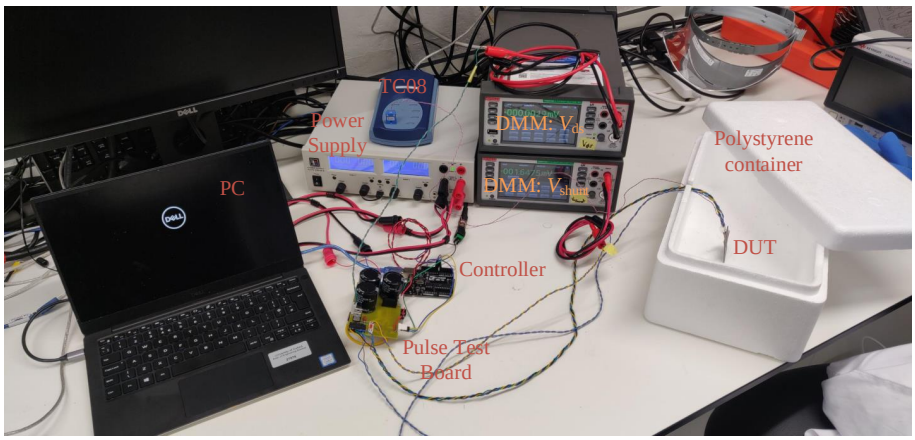


Figure 3.1: Photo showing the test setup. A python script run on the PC automates the test, controlling the power supply voltage and triggering the current pulses. It stores the measurements made with the TC08 thermocouple data-logger and two digital multimeters.

A shallow pool of LN2, approximately 1 cm in depth is poured into a polystyrene container, and the transistor (soldered to a PCB) is placed vertically into the fluid, partially submerging the board. As the LN2 evaporates, the level of the LN2 in the container falls, exposing more of the PCB to the nitrogen gas above the fluid. Once the LN2 has completely evaporated, the heat leak and thermal inertia of the components in the setup cause the temperature of the DUT to gradually rise until it reaches room temperature.

Due to the slow rate of temperature increase, two assumptions can be made. Firstly, the temperature distribution through the DUT can be assumed to be uniform because the small heat fluxes associated with the gradual warming of the apparatus have a negligible effect. Second, during the short current pulses of 10 µs, the temperature rise of the junction is negligible. These assumptions allow the temperature of the DUT to be considered quasi-static for the duration of the characterisation at each temperature. By waiting a sufficient time between measurement pulses, the DUT can

be tested over a range of temperatures at regular intervals. It was found a temperature range of −196 °C to 15 °C was easily achievable using this method. The junction temperature is plotted in Fig. 3.2 at three scales to show the changes in temperature over the course of the test.

The cold evaporated nitrogen gas is heavier than the ambient room temperature air so fills the internal volume of the container. The container is covered with a lid to prevent the disturbance of the gas in the container. Disturbing the gas causes the introduction and mixing of room temperature air with the cold nitrogen gas. The room temperature air is up to 223 K hotter than the nitrogen gas which evaporates at 77 K, if mixing occurs the rate of temperature increase of the DUT significantly increases, potentially voiding the two assumptions described previously. The lid is loosely fitted, allowing the evaporated nitrogen gas to vent. This prevents a potentially hazardous build-up of pressure in the container due to the expansion of the LN2 as it evaporates.

The cold nitrogen gas does not contain water vapour and is heavier than air so occupies the container volume, this prevents condensation forming on the DUT, which might otherwise result in short-circuits.

A Cauer network describing the thermal impedances of the transistor from the datasheet was used to model the transistor's temperature response to a heat input. By combining this model with approximate values for the $R_{\mathrm{ds(on)}}$ of the transistor, taken from the on-state resistance measurements made in [58], a suitable duration for the current pulse was determined. It was shown that for a 10 µs pulse of 100 A at 100 K a 2 K temperature increase would occur in the transistor junction. This was deemed to be an acceptable deviation from the ideal static temperature measurement, and a pulse duration of 10 µs was used throughout. A graphical representation of the temperature profile can be seen in figure 3.2.

The temperature of the DUT was measured using a Pico TC08 Thermocouple Data Logger with a bare-wire T-type thermocouple adhered directly to the top-side thermal pad of the DUT using Electrolube TBS20S adhesive. The TC08 datalogger has a 0.025 K resolution for measurement ranges down to 23.15 K when using T-type thermocouples. As mentioned previously, the small heat fluxes allow the temperature measured by the thermocouple to be assumed equal to the junction temperature of the transistor.

The components of the gate drive circuit, as with most electrical components, are not rated to cryogenic temperatures. To ensure that these components remained functional, the gate drive for the DUT was assembled on a separate board. The

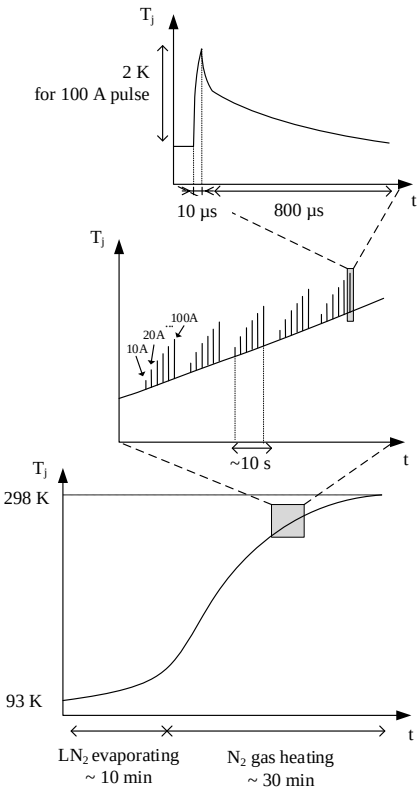


Figure 3.2: Stylised plots of junction temperature at three different levels of magnification.

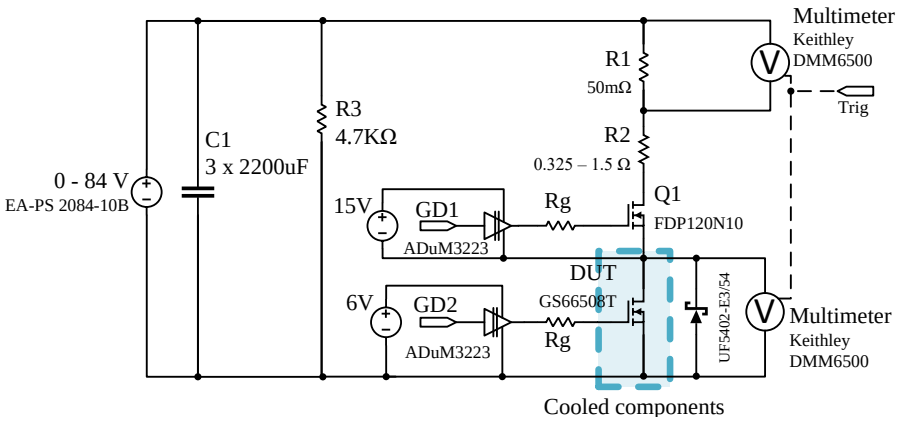


Figure 3.3: Circuit schematic for the pulse test. Only the DUT was cooled to cryogenic temperatures. Q1 was used to deliver current pulses to the DUT, the magnitude of which was controlled by the voltage applied to C1 and the resistance of R2. The current was measured using the sense resistor R1.

gate driver board was placed next to the container of LN2 and remained at room temperature.

The DUT was placed in the pool of LN2 and allowed to cool to its minimum

temperature, the test was then initiated. Each time the temperature has increased by a pre-determined increment, a set of measurements are recorded. Each set is collected by stepping the bus voltage across a set range. At each voltage set-point a current pulse is delivered to the DUT, the magnitude of which increases with the applied bus voltage.

3.1.1.2 Results

Fig. 3.4 is an example of the measured data. The steady-state voltage and current measurement points are averaged and the values are used to calculate the $R_{\mathrm{ds(on)}}$ of the transistor.

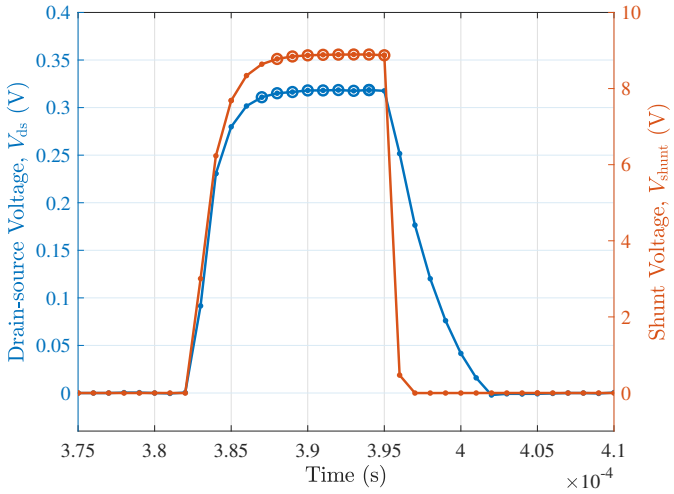


Figure 3.4: Plot of the drain-source voltage and current shunt voltage for a 23.8 A current pulse at 151 K. Steady-state measurement points are marked with circles.

$R_{\mathrm{ds(on)}}$ shows only a weak variation due to the drain-source current within the rated current range (≤ 30 A). Fig. 3.5 shows the on-state resistance across a range of drain-source currents, plotted against the junction temperature. The datapoints collected in the experiment do not lie on a perfect grid of temperature and current, to allow the data to be visualised the curves in Fig. 3.5 are transects of the interpolated $R_{\mathrm{ds(on}}(T_{\mathrm{j}}, I_{\mathrm{d}})$ surface at selected values of drain-source current. The individual datapoints are those measured within ± 4 A of the I_{d} value of each curve.

Plotting $R_{\mathrm{ds(on)}}$ against the junction temperature allows comparison to the $R_{\mathrm{ds(on)}}$ measurements in [96] and the datasheet [97], as shown in Fig. 3.6. It was found the room temperature $R_{\mathrm{ds(on)}}$ of the GS66508T transistors sampled were between 4.1 % to 8.2 % less than the datasheet value. To account for this variation, the measured

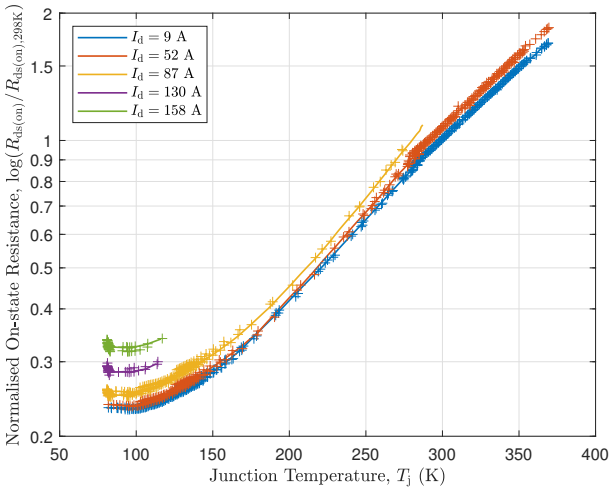


Figure 3.5: Log plot of $R_{ds(on)}$ against junction temperature, curves for 9 A to 158 A are shown for comparison. The y-axis is normalised to the measured on-state resistance at 298 K, 9 A (40 mΩ). Pulses above 90 A were only performed at low temperatures.

results are normalised by the transistor's room temperature $R_{ds(on)}$. It is believed this variation in $R_{ds(on)}$ is due to variation in the manufacturing process. After normalisation, there is good agreement between the experimental data reported in this thesis and the results from previous literature. There is a mean absolute error of 1.1 mΩ between the measurements in this work and [96], over the temperature range for which both report data. Measurements were compared for a 40 A current magnitude as reported by [96]. It should be noted that the data from [96] was extracted from a figure, introducing a possible source of error. Building upon the results presented in [96], this thesis presents results for a range of test currents, including values that exceed the room temperature current rating of the transistor (30 A), up to 110 A.

With reduced $R_{ds(on)}$ at cryogenic temperatures, increased operating currents are possible. Over the entire temperature range, the resistance was measured with current pulses up to 90 A. To examine the very high current behaviour of the transistor at cryogenic temperatures, current pulses were applied up to 158 A (five times the transistor's room temperature rating) at the lowest temperature that could be reached with the experimental setup. The result of this can be seen in Fig. 3.7.

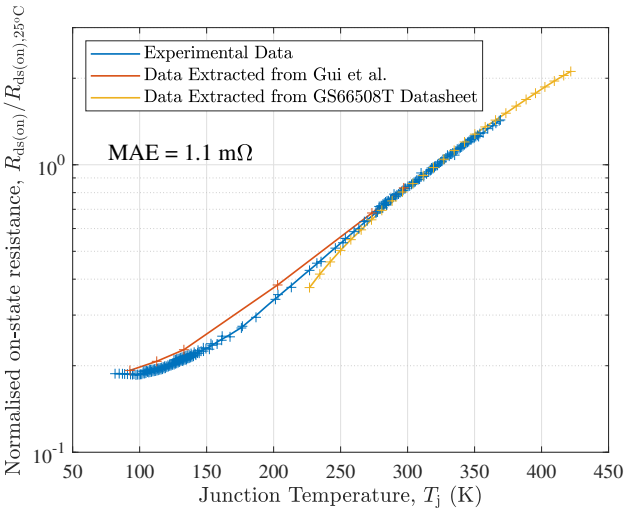


Figure 3.6: Plot of $R_{\mathrm{ds(on)}}$ against junction temperature, comparing experimental data reported in this paper against data extracted from Gui et al. [96] and the transistor's datasheet. Results normalised to datasheet $R_{\mathrm{ds(on)}}$ at 298 K, 9 A (50 mΩ).

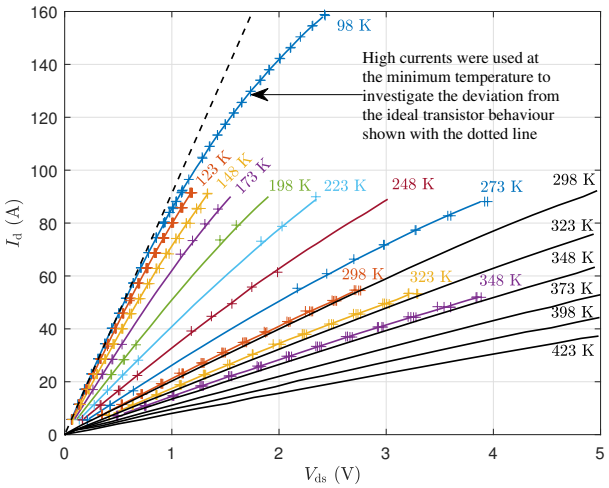


Figure 3.7: V_{ds} vs I_d plots across the temperature range with currents up to 158 A. Black lines show data extracted from the manufacturer's datasheet, coloured lines are calculated using transects of interpolated $R_{\mathrm{ds(on}}(T_j, I_d)$ experimental data. The datapoints are the points that lie within ±2 K of the temperature value associated with the transect.

3.1.2 Cryogenic Characterisation at Thermal Equilibrium

3.1.2.1 Experimental setup

The objective of the second experiment was to examine the $R_{\mathrm{ds(on)}}$ behaviour under high power dissipation at cryogenic temperatures. In previous work and in the experiment described in Section 3.1.1, short-duration currents in a double pulse test or low-current measurements using a curve tracer [52], [57], [58], [96] are used to measure $R_{\mathrm{ds(on)}}$. It is unknown if this is sufficient to properly characterise the transistors for operational use as the effects of the temperature gradient between the junction and casing due to self-heating are not considered.

In this work, a continuous controlled current was passed through the transistor, which was thermally and mechanically attached to a heat sink by the top-side thermal pad. The assembly was then submerged in a pool of liquid nitrogen. This can be seen in Fig. 3.9. I_{d} was increased in steps of 1 A with sufficient time between steps to reach thermal steady-state. From measurements of V_{ds} and I_{d}, $R_{\mathrm{ds(on)}}$ was calculated.

The same GaN Systems HEMT as used in the previous test, a GS66508T, was used as the DUT. It was continuously gated on with a 6 V supply and the test current, I_{d}, was supplied by a EA PSB 9500-90. The current was measured using a 1 mΩ current shunt. v_{ds} and the shunt voltage were measured using a Pico Tech ADC-20 datalogger with kelvin connections. This is drawn in 3.8.

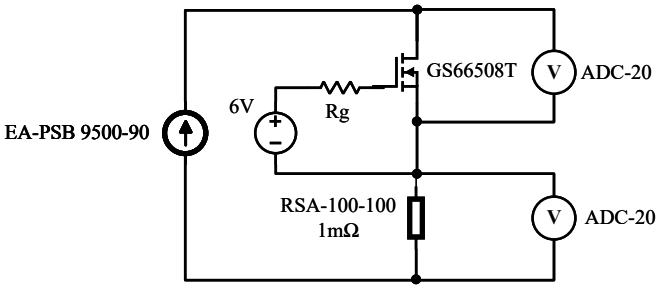


Figure 3.8: Electrical circuit diagram of the test setup used for the continuous current experiment.

The test apparatus, shown in Fig. 3.9, was designed with the bottom side of the transistor soldered to a small PCB to make the electrical connections. The connection between the top-side thermal pad and the copper heat sink, which is subject to large thermal gradients, was made using indium-tin solder which acted as thermal interface material (TIM). Indium-tin solder was selected due to the softness and ductility of the metal both at room-temperature and cryogenic temperatures, which reduces the

mechanical stress on the transistor due to mismatches in CTE and large temperature changes. The indium-tin alloy was found to have superior wetting performance than pure indium and was used to help prevent poor solder joints.

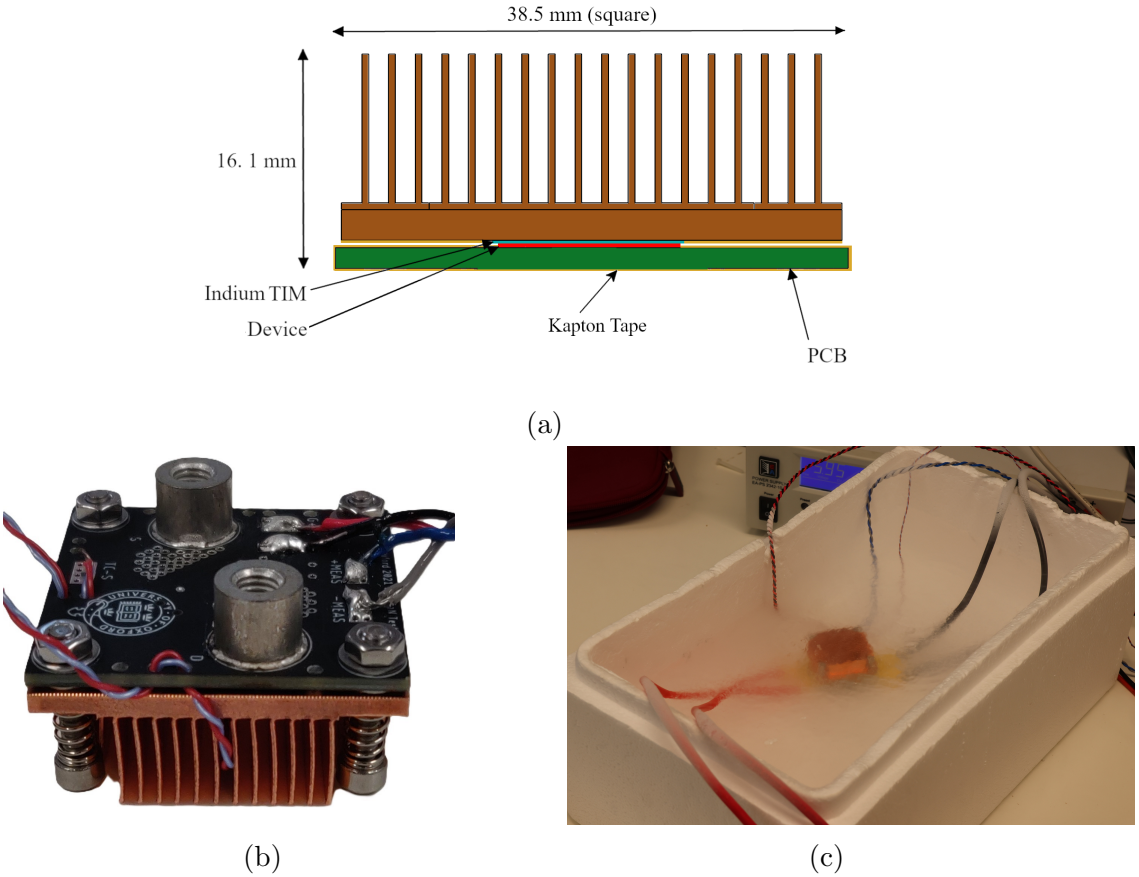


Figure 3.9: Images of the continuous current test assembly. (a) Cross-section of the assembly. (b) Photo of heatsink and PCB assembly, no kapton tape was applied in this early iteration of the assembly. (c) Photo of the heat sink and transistor assembly in a pool of liquid nitrogen during an extended duration current test.

3.1.2.2 Thermal equilibrium characterisation results

The test was repeated with five test articles (DUT 1–5), the results of which are plotted in Fig. 3.10. The y-axis is normalised to the datasheet value for $R_{\mathrm{ds(on)}}$ at 298.15 K (25 °C) given in the datasheet (50 mΩ). A monotonically increasing $R_{\mathrm{ds(on)}}$ was observed as the current was increased due to the greater power being dissipated in the device which led to a rising steady-state temperature. It should be noted that the measured room temperature $R_{\mathrm{ds(on)}}$ was significantly less than reported in

the datasheet: the five test DUTs had a mean $R_{ds(on)}$ of 42 mΩ, 16% less than the datasheet value.

The $R_{ds(on)}$ at cryogenic temperatures agree with the pulsed current measurements. These measurements also show that the transistors not only had a greatly reduced $R_{ds(on)}$ at cryogenic temperatures but that this was maintained with significant heat generation. A steady-state condition was reached for currents up to 3.1 times the DUT datasheet current rating.

Transistor failure occurred when the current was stepped beyond a critical point. All the transistors failed open-circuit. This occurred despite the estimated junction temperature, prior to failure, being well below room temperature. The resultant spike in drain-source voltage can be seen in Fig. 3.11 for DUT 3 which occurred when I_d was increased beyond 90.5 A. The temperature of the junction is estimated by calculating the on-state resistance and using the data plotted in Fig. 3.5 as an interpolated lookup table for junction temperature.

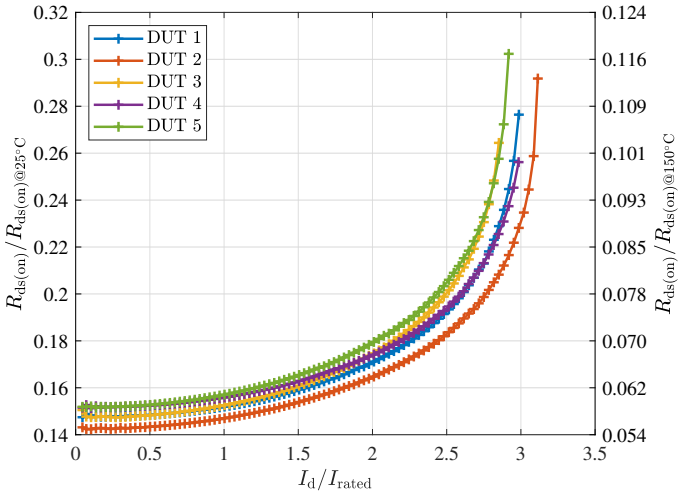


Figure 3.10: Steady state on-state resistance against current with the x-axis normalised to the rated current (30 A), the y-axis is normalised to the datasheet on-state resistance at 298.15 K (25 °C), 9 A (50 mΩ).

The results of the five repeated tests are tabulated in Table 3.1. The failure current was repeatable with a maximum deviation of 5% from the mean of 89.3 A.

3.1.2.3 Thermal failure analysis

Three failure modes were considered:

1. CTE mismatch causing mechanical failure, possibly exacerbated by low-temperature induced brittleness of the materials in the transistor,

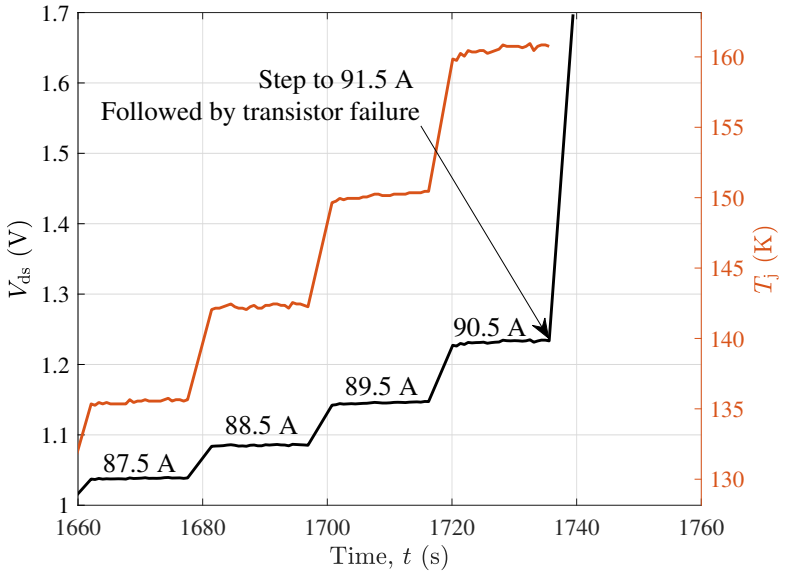


Figure 3.11: DUT 3's voltage and junction temperature against time during a continuous current experiment. At 1735 s the current was increased to the next step-point and failure occurred.

Table 3.1: Current, heat generation, and junction temperature at failure.

DUT	$R_{ds(on)@293.15\,K}$ (mΩ)	I_{fail} (A)	Q_{fail} (W)	Estimated $T_{j,fail}$ (K)
4	43.7	85.5	96.7	155.85
5	42.5	87.5	116	179.05
1	42.1	89.6	111	169.05
3	40.9	90.5	112	170.35
2	41.8	93.4	127	176.55

2. thermal instability, leading to thermal runaway,

3. unmodeled electrical behaviour at high current densities and/or low temperatures.

Here the second proposed cause of failure, thermal instability, is examined. This is where a positive feedback loop is created between the heat generation and junction temperature. The junction temperature increases until the excessive temperature damages the die and/or the packaging, causing the DUT to failure.

The thermal limit of a transistor, for room temperature applications, is the largest I_d current that can conducted without exceeding the maximum rated junction temperature, $T_{j(max)}$. This limit can be calculated from parameters provided in the man-

ufacturer's datasheet for the junction to casing thermal resistance, $R_{\mathrm{j-c}}$, and the thermal resistance between the casing and ambient, $R_{\mathrm{c-a}}$. These can be used to solve Eq. 3.1.

$$I_{\mathrm{d(max)}} = \sqrt{\frac{T_{\mathrm{j(max)}} - T_{\mathrm{a}}}{R_{\mathrm{ds(on)},\mathrm{T_{j(max)}}} \left(R_{\mathrm{j\text{-}c}} + R_{\mathrm{c-a}}\right)}} \tag{3.1}$$

For an LN2 cooling system, the $\Delta T_{\mathrm{j(max)-a}}$, where $T_{\mathrm{a}} = 77.15\,\mathrm{K}$, is 2.8 times larger than the temperature differential between $T_{\mathrm{j(max)}}$ and room temperature ambient. Very naively it could be assumed, therefore, that the increase in rated current is a factor of $\sqrt{2.8}$. Later in this section, it is shown that for a practical cooling design, the point of thermal instability is reached at a temperature much lower than the maximum rated junction temperature. Therefore, the maximum rated junction temperature is irrelevant when cooling with a cryogenic fluid, and Eq. 3.1 is no longer applicable. Currents greater than $\sqrt{2.8} I_{\mathrm{d(max)},298.15\,\mathrm{K}}$ are in fact possible due to the lower $R_{\mathrm{ds(on)}}$ than assumed in Eq. 3.1.

3.1.2.4 Thermal resistance

To analyse the thermal stability of the continuous-current setup, the thermal resistance between the junction and the liquid nitrogen was estimated.

First, the junction temperature was inferred by comparing the resistance measured to the results presented in Section 3.1.1. Good temperature estimates can only be made when sufficiently high heat is dissipated, as at the lowest temperatures the rate of change of $R_{\mathrm{ds(on)}}$ with respect to T_{j} is small, making the estimate very sensitive to small errors in the measured $R_{\mathrm{ds(on)}}$.

The thermal resistance can then be calculated as $R_{\mathrm{th}} = (T_{\mathrm{j,est}} - T_{\mathrm{LN2}})/Q_{\mathrm{dis}}$, the result of which is plotted in Fig. 3.13. The final value of the thermal resistance (circled on the figure) gives the $R_{\mathrm{th,fail}}$ used to calculate the point of thermal instability for each DUT.

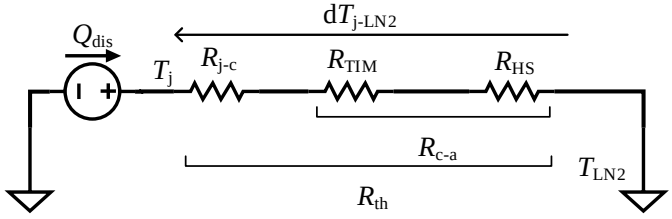


Figure 3.12: Thermal circuit showing the thermal resistances incorporated into R_{th}.

Due to the large finned area of the heat sink in contact with the fluid, the thermal resistance at the copper/fluid boiling interface can be assumed to be negligible. The total thermal resistance will be dominated by the package thermal resistance and the thermal resistance of the TIM, $R_{\mathrm{HS}} << R_{\mathrm{j-c}} + R_{\mathrm{TIM}}$. The three materials in the thermal path, GaN, Si (the transistor is a GaN-on-Si HEMT), and copper all have increased thermal conductivity at cryogenic temperatures as shown in Fig. 3.14. This explains the trends observed in Fig. 3.13 with increasing thermal resistance as the junction temperature increases.

There appears to be vertical offsets between the R_{th} curves plotted in Fig. 3.13, this is most likely due to variation in the quality of the solder joint made between the thermal pad and the heatsink. Significant care was made to ensure repeatability of this process as inspection of the solder joint after assembly was not possible.

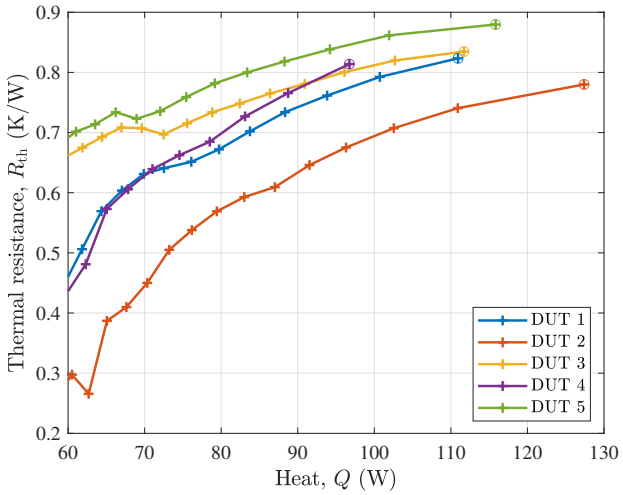


Figure 3.13: Estimated thermal resistance using inferred junction temperature and heat dissipated ($Q = V_{\mathrm{ds}} I_{\mathrm{d}}$).

DUT	$R_{\mathrm{ds(on)},293.15\,\mathrm{K}}$ (mΩ)	$R_{\mathrm{th,fail}}$ (K/W)
4	43.7	0.813
5	42.5	0.880
1	42.1	0.823
3	40.9	0.834
2	41.8	0.780

Table 3.2: Measured room temperature $R_{\mathrm{ds(on)}}$ and $R_{\mathrm{th,fail}}$ as plotted in Fig. 3.13.

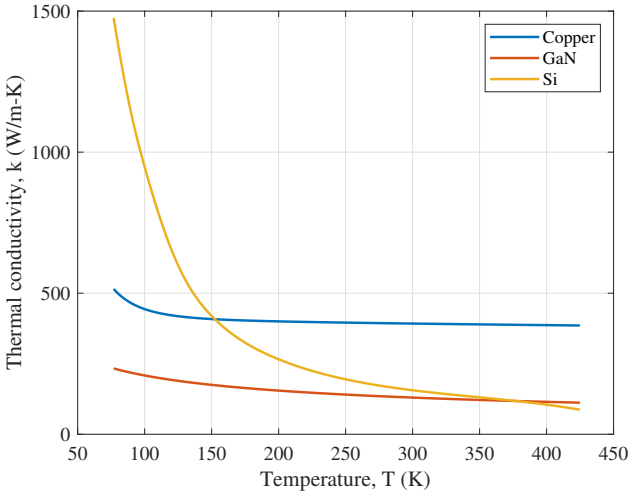


Figure 3.14: Thermal conductivity of transistor materials [98], [99], [100]

3.1.2.5 Stability conditions

In thermal steady-state, the generated heat is equal to the dissipated heat.

$$Q_{\text{gen}}(T_{\text{j}}) = Q_{\text{dis}}(T_{\text{j}}) \tag{3.2}$$

Equivalent to:

$$I_{\text{d}}^2 R_{\text{ds(on)}}(T_{\text{j}}) = \frac{T_{\text{j}} - T_{\text{LN2}}}{R_{\text{th}}(T_{\text{j}})} \tag{3.3}$$

Where $R_{\text{th}}(T_{\text{j}})$ is the temperature dependent total thermal resistance between the junction and ambient. An operating point is thermally stable if it satisfies Eq. 3.2 and the inequality:

$$\left.\frac{\mathrm{d}Q_{\text{gen}}}{\mathrm{d}T_{\text{j}}}\right|_{T_{\text{j}}} < \left.\frac{\mathrm{d}Q_{\text{dis}}}{\mathrm{d}T_{\text{j}}}\right|_{T_{\text{j}}} \tag{3.4}$$

Assuming a simple thermal resistance to ambient:

$$\left.\frac{\mathrm{d}Q_{\text{gen}}}{\mathrm{d}T_{\text{j}}}\right|_{T_{\text{j}}} < \frac{1}{R_{\text{th}}(T_{\text{j}})} \tag{3.5}$$

A plot showing the heat dissipation and generation for three I_{d} currents against junction temperatures is shown in Fig. 3.15. It can be seen that a thermally stable system has two equilibria, one stable equilibrium and one unstable equilibrium. At the onset of instability, a single unstable equilibrium point will be calculated where

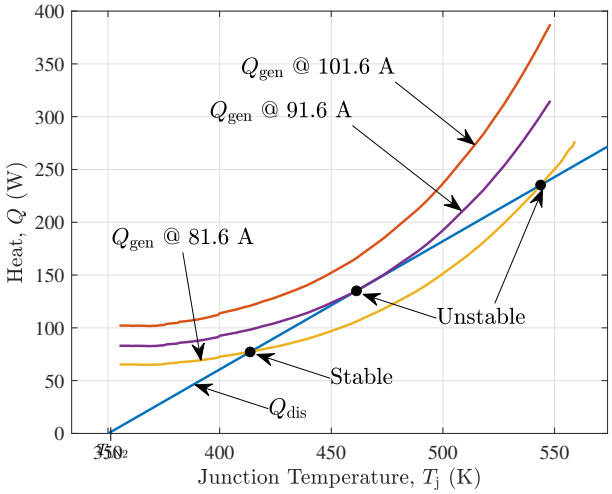


Figure 3.15: A plot showing the generated and dissipated heat power against junction temperature for DUT 1. Three cases are shown: stable, unstable and the onset of instability.

the heat generation and dissipation are balanced. A completely unstable system has no equilibrium points.

The current at the onset of instability can be calculated by rearranging Eq. 3.3 for I_d, which unlike Eq. 3.1 is a function of T_j. The maxima of this function gives the drain-source current and the junction-temperature at which the onset of instability occurs.

This calculation is performed for each DUT using the thermal resistances and room temperature $R_{ds(on)}$ measured in section 3.1.2.4.

DUT	I_{fail} (A) predicted/ measured	Q_{fail} (W) predicted/ measured	$T_{j,fail}$ (K) predicted/ estimated	$R_{ds(on),fail}$ (mΩ) predicted/ measured
4	90.5 / 85.5	136.7 / 96.7	188.29 / 155.85	16.7 / 13.2
5	88.2 / 87.5	126.3 / 116	188.29 / 179.05	16.2 / 15.1
1	91.6 / 89.6	135.0 / 111	188.29 / 169.05	16.1 / 13.8
3	92.3 / 90.5	133.3 / 112	188.29 / 170.35	15.6 / 13.6
2	94.5 / 93.4	142.5 / 127	188.29 / 176.55	16.0 / 14.6

Table 3.3: Calculated and measured failure current, generated heat, temperature and on-state resistance.

Table 3.3 compares the model predictions with the measured data. The predicted thermal current limit is approximately three times greater than the datasheet's rated

current for the GaN Systems GS66508T [97]. It is important to note that the measured values are recorded at the set-point prior to failure and should therefore be less than the predicted values. It can be seen in Fig. 3.10 that the rate of change of $R_{\mathrm{ds(on)}}$ with respect to current just prior to failure is very large and as such the significant difference between the measured pre-failure $R_{\mathrm{ds(on)}}$ and predicted $R_{\mathrm{ds(on)}}$ at failure is reasonable. This in turn gives rise to the much larger Q at failure compared to that measured at the proceeding set-point.

The relatively good agreement between the predicted and measured failure currents suggests that thermal instability is the cause of the transistor failures in Section 3.1.2.

3.2 Switching Loss Characterisation

In the first half of this chapter, the on-state resistance and resultant conduction losses of a GaN Systems GaN HEMT were characterised at cryogenic temperatures. In this second section, the switching performance and switching losses of the transistor are explored, which is the other significant source of loss in a power transistor.

Analysing the switching performance may yield potential failure mechanisms contributing to answering research question 2b: *Do new mechanisms lead to failure for a GaN transistor at cryogenic temperature or are conventional failure modes exacerbated by the change in the properties of the GaN transistor at cryogenic temperatures?* While measuring the switching losses directly answers research question 1a: *How are switching losses of a GaN HEMT affected by cryogenic temperatures?*

An experimental setup was developed to conduct systematic characterisations of four power transistor technologies at room temperature and elevated temperatures. This work was a collaborative effort to which the author was a major contributor resulting in the publication of "A Comparison of the Hard-Switching Performance of 650 V Power Transistors With Calorimetric Verification," published in the *IEEE Open Journal of Power Electronics*, 2023. The author was primarily responsible for, in collaboration with other authors, the design and implementation of the apparatus to control the junction temperature, data collection and processing, as well as writing of the text and producing figures. In this section, the continuation of this work conducted by the author is detailed; examining a GaN HEMT at cryogenic temperatures with modified hardware. The modified hardware is used to make measurements of the switching waveforms and calculate the switching losses at reduced temperatures. A brief description of the test platform is taken from the cited paper.

The experimental apparatus was modified to cool the DUTs to sub-ambient temperatures whilst keeping the measurement circuits above 250 K. Measurements of the switching edges were made for temperatures down to a minimum of 140 K.

In Section 3.1 the smaller 30 A rated GS66508T transistor was characterised to reduce the required currents to induce failure. In this section, the larger 60 A GS66516T transistor is characterised.

3.2.1 Test Platform

A detailed description of the test platform is provided in the journal publication. The key points relevant to this section are quoted below [101]:

"A high-level schematic and block diagram of the test platform is shown in Fig. 3.16. The core of the system is a half-bridge switching cell comprising a tightly coupled DC link capacitor, two transistors and a current sense resistor, mounted on a PCB. This PCB also mounts isolated gate drivers, three high-bandwidth measurement channels, and supporting power supply circuitry as shown in Fig. 3.17."

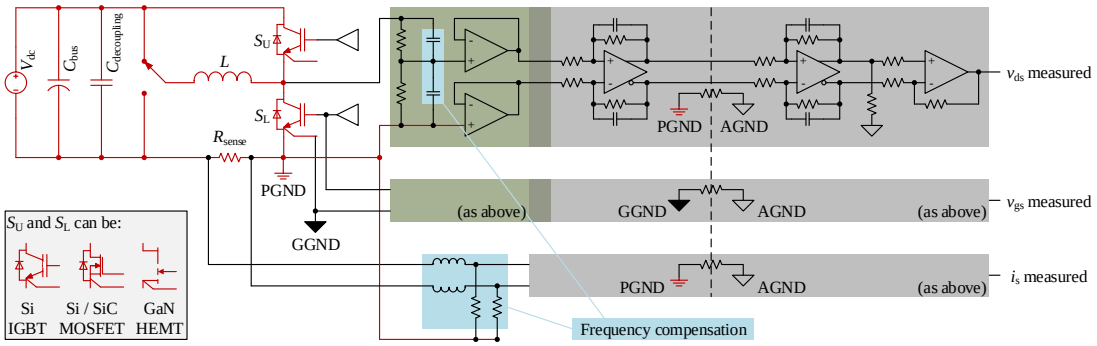


Figure 3.16: Schematic of the test platform showing power (red) and signal (black) chains [101].

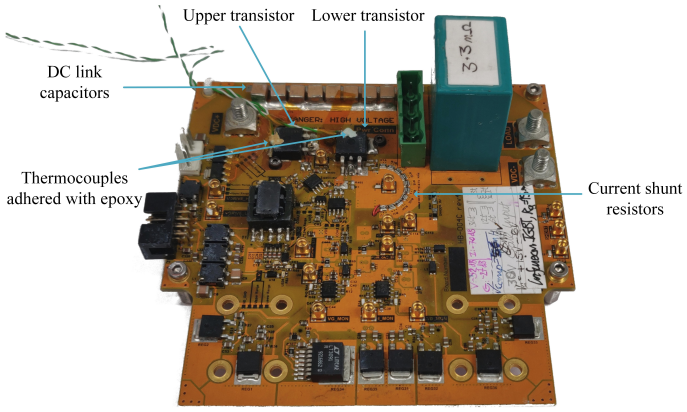


Figure 3.17: Photograph of the PCB with D2PAK transistors mounted [101].

"The gate drive circuits are built around the SI8271GB-ISR, a fast isolated silicon driver, capable of delivering up to 4 A gate current and providing transition times of ~ 10 ns. It provides internal isolation for the gate control signal path."

"Importantly, the gate drive power supply voltage is adjustable, allowing the same gate driver circuit to be adapted using selector links to set the off-state drive voltage, relative to the Kelvin source pin. The voltage

can be set to either zero or a negative level that is approximately equal to, or one-third of, the magnitude of the positive on-state level (e.g., +6 V and −2 V, or +6 V and −6 V)."

"The test platform PCB integrates three high-bandwidth measurements:

- The source current (i_s) in the lower transistor, by measuring the voltage across the current sense resistor.
- The drain-source voltage (v_{ds}), measured across the lower transistor using a high-voltage potential divider.
- The gate-source voltage (v_{gs}), measured across the gate and Kelvin source connections of the lower transistor.

The outputs of all the measurement channels are fed directly to a 1 GHz, 12.5 GS s^{-1}, 12-bit Tektronix MSO44 oscilloscope using length-matched 50 Ω coaxial lines and 50 Ω termination."

Given the close proximity of the gate driver IC and the power circuit, the SI8271 gate driver must be able to tolerate temperatures close to the recorded transistor temperature. In the literature mixed performance has been reported for this gate driver at cryogenic temperatures below 130 K [54], [73], [82], but there is consensus that the gate driver functions above this temperature.

3.2.2 Thermal Design

For the elevated temperature tests in [101] an external heater was used to maintain the lower transistor at a temperature above ambient during the test cycle. The heater was inserted into a copper mount, shown in Fig. 3.18, which is soldered directly to the thermal pad. The thermal pad is connected internally to the source pad and so the mount is at a fixed potential and does not require electrical isolation.

For the cryogenic tests both transistors were cooled by mounting two independent aluminium blocks to the thermal pads on the backside of the PCB under the transistors. The thermal pads are electrically connected to the drain terminal of each transistor. The aluminium blocks were submerged in liquid nitrogen and cool the transistors by conduction through the PCB. As nitrogen is a dielectric fluid, there are no concerns regarding electrical isolation between the blocks. To achieve a range of temperatures, the liquid nitrogen was allowed to evaporate and the temperature gradually increased, the rate of which was limited by the thermal inertia of the PCB and

aluminium block. The double pulse test was conducted each time a set temperature interval had been surpassed.

A DPT takes approximately 14.5 µs to complete and is repeated infrequently (4 Hz). This results in a very small heat dissipation. The junction temperature can therefore be assumed to be equal to the casing temperature where it was measured. This was done using a thermocouple inserted into the original copper mount, attached to the thermal pad of the lower transistor.

To ensure that the measurement circuits were operating within their rated temperature range, halogen lamps were used to radiatively heat the lower region of the board on which they were populated.

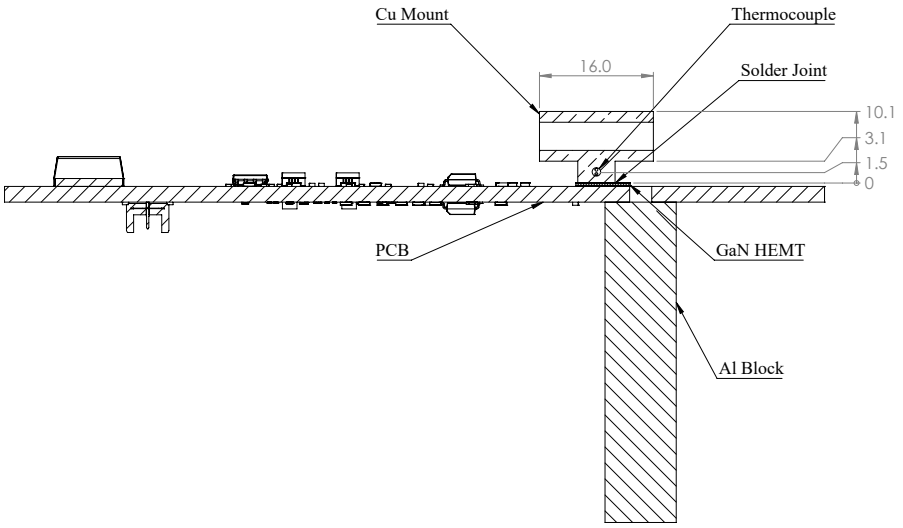


Figure 3.18: Section view of the test platform showing the cooling arrangement for the cryogenic testing (dimensions in mm).

3.2.3 Results

The results were collected with current flowing out of the bridge (Fig. 3.20b), in which case the lower transistor is either not conducting or reverse-conducting, and the top transistor switching causes the current to commutate. Results were also collected for the case where current is flowing into the bridge (Fig. 3.20a) and the lower transistor is hard-switched generated significant switching energy.

The following observations are made from the waveform measurements with current flowing into the bridge, Fig. 3.20a (the observations are highlighted on the figures with numbered arrows for clarity):

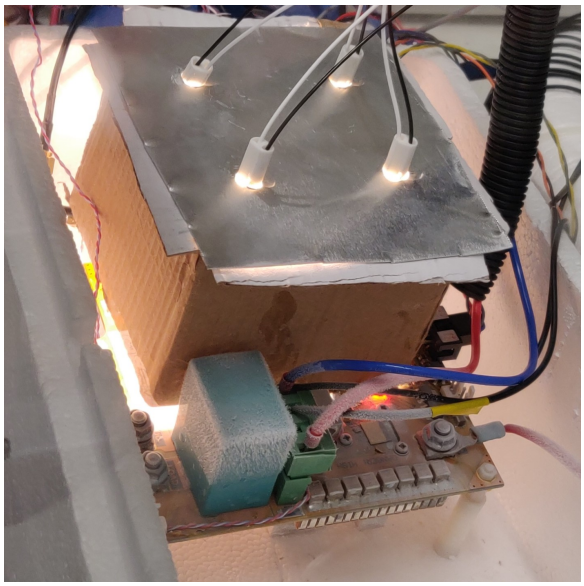


Figure 3.19: Image of the double pulse test platform during cryogenic testing. The aluminium blocks are visible below the board. Halogen lamps are being used to heat the measurement circuits to ensure they are in their operational temperature range.

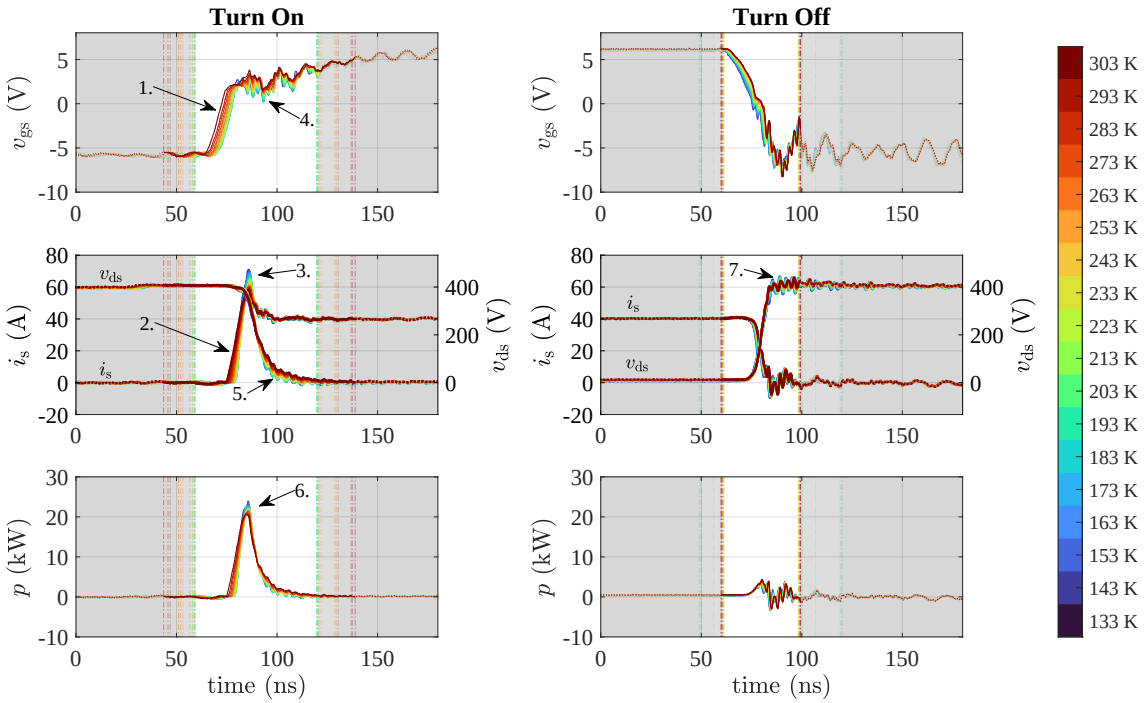
1. The reduced threshold voltage at cryogenic temperatures [52], [58] is visible as a temporal shift of the v_{gs} turn-on and turn-off waveform as each DPT capture is aligned by the falling edge of v_{ds}.

2. The expected increase in $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ with lower temperatures is clearly visible in the turn-on i_{s} trace.

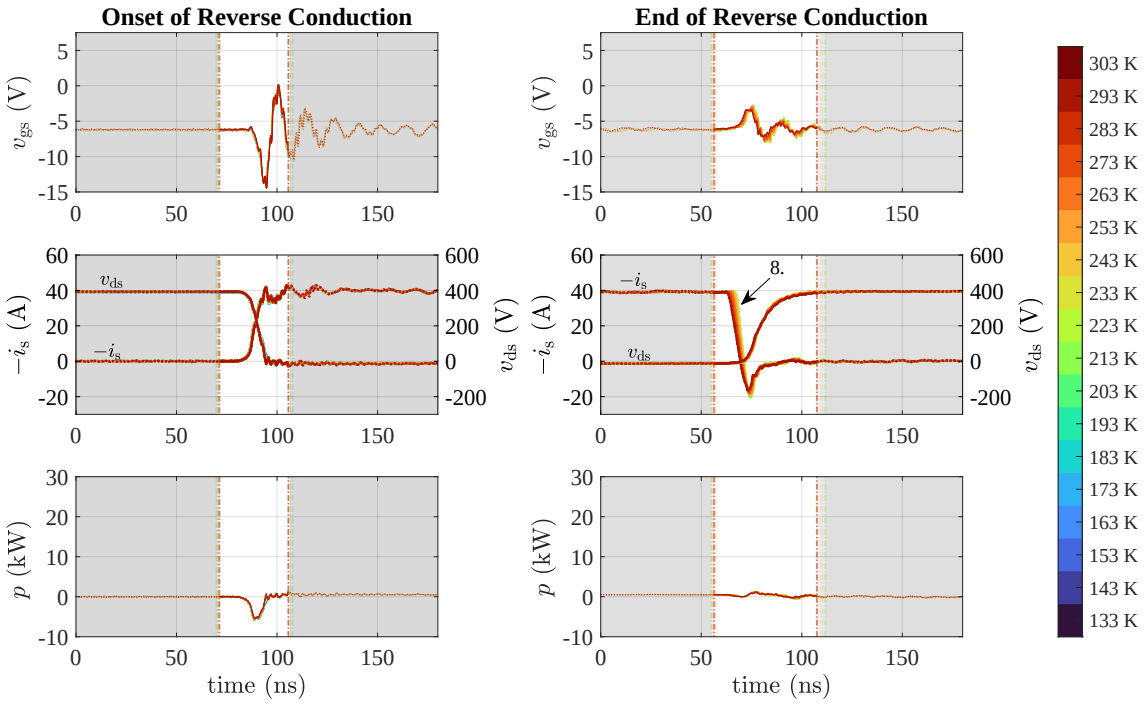
3. The magnitude of the current overshoot in the turn-on i_{s} measurement increases at cryogenic temperatures. The overshoot is caused by the node capacitance discharging. The capacitance is not expected to change at cryogenic temperatures. The stored charge is approximately equal to the area of the overshoot in the i_{s} trace, and so given the faster $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ a larger overshoot magnitude to maintain the same area can be expected.

4. Larger sags are seen in v_{gs} at cryogenic temperatures during turn-on due to the higher $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ through the parasitic source inductance and marginally larger $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ across the miller capacitance.

5. At turn-on the "tail" of the v_{ds} measurement approaches zero faster at cryogenic temperatures, resulting in lower switching losses. The shape of this curve is governed by the non-linear voltage characteristics of the transistor C_{oss} suggesting this changes at cryogenic temperatures.



(a)



(b)

Figure 3.20: Switching edges at low temperatures, showing gate-source voltage, drain-source voltage, source current, and instantaneous switching loss. (a) shows current out of the bridge (hard-switching), (b) shows current into the bridge (soft-switching). The observations listed in Section 3.2.3 are numbered on the figures.

6. The resultant switching power pulse is shorter at cryogenic temperatures but with a fractionally higher peak power.

7. In the turn-off v_{ds} waveform, marginally larger amplitude ringing is observed.

Regarding the waveform measurements with current flowing out of the bridge, Fig. 3.20b, there is remarkably little difference between these waveforms with the exception of the $\mathrm{d}i_d/\mathrm{d}t$ in the turn-off i_s trace (indicated on the figure as 8.). Anomalous switching behaviour is observed at the turn-off edge at temperatures below 193 K. This is the subject of discussion in Section 3.2.3.2.

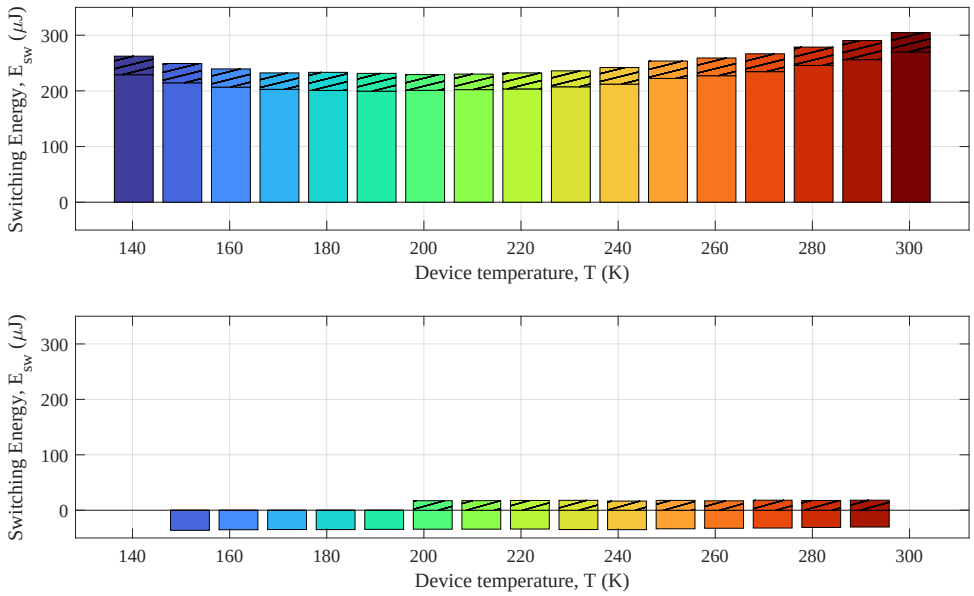


Figure 3.21: Bar plot showing the switching energy of the GS66516T transistor with 40 A switched current at cryogenic temperatures. The top graph shows the switching energy when the current is into the bridge and the transistor is hard-switched. The bottom graph shows when current is out of the bridge resulting in soft-switching.

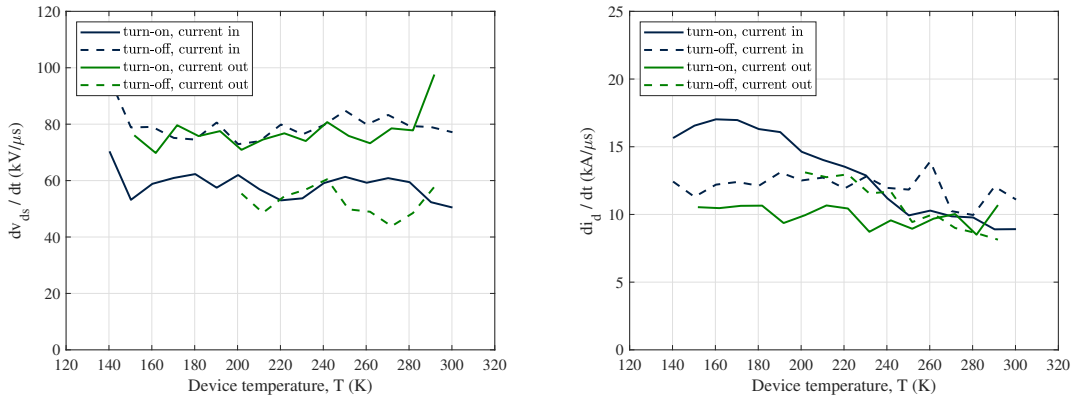
The switching losses initially decrease with falling temperature to a minimum of 212 µJ recorded at 200 K. This represents a 27% reduction compared to the switching energy measured at room temperature (292 µJ). Below this minimum, the switching energy was seen to increase. This is in contrast to two papers previously published in the literature for the GS66516T transistor [54], [60], where the decrease is monotonic. Our result agrees with the findings of [47], which shows a similar trend with a minimum switching energy at ∼198 K, but for the lower current GS66504B and GS66508B transistors. They note that in their setup, the on-state gate voltage decreases at cryogenic temperatures, from 6.1 V to 5.6 V. This may lead to the rise, or

part of the rise, in switching energy below 198 K. From the v_{gs} waveforms it can be seen that this is not the cause of the non-monotonic trend in our results. The initial reduction in switching losses appears to be due to the faster $\mathrm{d}i_d/\mathrm{d}t$ and $\mathrm{d}v_{ds}/\mathrm{d}t$, but at sufficiently low temperature, the additional switching loss due to the increasing overshoot of i_s dominates, causing the switching losses to increase.

Switching losses are only presented for the GS66516T at 400 V bus voltage over a range of switched currents in [54]. The switching energy measurements at 298 K and 203 K in [54] agree to within a reasonable degree of error to the measurements presented here. The lowest temperature reported 133 K deviates significantly, with switching losses shown to continue decreasing. The method in [54] requires a deskewing step in post-processing which may introduce significant error.

A qualitative comparison of the results presented here to those in the existing literature is summarised in Table 3.4. There are limitations with the methods presented in the literature to date which may affect the accuracy or validity of the reported results, these are also highlighted in the table. The work presented here does not suffer from these limitations having used a carefully designed experimental setup and methodology.

The results presented here constitute a significant contribution to the literature. By using a well understood and calorimetrically validated test setup and procedure there is greater certainty in the validity of the results compared to past works. The observations of [47], which suggested a different trend to those in previous papers have been shown to be repeatable with the higher current rated GS66516T transistor.



(a) (b)

Figure 3.22: Switching speeds for the GS66516T transistor for the four types of switching edges, current in and out of the bridge, and turn-on and turn-off. (a) $\mathrm{d}v_{ds}/\mathrm{d}t$, (b) $\mathrm{d}i_d/\mathrm{d}t$.

Table 3.4: Comparison of results with previous literature.

Paper	Comparison of results	Limitations of paper
[82]	This paper reports a decrease in switching losses between RT and 77 K. Because results are only presented at two temperatures (for a range of switched currents), it is not possible to determine if the decrease was monotonic. Switching losses measured are less than measured in this work despite large oscillations in current waveform.	Large oscillations (200 A_{p-p} are observed in the current measurement channel, indicative of poor switching behaviour, which has not been observed in this work likely due to a sufficiently low SCCL inductance. The switching energy results therefore are not representative of a well functioning circuit.
[60]	This paper reported a monotonic decrease in switching losses with decreasing temperature in contrast with our result. The losses are significantly less than measured here due to the lower bus voltage.	A 200 V bus voltage is used for the double pulse testing, which is less than a third of the transistor's rated voltage. Testing at 400 V is representative of a practical application voltage and imposes greater voltage stress on the transistor.
[54]	This paper reported a monotonic decrease in switching losses with decreasing temperature in contrast with our result. The datapoints at temperatures above 133 K correlate with the measurements in this work.	The test setup required a deskewing step in post-processing which may introduce significant error. An error in the deskew value leads to an error of 9.5 % ns^{-1} [101].
[47]	Trends in switching loss measurements match those observed in this work's measurements. A lower current rated version of the transistor was used for these measurements resulting in smaller switching energies.	A SiC diode was used as the opposing device rather than a second GaN transistor, which may not be representative of a half-bridge switching cell.

3.2.3.1 Mitigation of $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ induced false turn-on

At temperatures only marginally below room temperature, shoot-through was observed to occur when the bottom transistor was hard turned-on, Fig. 3.23a. The magnitude of the shoot-through increased most significantly between 303 K and 243 K. This has previously been observed to occur in [54]. The cause of the shoot-through is the $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ across the top transistor when the lower transistor is switched on, the miller current charges the gate of the upper transistor, causing it to conduct. This effect is caused by $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$, which is strongly dependent on the applied bus voltage, it is possible to prevent the top transistor from fully conducting by reducing the bus voltage to 100 V, as in Fig. 3.23b.

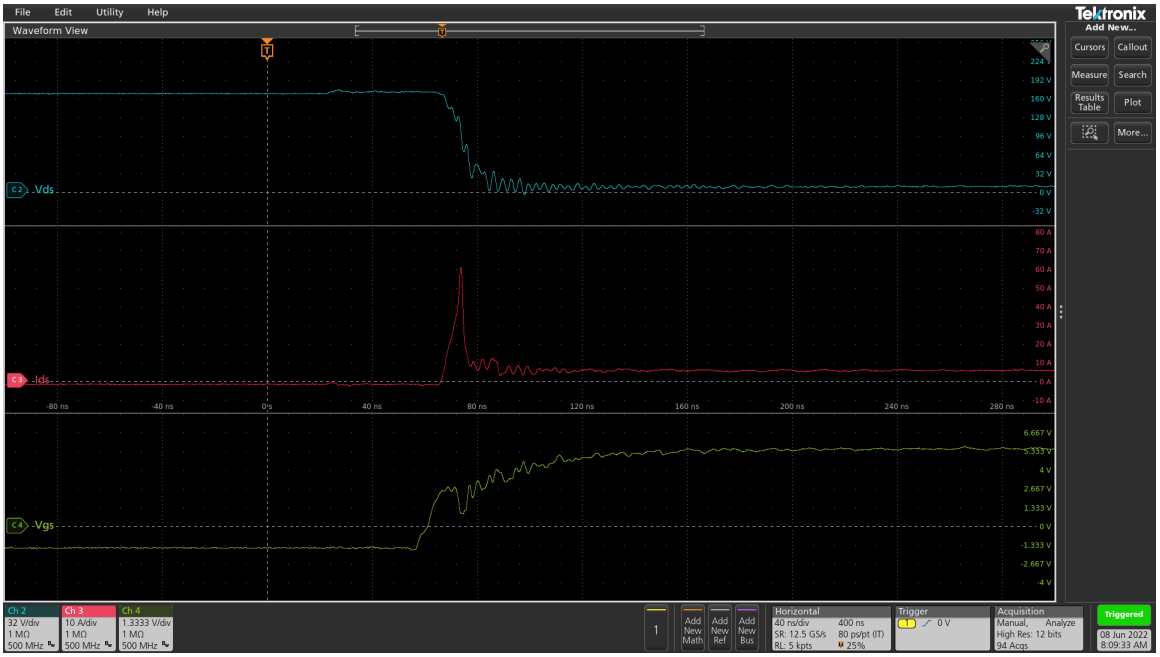
It can be seen in Fig. 3.22a that at cryogenic temperatures there is no significant increase in $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$. The shoot-through at cryogenic temperatures must therefore be due to the decreased threshold voltage, which falls approximately linearly from 1.7 V to 1.2 V between room temperature and 77.15 K [52].

A −2 V off-state gate voltage is insufficient to completely eliminate shoot-through, (−3 V, which is the manufacturer's recommendation for $v_{\mathrm{gs(off)}}$, was used in [54] where shoot-through was also observed). Using the variable off-state gate voltage of the test platform, it was found that it was possible to eliminate shoot-through by using −6 V turn-off gate voltage. This prevented the upper transistor gate-voltage from exceeding the threshold voltage, keeping the transistor pinned in the off-state during hard switched turn-on. The use of −6 V may be lower than required, but was the only lower off-state gate voltage possible with this test platform. Reducing the off-state gate voltage was also shown in [101] to reduce switching losses. As long as the duration of dead-time is kept small, a lower off-state gate voltage is beneficial for converter performance. The manufacturers recommended −3 V off-state gate voltage appears to be the least negative value which prevents shoot-through from occurring at room-temperature, minimising dead-time losses. The negative gate voltage rating is −10 V absolute, with a transient rating of −20 V. Therefore, a −6 V off-state gate voltage should not affect the reliability of the transistor.

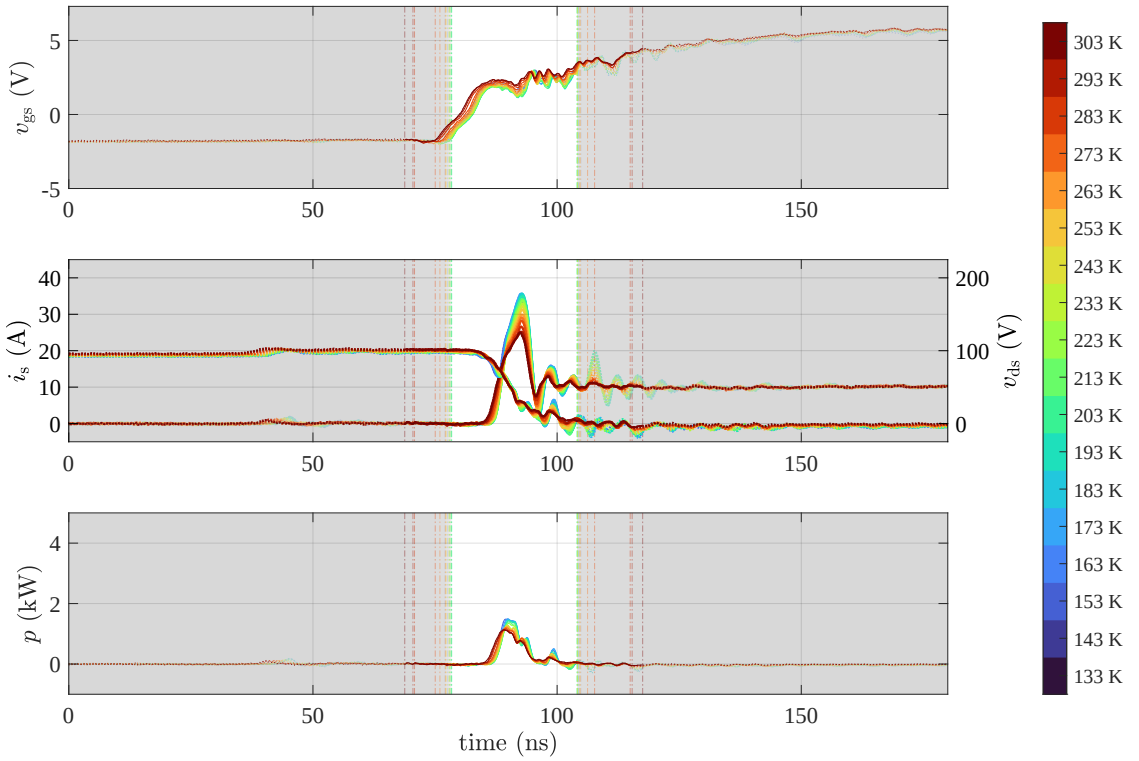
The switching energies shown in Fig. 3.21 are therefore compiled using a −6 V off-state gate voltage.

3.2.3.2 Discussion on anomalous switching behaviour and temperature limitation of experimental apparatus

At temperatures below 150 K large deviations from the expected current were observed in the i_{s} signal during the soft switched turn-off of the bottom transistor.



(a)



(b)

Figure 3.23: Scope captures showing shoot-through at a hard turn-on switching edge when only −2 V turn-off gate voltage was used. (a) 160 V bus voltage at 103 K, (b) 100 V bus voltage for a range of temperatures between 133 K to 303 K.

This is shown in Fig. 3.24. In this transition it is the gating of the top transistor causing the current to commutate. Initially, the current is flows out of the bridge via the lower transistor. Gating the lower transistor off results in it operating with body-diode like behaviour, the current free-wheeling in the lower transistor. The top transistor is then hard-switched on, causing the current to commutate.

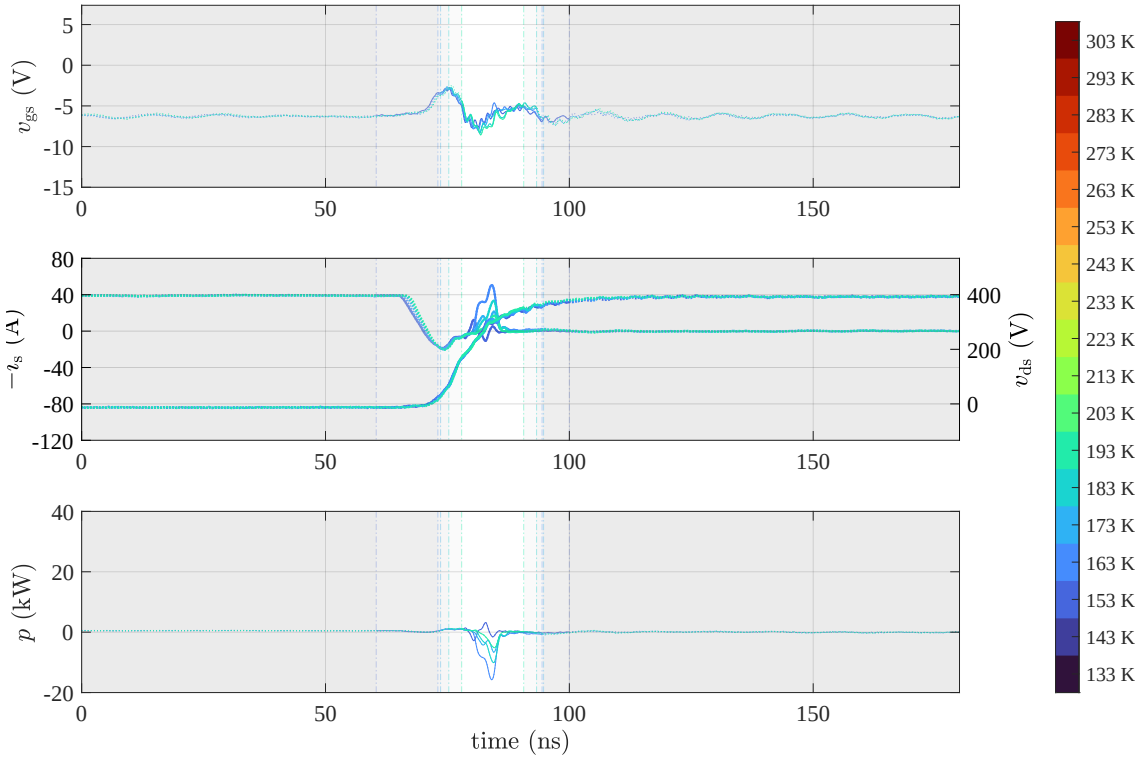


Figure 3.24: DPT waveforms excluded from the results due to anomalous behaviour in the current measurement channel.

It was hypothesised that the current deviation could be attributed to false momentary turn-off of the top transistor due to the large $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ turn-on transition occurring in the opposing transistor at cryogenic temperatures. If this was the case, when the top-switch is gated on, the inductor current commutates from conducting through the bottom transistor to the top. This causes a voltage spike across the parasitic source inductance of the top transistor, reducing the effective voltage between the gate and source. This switches the transistor off momentarily, causing the current to commutate back to the lower transistor. This behaviour was observed in [54]. They suggest the voltage spike across the parasitic inductance L_s may be sufficient to over-volt the gate of the top transistor, damaging the transistor.

On further investigation, large $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ induced turn-on is considered unlikely for the following reasons:

1. The deviation from the expected current trace occurs after the instant of peak $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$.

2. The oscillations in the current measurement are not reflected in the v_ds or v_gs channels.

3. Given the symmetric operation of the half-bridge and the near identical electrical layouts, it is surprising that the anomalous behaviour is only observed when current is flowing out of the bridge.

Therefore it is likely that the anomaly was the result of an issue occurring in the signal chain of the i_s measurement channel. To confirm this the shunt voltage was directly measured and no evidence of the deviation could be detected.

It is not understood why the combination of cryogenic temperatures and the soft-switched turn-off edge led to the anomalous behaviour in the measurement circuit. Heating the measurement circuits with radiative heaters did not resolve the issue (nor did heating the gate-drivers). Due to the tightly integrated design of the power and measurement circuits, it is possible despite the heater that components in close proximity to the power circuit were still outside their operational temperature range. This highlights the challenges of exposing electronics to cryogenic temperatures. Given that the anomaly occurred consistently on a single switching transition but not on others it is not likely a mechanical issue caused by contraction of the materials, rather that the tolerance to noise (potentially induced by ground bounce between the measurement ground and power ground) was degraded due to the low temperatures.

Unfortunately, the test equipment was returned to the owner before the cause of this anomalous behaviour could be determined.

3.3 Conclusions

In the first section of this chapter, Section 3.1, the on-state resistance of the GaN Systems GS66508T, top-side cooled, 650 V transistor has been comprehensively characterised. The results of the first experiment which examined the $R_{\mathrm{ds(on)}}$ at a known junction temperaure agreed with previous cryogenic characterisations of this transistor conducted at low current densities. The range of current densities characterised

was extended to three times the room temperature rating of the transistor (90 A), this provides important insight into the behaviour of the HEMT at high current densities where non-linear effects such as saturation and pinch-off can occur. This had not previously been investigated.

The second experiment, using large continuous currents, has not previously been conducted in the literature. Transistor failure occurred repeatably at three times the rated current as a result of thermal instability. This occurred at a temperature 250 K lower than the maximum rated junction temperature of the transistor. The thermal conductivity of silicon (from which the die is mostly composed) increases by a factor of 9.4 at 77.15 K compared to room-temperature. The large thermal loads increased junction temperature which led to an increase in the on-state resistance and thermal resistance of the heat dissipation path (due to an increased thermal resistance of the die). This had a significant role in determining the point of thermal instability. This work therefore comprehensively addressed research question 2a.

Regarding research question 2b, as previously stated, it was determined that thermal instability is the mechanism responsible for thermal failure at cryogenic temperatures. This is not a novel failure mode but at cryogenic temperatures it defines thermal limit whereas at room temperature the maximum junction temperature is typically considered to be the thermal limit. This understanding of the thermal limit was important for the design and modelling of a cryogenic inverter described in later chapters. While it was unexpected that the point of instability occurs when the junction temperatures is 250 K lower than the maximum rated junction temperature, the cryogenic temperatures did not exacerbate this failure mode, and in fact, the reduced junction-to-casing thermal resistance and $R_{\mathrm{ds(on)}}$ caused the onset of this failure mode to occur at three times higher currents than the room temperature current rating of the transistor.

In Section 3.2, the switching behaviour of the GaN Systems GS66516T transistor was investigated at cryogenic temperatures.

$\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ induced shoot-through, that has previously been reported in the literature to be an issue at cryogenic temperatures [54], was observed. By using a lower off-state gate voltage, it was shown that this could be effectively suppressed. Had this failure mechanism not been resolved it would have been significant in answering research question 2b, and constrained the maximum power of a potential cryogenic inverter, in turn answering research question 2c.

Measurements of switching-speeds and switching energies were recorded at cryogenic temperatures using a well-understood and calorimetrically verified test platform.

An initial decrease in the switching energy was observed which is consistent with the literature. At 213 K a minimum switching energy was observed and for temperatures below this the switching energy monotonically increased. Although this has been reported for a lower current transistor from the same manufacturer and series, this has not been reported to date for the GS66516T transistor characterised. Previous characterisations have shown a monotonic decreases in switching energy from room temperature to the minimum temperature measured. This work contributes to our understanding for answering sub-question 1a. Further work is required to reduce the minimum junction temperature that can be achieved with the test platform.

The combination of an eight-fold reduction in on-state resistance (between 373 K and 123 K) and consistent switching performance at cryogenic temperatures makes this power transistor a good candidate for a cryogenic power converter.

Chapter 4

Cryogenic Inverter Modelling

In Hartmann et al. [3] pessimistic, baseline and optimistic values for inverter efficiency are estimated and assumed to be constant for the entire flight profile. These estimates are used in a wider aircraft model to evaluate the performance of a liquid hydrogen fuelled aircraft. However it is well understood that the efficiency of an inverter is typically a function of power and can vary significantly, suggesting that the constant efficiency model used in [3] is an over simplification. In particular, two key errors will result from using a constant efficiency model, which is exacerbated by the large power differential between the take-off and cruise phase of flight. Firstly, larger thermal loads than modelled will occur during the take-off phase, due to the falling efficiency at high power; at a system level this will result in an under-sizing of the inverter and its associated thermal management. And secondly, the inverter will have higher efficiency than modelled during the cruise phase, where it operates at relatively light load. This will consequently cause an overestimate of the predicted mass of fuel required for the flight.

In this chapter, a detailed model to simulate a cryogenically cooled inverter, developed in MATLAB, is presented. The simulation is able to predict the losses and resultant junction-temperature for a given set of transistor parameters, inverter parameters, and a specified coolant (either a cryogen or air).

This model is used to predict the losses of the experimental inverter described in Chapter 5 and to analyse the potential performance of a full-scale inverter suited for a drive cycle representative of the requirements for a light-aircraft. A comparison of the drive-cycle performance is conducted for a cryogenically cooled inverter and a conventionally cooled inverter.

As well as the insights from the analysis of the inverter systems presented in this chapter, the model developed has a broader value as it can be integrated into an

aircraft system model such as the one presented in [3] to improve their accuracy considering the dynamic efficiency of the inverter during the different phases of flight.

The work described in this chapter therefore addresses one of the gaps identified in the literature and answers research question 1b: *What improvements in efficiency and peak power can be achieved by cryogenically cooling a GaN inverter compared to a conventionally cooled GaN inverter for aircraft propulsion applications?*.

4.1 Inverter Losses

The sources of losses in an inverter include:

1. **Transistor conduction loss** - the joule losses incurred due to the on-state resistance between the drain and source of the transistor, $R_{\mathrm{ds(on)}}$

2. **Switching losses** - this loss can be decomposed into the loss caused by the overlap of drain-source voltage, v_{ds}, and drain-source current, i_{ds}, during the switching transition and discharging and changing of the node capacitance.

3. **Dead time loss** - during the dead time the negatively biased GaN HEMT conducts with a bias voltage equal to the difference between the off-state gate voltage (typically $-3\,\mathrm{V}$ to $-6\,\mathrm{V}$) and the threshold voltage, V_{th}. The dead time losses are then the product of the negative bias voltage and the conducted current.

4. **Conductor copper losses** - Joule losses in copper conductors such as PCB traces and cables. Note that the resistivity of copper falls by a factor of six from $373\,\mathrm{K}$ to $77\,\mathrm{K}$.

5. **DC link capacitor losses** - capacitor losses are the product of the square of the RMS current flowing in the capacitor and the equivalent series resistance (ESR) of the capacitor.

All of these sources of loss are modelled in the MATLAB simulation. EMI input and output filters are components of the larger motor drive system, and are not considered parts of the inverter. The losses associated with any filters are therefore not modelled.

The losses of a GaN HEMT, both conduction and switching, depend on the junction temperature as shown in [7], [60], [101], [102]. The simulation therefore accounts

for the electro-thermal behaviour of the transistor, calculating the generated heat coupled with the prediction of the junction temperature. As mentioned, copper losses are also dependent on temperature, though it is a much smaller contribution to the overall inverter losses.

A flow diagram showing how the simulation is executed is shown in Fig. 4.1.

First the simulation parameters are used to determine the electrical frequency and the constant components of the inverter cooling thermal resistance, to the coolant (LN2 or air), R_{th}. The constant components are the junction to casing thermal resistance, $R_{\text{j-c}}$, and the thermal resistance of the thermal interface material, R_{TIM}. The final component of the thermal resistance path is the heat sink thermal resistance, R_{HS}, which is dependent on the heat conducted.

Second, the losses for an initial estimate of the junction temperature are calculated, the losses associated with the transistors, Q_{tran}, are then used to calculate an updated junction temperature, the model is iterated to converge on a heat generation and junction temperature. The thermal resistance between the junction and the coolant (LN2, LH2, or air) is modelled using a lumped thermal resistance model. This is described in greater detail in Section 4.3.

The model is deemed to have converged once the change in junction temperature has fallen below a suitably small threshold, c.

4.1.1 Transistor Conduction Losses

As shown in Chapter 3, the $R_{\text{ds(on)}}$ significantly decreases at cryogenic temperatures, which in turn decreases conduction losses. This effect is accounted for by interpolating $R_{\text{ds(on)}}$ from the dataset collected in Chapter 3 for a given junction temperature.

In each phase, one of the two switches in a phase is continuously conducting the phase current. The conduction losses of the inverter can therefore be calculated simply as per Eq. 4.1 using the temperature dependent on-state resistance.

$$Q_{\text{con}} = 3I_{\text{ph,RMS}}^2 \left(\frac{R_{\text{ds(on)}}(T_{\text{j}})}{n_{\text{p}}} \right) \tag{4.1}$$

where n_{p} is the number of transistors in parallel per switch.

4.1.2 Transistor Switching Losses

In a motor drive, the motor speed sets the electrical frequency. This in turn sets the minimum switching frequency that can be used to generate the sine wave output

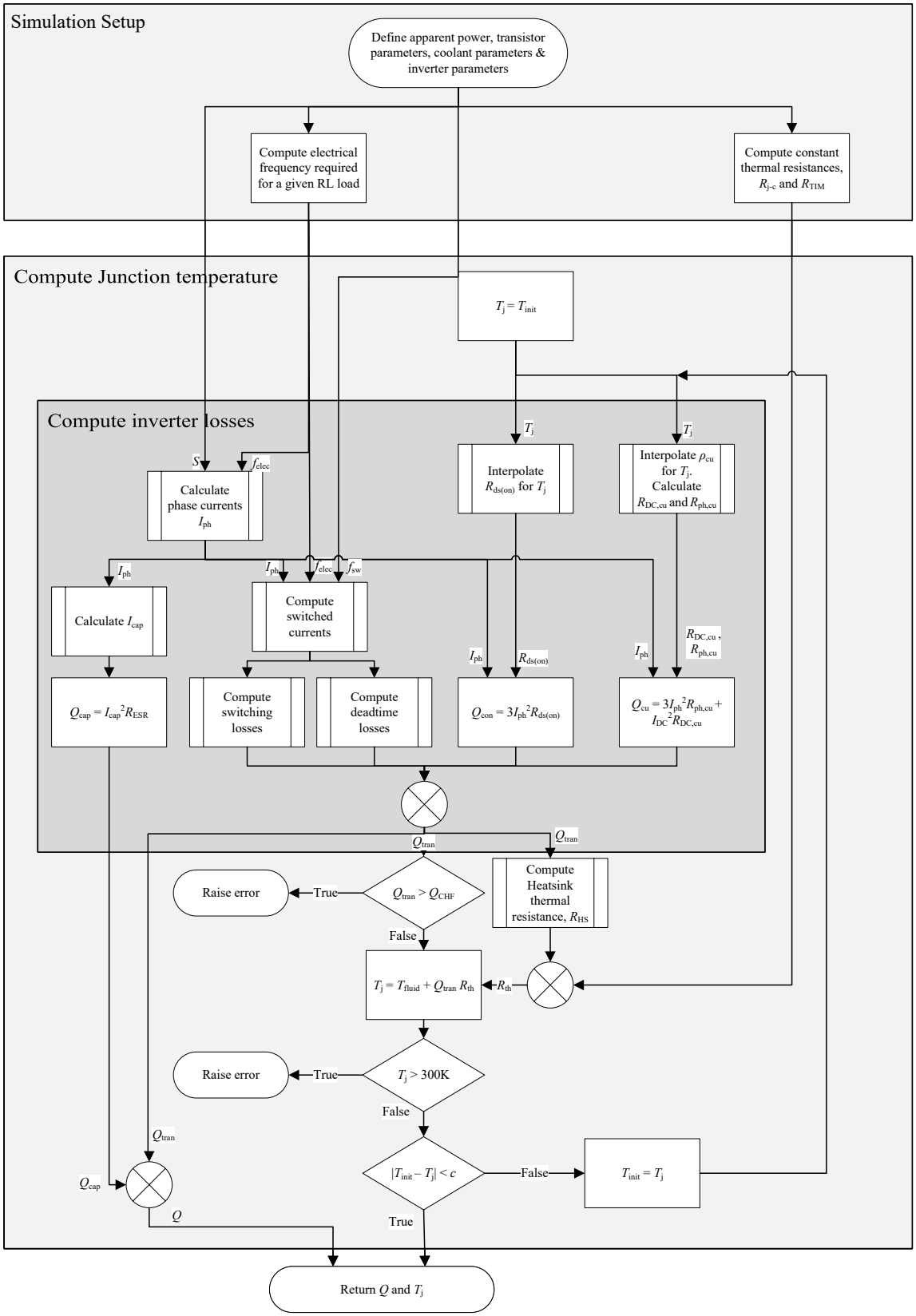


Figure 4.1: Flow diagram describing the execution of the inverter model.

current without significant distortion. Consequently, in motor drive applications, the switching frequency is typically between 15 kHz to 30 kHz. For a room-temperature GaN inverter, with low switching energy and low switching frequency it can be seen that the switching losses are a much smaller proportion of the overall losses compared to the conduction losses.

At cryogenic temperatures, the conduction losses are eight times smaller than at 373 K, leaving the switching losses as a significant, if not dominant, source of loss in the inverter. To accurately assess the losses, it is therefore necessary to accurately estimate the switching losses.

Calculating accurate switching losses is challenging, as the losses depend on the interactions between the transistor switching behaviour, the transistor package, the gate drive strength, and the circuit's parasitic elements. Even with accurate measurements of the parasitic elements, loss models can underestimate losses by up to 30% [103].

Three methods of calculating the switching losses are assessed: a parametric loss model, interpolation of empirical measurements of the switching loss, and finally extracting the switching loss from a SPICE circuit simulation.

All three methods assume a 400 V bus voltage and require the switched current as an input. Cryogenic temperatures marginally reduce switching losses as seen in Section 3.2. The effect of temperature is discussed in Section 4.1.2.4.

The switched current is calculated as follows. The time at which a switching instance occurs is calculated using the centre aligned and regular sampled PWM method used to generate the gate signals $t_{\mathrm{on},p,k}$ and $t_{\mathrm{off},p,k}$. The current at the switching instance $i_{\mathrm{ph},p}(t)$, can then be calculated from the power factor and the impedance of the load.

The reference signals generate sinusoids using third-harmonic injection to maximise the line-to-line voltage without creating discontinuities in the load star-point voltage. The reference signals for the PWM generation are given in Eq. 4.2 where ω_e is the electrical frequency to be generated.

$$v_{ref,a} = \frac{2}{\sqrt{3}} \sin\left(\omega_{\mathrm{e}} t\right) + \frac{1}{6} \sin\left(3\omega_{\mathrm{e}} t\right) \tag{4.2a}$$

$$v_{ref,b} = \frac{2}{\sqrt{3}} \sin\left(\omega_{\mathrm{e}} t + \frac{2\pi}{3}\right) + \frac{1}{6} \sin\left(3\omega_{\mathrm{e}} t\right) \tag{4.2b}$$

$$v_{ref,c} = \frac{2}{\sqrt{3}} \sin\left(\omega_{\mathrm{e}} t + \frac{4\pi}{3}\right) + \frac{1}{6} \sin\left(3\omega_{\mathrm{e}} t\right) \tag{4.2c}$$

A sawtooth carrier at the switching frequency is then used to modulate the reference signals, identifying the switching instances as $t_1, ..., t_k$. The phase currents are assumed to be a perfect sinusoid i.e. the first fundamental of the real phase current. The phase currents are calculated as per Eq. 4.5 which is dependent on the impedance and power factor of the load, Z_{load} and $\cos\phi$.

$$i_a = \frac{V_{\text{DC}}}{|Z_{\text{load}}|} \sin(\omega_e t + \phi) \tag{4.3}$$

$$i_b = \frac{V_{\text{DC}}}{|Z_{\text{load}}|} \sin\left(\omega_e t + \frac{2\pi}{3} + \phi\right) \tag{4.4}$$

$$i_c = \frac{V_{\text{DC}}}{|Z_{\text{load}}|} \sin\left(\omega_e t + \frac{4\pi}{3} + \phi\right) \tag{4.5}$$

The switched current, $i_{p,k}$, is calculated for each switching transition $k = 1, ..., n$, on each phase $p \in \{A, B, C\}$. The switching energy, $E_{\text{sw(on)},p,k}$ or $E_{\text{sw(off)},p,k}$, is calculated using one of the methods described in subsequent sections.

$$E_{\text{sw,upper}} = \sum_{p\in\{A,B,C\}} \sum_{k=1}^{\frac{f_{\text{sw}}}{f_{\text{e}}}} \left(E_{\text{sw(on)},p,k} + E_{\text{sw(off)},p,k}\right) \tag{4.6}$$

The switching losses are computed for the upper transistor in a phase and doubled to account for the symmetric operation of the switches in a half-bridge with sinusoidal current. At each switching instance, for current out of the bridge, one transistor is hard switched (the transistor is turned on while blocking voltage, or the transistor is turned off while conducting current) and the opposing transistor is soft switched.

$$Q_{\text{sw}} = 2E_{\text{sw,upper}} f_{\text{e}} \tag{4.7}$$

4.1.2.1 Parametric model

The first method used to estimate the switching loss is a parametric model using values from the manufacturer's datasheet. The hard switched transistor's switching loss is approximated as per Eq. 4.8. In the soft switched case, Eq. 4.9, the switching loss is minimal and equal to the energy stored in the node capacitance and the reverse recovery charge of the body diode (a GaN HEMT does not have a body diode, so it has zero reverse recovery charge). The rise and fall times of the GaN transistor differ significantly, so the on and off switching energies are calculated separately [28].

This method relies on the accuracy of the parameters supplied in the manufacturers datasheet and the similarity between the parasitic elements in the test circuit and the circuit layout to be simulated.

For hard switching ($I_{\text{on},p,k} > 0$ or $I_{\text{off},p,k} > 0$):

$$E_{\text{sw(on)},upper,p,k} = \frac{1}{2} C_{\text{o(er)}} V_{\text{bus}}^2 + \frac{1}{2} V_{\text{bus}} I_{\text{on},p,k} \cdot t_r \tag{4.8a}$$

$$E_{\text{sw(off)},upper,p,k} = \frac{1}{2} C_{\text{o(er)}} V_{\text{bus}}^2 + \frac{1}{2} V_{\text{bus}} I_{\text{off},p,k} \cdot t_f \tag{4.8b}$$

For soft switching ($I_{\text{on}} \leq 0$ or $I_{\text{off}} \leq 0$):

$$E_{\text{sw,on},upper,p,k} = -\frac{1}{2} C_{\text{o(er)}} V_{\text{bus}}^2 + V_{\text{bus}} Q_{\text{rr}} \tag{4.9a}$$

$$E_{\text{sw(off)},upper,p,k} = \frac{1}{2} C_{\text{o(er)}} V_{\text{bus}}^2 + V_{\text{bus}} Q_{\text{rr}} \tag{4.9b}$$

4.1.2.2 Empirical measurements

An alternative approach to the parametric switching loss model is to interpolate the losses from a reference empirical dataset of switching energies [101]. In [101] the switching energies for a GaN Systems GS66516T HEMT were measured over a 100 V to 400 V bus voltage, 10 A to 40 A switching current, and between 323 K to 423 K, with rated and zero gate-resistance, and negative and zero $V_{\text{gs(off)}}$. In Chapter 3 these measurements are extended to cryogenic temperatures.

A piecewise spline is fitted to the data set to interpolate and extrapolate from the experimental data. Close to zero switched current, the switching loss has a non-linear trend leading to an under-estimate of the switching loss using the piece-wise fit. At currents exceeding the measured dataset, the linear extrapolation would also be expected to diverge from the actual switching losses, as a result of non-ideal, non-linear behaviour, such as when the transistor starts to saturate.

An additional issue arises for negative switched currents. The measurement accuracy combined with the very small switching losses associated with charging and discharging C_{coss}, results in the sum of the turn-on and turn-off losses being a small negative values, $\sim -5\,\mu\text{J}$, which is non-physical.

4.1.2.3 SPICE simulation

The key disadvantage of the two methods described so far is that they characterise the transistor for a given gate resistance. The switching speed and therefore the switching losses are highly dependent on the value of gate resistor used. Typically, the value of gate resistor is tuned to lower switching losses while not using such a

low value that the faster switching transients result in damage to the transistors. If the circuit layout is compromised (such as in a cryogenic design as discussed in Chapter 5), the gate resistors may also need to be increased from the manufacturer's recommendation.

In the event that different gate resistors are used from those characterised, the switching losses may be significantly over/underestimated, and using either of the two methods described so far will not capture the increased switching losses. To overcome the issues with the parametric and empirical measurements methods, a SPICE simulation of a half-bridge was developed and set up to record switching energies over a range of output currents. A screenshot of the model can be seen in Fig. 4.2. The transistor model was provided by GaN Systems for the GS66516T transistor [104], [105], and values for the parasitics elements in the circuit were taken from the values measured in [101].

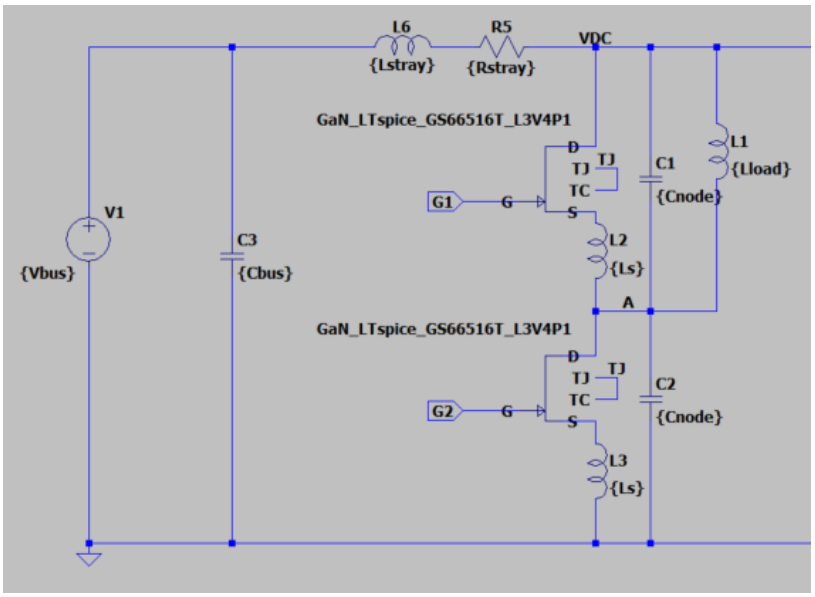
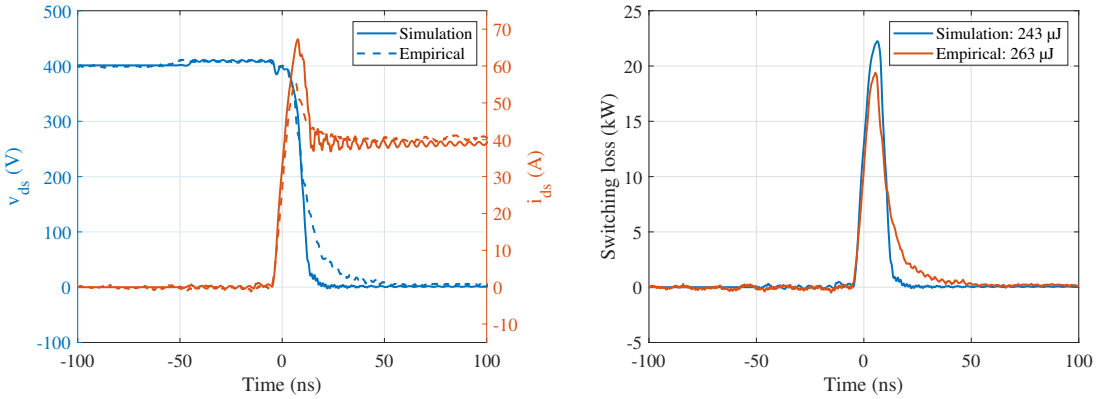


Figure 4.2: Screenshot of the SPICE model with parasitic elements used to estimate the switching losses.

The simulation was correlated with the results from [101], to give similar waveform outputs and switching energies. This can be seen in Fig. 4.3. The most obvious difference between the simulation and the measurements is the shape of V_{ds} as it approaches zero and the overshoot in i_{s}. Both of these effects can be attributed to the way the output capacitance C_{oss} is modelled. C_{oss} has a non-linear voltage dependence with more charge stored per volt at lower voltages. This does not appear to have been accurately captured in the SPICE model provided by GaN Systems. This

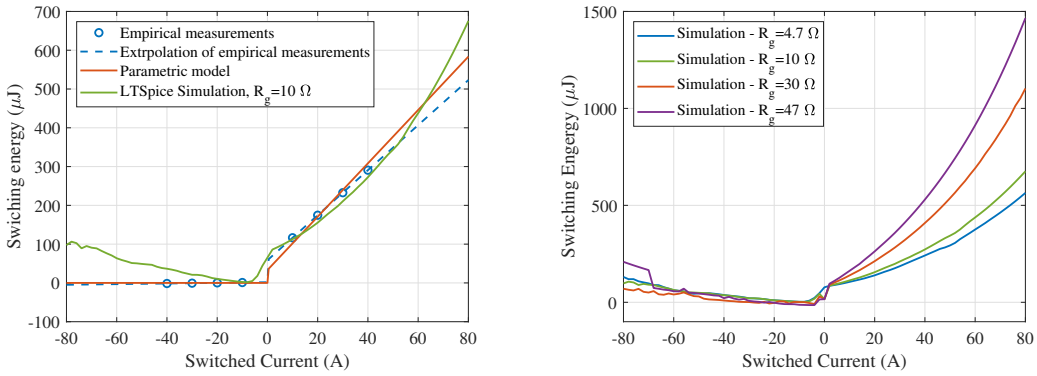
simulation was then used to sweep the current from −80 A to 80 A accounting for the non-linearities around 0 A. A plot showing the comparison between the methods to calculate the switching energy discussed is shown in Fig. 4.4a and a comparison of the output of the SPICE model for different values of $R_{g(on)}$ where empirical data is not available in Fig. 4.4b.



(a) (b)

Figure 4.3: A comparison of the LTspice output to empirically measured waveforms of a switching edge. (a) Comparison of V_{ds} and I_{ds}, (b) Comparison of instantaneous switching loss.

A plot showing the comparison between the methods to calculate the switching energy discussed is shown in Fig. 4.4a and a comparison of the output of the SPICE model for different values of $R_{g(on)}$ where empirical data is not available in Fig. 4.4b.



(a) (b)

Figure 4.4: Switching energies computed using LTspice. (a) Comparison of the three methods used to calculate switching losses. Using $R_{g(on)} = 10\,\Omega$ (b) Switching losses for the GaN transistor modelled in LTspice using a range of gate resistor values.

4.1.2.4 Temperature effect on switching losses

There is significant uncertainty regarding the effect that cryogenic temperatures have on the switching losses. Measurements from [54] suggest up to a 30% reduction in switching losses down to the minimum temperature measured, while in [51] and Chapter 3 they are shown to not decrease monotonically and start increasing again below ∼198 K. It is not possible to use the results in Chapter 3 or [51] to inform the modelled switching losses, as the minimum temperatures measured do not extend as low as the junction temperatures simulated. It is argued that room temperature switching loss characterisations are a valid worse-case estimate of switching loss and are used for modelling in [84]. The same approach is applied here.

4.1.3 Dead Time Losses

The dead time losses are computed for each phase at each switching instance. Only one transistor conducts during the deadtime on each phase at each switching instance. The time at which the switching instance occurs is calculated using the same centre-aligned PWM method used to generate the gate signals. The current at the switching instance $i_{\mathrm{ph},p}(t_k)$, can then be calculated from the power factor and impedance of the load, as explained in Section 4.1.2.

The threshold voltage is strongly affected by the junction temperature [52], [96], which is modelled, but this change has a negligible effect on the overall losses in an inverter application. Firstly due to the short duration of the deadtime compared to the switching period, the deadtime is a very small fraction of the losses before temperature effects are considered, and secondly the 25% reduction in the threshold voltage, V_{gs} is only a small fraction of the reverse bias voltage if a negative off-state gate voltage is used.

$$E_{\mathrm{dt},p,k} = \left|i_{\mathrm{ph},p}(t_k)\right| \left(-V_{\mathrm{gs(off)}} + V_{\mathrm{th}}\left(T_{\mathrm{j}}\right)\right) t_{\mathrm{dt}} \tag{4.10}$$

$$Q_{\mathrm{dt}} = f_{\mathrm{e}} \sum_{k=1}^{\frac{2f_{\mathrm{sw}}}{f_{\mathrm{e}}}} \sum_{p\in\{A,B,C\}} E_{\mathrm{dt},p,k} \tag{4.11}$$

where p denotes one of the three phases A, B, or C. k denotes th kth a switching transition.

4.1.4 Conductor Copper Losses

To calculate the joule losses that occur in the inverters conductors it is assumed that the copper temperature is equal to the transistor junction temperature. This is a conservative assumption as the junction would be expected to be hotter than the copper due to its higher resistivity and poorer thermal contact with the coolant. The copper resistivity is calculated using Eq. 4.12 [6].s Using the dimensions of the copper tracks and the calculated resistivity, the resistance is calculated for the DC and the phase current paths. The overall conductor losses are calculated as $Q_{\text{con}} = I_{\text{DC}}^2 R_{\text{DC}} + 3I_{\text{ph,RMS}}^2 R_{\text{ph}}$.

$$\rho_o = \frac{\rho_{\text{cu,273 K}}}{\text{RRR}} \quad \text{(Temperature-independent Residual Resistivity)} \tag{4.12a}$$

$$\rho_i = \frac{P_1 T^{P_2}}{1 + P_1 P_3 T^{(P_2+P_4)} e^{-\left(\frac{P_5}{T}\right)^{P_6}}} \quad \text{(Intrinsic Resistivity)} \tag{4.12b}$$

$$\rho_{io} = \frac{P_7 \rho_{\text{i}} \rho_{\text{o}}}{\rho_{\text{i}} + \rho_{\text{o}}} \tag{4.12c}$$

$$\rho = \rho_{\text{o}} + \rho_{\text{i}} + \rho_{\text{io}} \quad \text{(Resistivity [n}\Omega\,\text{m])} \tag{4.12d}$$

Where RRR is the residual-resistance ratio for copper, which is dependent on the purity of the copper. A value of 50 can be assumed for RRR [106]. The parameters $P_{1\ldots7}$ are given in Table 4.1.

Parameter	Value
$P1$	1.171×10^{-17}
$P2$	4.49
$P3$	3.841×10^{10}
$P4$	-1.14
$P5$	50
$P6$	6.428
$P7$	0.4531

Table 4.1: Parameters from [6] for Eq. 4.12. Note: there is a typographical error in the citation and P4 is required to be negative.

It can be seen later in this Chapter the low resistivity of copper at cryogenic temperatures means a PCB based inverter design will have negligible conductor losses.

4.1.5 Capacitor Losses

The RMS capacitor current is calculated using the equation given in Kolar et al.[107]. The capacitor losses can subsequently be calculated by multiplying this by

the equivalent series resistance of the capacitor and the resistance of the package leads. No temperature effects are modelled.

$$I_{\text{cap,RMS}} = I_{\text{ph,RMS}} \sqrt{2M \left[\frac{\sqrt{3}}{4\pi} + \cos^2\phi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right]} \tag{4.13}$$

Where M is the modulation index, $M \in \{0, \frac{2}{\sqrt{3}}\}$, and $\cos\phi$ is the power factor.

4.1.6 Gate-drive Losses

The power dissipated due to charging and discharging the gate capacitance is modelled as:

$$Q_{\text{g,sw}} = n_{\text{p}} Q_{\text{g(tot)}} \left(V_{\text{gs(on)}} - V_{\text{gs(off)}} \right) f_{\text{sw}} \tag{4.14}$$

4.2 Inverter Electrical Model

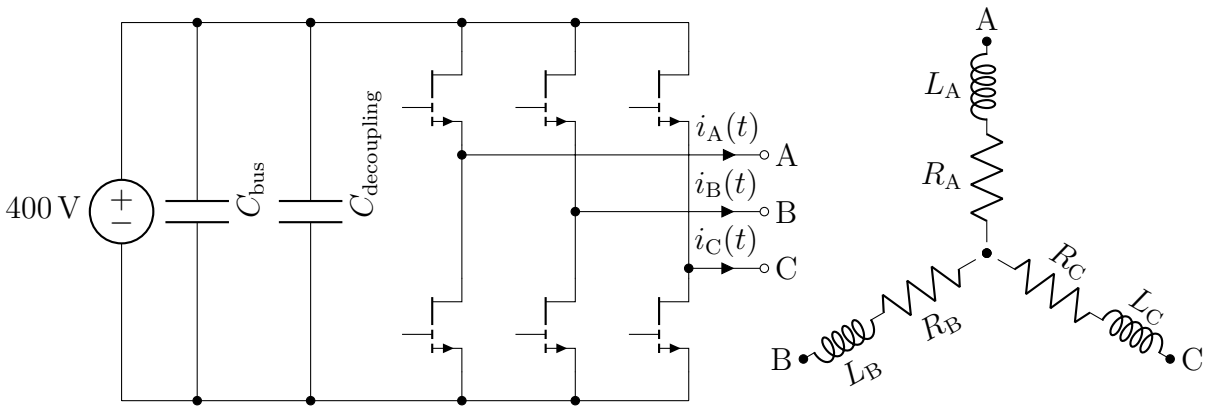


Figure 4.5: Schematic of the full-bridge inverter and load.

Analytical equations are used to compute the inverter DC and phase currents, for the given modulation scheme, load, and DC supply voltage. The calculation assumes that the inverter is perfectly efficient when determining the phase currents. Given the high efficiency of the inverter, this is a valid assumption which will have a negligible effect on the simulation results.

4.2.1 Phase currents

For SPWM with a modulation index of 1 the line-to-line voltage is:

$$V_{\text{ll,RMS}} = \frac{\sqrt{3}}{2} \frac{V_{\text{bus}}}{\sqrt{2}} \qquad \text{(SPWM)} \tag{4.15}$$

Table 4.2: Parameters of the RL load used in the experimental tests

Parameter	Value	Unit
R	110	mΩ
L	0.94	mH
R_p	5.9	mΩ

By using modulation schemes such as third-harmonic injection or down-clamping, the modulation index can be increased to $2/\sqrt{3}$ resulting in higher peak phase-voltage (equal to the bus voltage).

$$V_{\mathrm{ll,RMS}} = \frac{V_\mathrm{bus}}{\sqrt{2}} \qquad \text{(THI)} \tag{4.16}$$

Assuming a star-connected load for a given power and power-factor, the inverter phase currents are calculated as per Eq. 4.17.

$$I_{\mathrm{ph,RMS}} = \frac{P}{\sqrt{3}V_{\mathrm{ll,RMS}}\cos\phi} \tag{4.17a}$$

$$= \frac{2\sqrt{2}P}{3V_\mathrm{bus}\cos\phi} \tag{4.17b}$$

For the simulation of a light aircraft where the inverter is expected to operate as a motor drive the power-factor of the motor is estimated as $\cos\phi = 0.9$ as in [108].

4.2.2 RL load

In the experimental tests of the cryogenic inverter described in Chapter 5, the inverter is connected to a three-phase star-connected RL load and the apparent power increased incrementally. For the RL load used in the experimental set-up, the known impedance allows the phase currents and power factor to be calculated.

$$Z_\mathrm{load} = R + j\omega_\mathrm{e}L \tag{4.18}$$

The required electrical frequency, f_e, for a required apparent power, S, is calculated as per Eq. 4.19.

$$f_\mathrm{e} = \frac{\sqrt{\left(\frac{V_\mathrm{ll}^2}{S}\right)^2 - \left(R_\mathrm{load} + R_\mathrm{p}\right)^2}}{2\pi L_\mathrm{load}^2} \tag{4.19}$$

4.3 Thermal Model

Lumped thermal resistances are used to model the components in the heatpath between the transistor junction and ambient. This assumes the transistors are the primary source of loss, which is true for the cases modelled. The total thermal resistance is the sum of:

1. The transistor junction to casing thermal resistance, $R_{\mathrm{j-c}}$
2. The thermal resistance of the thermal interface material, R_{TIM}
3. The thermal resistance of the heat sink, R_{HS}

The thermal resistance calculations below assume the inverter is designed with discrete transistors with individual heat sinks soldered to the thermal pad and that the dominant heat path is via heat sink. The thermal resistance of each component is therefore divided by the number of parallel transistor that form a switch, n_{p}, and then by six switches that form the full-bridge inverter. This is shown in Fig. 4.6.

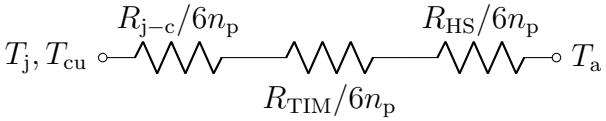


Figure 4.6: Thermal resistance model used to compute the junction temperature, T_{j} for given loss Q.

4.3.1 Transistor Package and TIM

A junction to casing thermal resistance is provided in the manufacturer's datasheet, $0.27\,\mathrm{K\,W^{-1}}$. As shown in Fig. 3.14 the thermal resistance of the materials in the package thermal path all have increased thermal conductivity at cryogenic temperatures, most notably silcon, which increases by a factor of 9 between room temperature and the temperature of liquid nitrogen.

The internal dimensions of the transistor are unknown, though they have been estimated for the smaller GS66508T transistor from an exploded render of the package [109]. These dimensions do not lead to a thermal resistance that correlate with the datasheet thermal resistance value for the GS66508T. For this reason, it was decided the inverter model should use the datsheet value as an upper bound of the thermal resistance. In future work, accurate modelling of the package internals should be performed to determine its thermal resistance at cryogenic temperatures. This

would require the dimensions of the transistor's internal structures to be known, likely requiring collaboration with the manufacturer.

In52/Sn48 solder is used to attach the copper heat sinks to the transistor thermal pad. The thermal conductivity of the solder is $34\,\mathrm{W\,m^{-1}\,K^{-1}}$ [110], the solder joint thickness is conservatively assumed to be 0.1 mm over the area of the GS66516T thermal pad. A thermal resistance of $0.06\,\mathrm{K\,W^{-1}}$ resistance is calculated, which is negligible in all cases compared to the package junction to casing thermal resistance.

4.3.2 Heat sink

In this model the heat sinks finned faces are assumed to be in a room temperature air flow or submerged under liquid nitrogen. The heat sink thermal resistance is modelled using standard solutions for a finned heat sink with a constant heat transfer coefficient along the length of the fin. The heat-transfer coefficient applied to the surface is dependent on the coolant fluid simulated.

The thermal resistance of the heat sink is calculated considering a thermal resistance across the copper base of the heat sink, $R_{\mathrm{b,con}}$, which is in series with the parallel combination of the thermal resistance associated with the wall/fluid interface for the wetted base area, $R_{\mathrm{b,cv}} = \frac{1}{hA_{\mathrm{b,wet}}}$, and the fins, R_{fin}.

$$R_{\mathrm{HS}} = \frac{R_{\mathrm{b,cv}} R_{\mathrm{fin}}}{R_{\mathrm{b,cv}} + R_{\mathrm{fin}}} + R_{\mathrm{b,con}} \tag{4.20}$$

The thermal resistance of the fins are calculated using the standard solution for an extended surface with a constant heat transfer coefficient, h, (adiabatic tip condition) and dividing by the number of fins, N_{fin}.

$$R_{\mathrm{fin}} = \frac{1}{N_{\mathrm{fin}} \sqrt{hP_{\mathrm{f}} \cdot kA_{c,\mathrm{fin}}} \tanh(m_{\mathrm{fin}} H)} \tag{4.21}$$

Where P_{fin} is the perimeter of the fin, $A_{c,\mathrm{fin}}$ is the cross-sectional area of the fin, H is the height of the fin, and k is the thermal conductivity of copper,

$$m_{\mathrm{fin}} = \sqrt{\frac{hP_{\mathrm{fin}}}{k \cdot A_{\mathrm{c,fin}}}} \tag{4.22}$$

The forced convection heat transfer mechanism for air cooling differs greatly from the nucleate-boiling mechanism, which is the primary heat transfer mechanism between the inverter heat sinks and the liquid nitrogen. Two different methods for calculating the heat transfer coefficient, one for air cooling and the other for cryogenic cooling, are therefore used as described in the following sections.

4.3.2.1 Air-cooling

When air cooling the inverter, an axial fan is mounted so that the airflow is directed down on to the transistor heat sinks. The velocity of the air can be calculated from the datasheet parameters of the fan. Using the average Nusselt number, $\boldsymbol{Nu}$, for a flat plate in laminar flow, the heat transfer coefficient of the surface can be estimated [111].

The $10\,\mathrm{m\,s^{-1}}$ air velocity, over the 12 mm fin gives a Reynolds number $\boldsymbol{Re} = 8000$. The Prandtl number for room temperature air is $\boldsymbol{Pr} = 0.709$. The heat transfer coefficient, h, is therefore $114\,\mathrm{W\,m^{-1}\,K^{-1}}$.

$$\boldsymbol{Pr} = \frac{\mu C_p}{k} = 0.709 \quad \text{(Prandtl number for air)} \tag{4.23}$$

Where μ is the dynamic viscosity, k the thermal conductivity, and C_P the specific heat capacity of air.

$$\boldsymbol{Nu} = \frac{hL}{k_\mathrm{air}} = 0.664\boldsymbol{Re}_L^{\frac{1}{2}}\boldsymbol{Pr}^{\frac{1}{3}} = 53 \quad \text{(Nusselt number)} \tag{4.24}$$

Where L is the height of the fin.

$$h = \frac{\boldsymbol{Nu}k_\mathrm{air}}{L} = \frac{53 \times 0.0258}{12 \times 10^{-3}} = 114\,\mathrm{W\,m^{-1}\,K^{-1}} \tag{4.25}$$

When this is applied to Eq. 4.20 a thermal resistance of $3.7\,\mathrm{K\,W^{-1}}$ is calculated.

4.3.2.2 Cryogenic pool-boiling

The boiling curve for liquid nitrogen is shown in Fig. 4.7 [112]. Below the heatflux required for boiling, heat transfer to the fluid is by convection. Once the necessary heatflux is surpassed nucleate boiling will start to occur. In this regime discrete bubbles form and detach from the surface. This is a highly efficient regime of heat transfer, with a steep rise in heatflux with increasing temperature differential. The maximum heat flux that can be dissipated in the nucleate-boiling regime is known as critical heat flux (CHF). Once this is surpassed, the heat flux is limited by conduction through a vapour layer which forms over the heated walls. This regime of boiling is known as film boiling. The vapour film greatly increases the thermal resistance of a heat sink causing a large temperature rise. Between the nucleate and film boiling regimes is transition boiling. This is an unstable regime and occurs briefly as the boiling regime transitions from nucleate to film boiling.

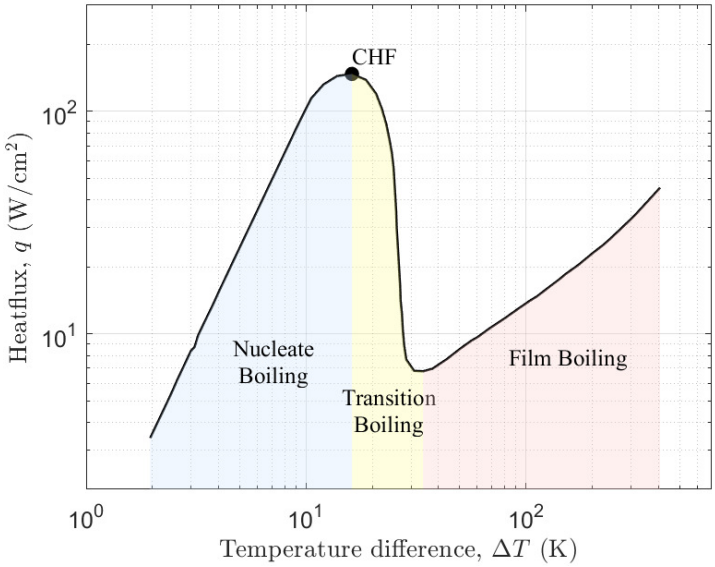


Figure 4.7: Boiling curve for liquid nitrogen [112]. The three boiling regimes (nucleate, transition and film) are shaded and labelled. The point of critical heatflux is also marked.

Nucleate boiling is the primary mechanism for heat transfer to the cryogenic coolant fluid. A large number of correlations for nucleate boiling have been proposed to relate the wall-superheat (dT) to the heat flux using dimensionless groups. The Rohsenow correlation is commonly used for predicting the temperature rise for nucleate boiling, and a specific form exists for cryogenics (Eq. 4.26 [113]). The modified form is necessary due to the significant differences of cryogenic fluids from conventional coolants, namely, the extremely low bubble contact angle, α_{f}, and higher thermal conductivity, k_{f}, [114]. The Forster and Zuber correlations (Eq. 4.27 [115]) have been shown to be predictive of experimental data for a number of cryogenic fluids [116]. The Kutateladze correlation is also recommended for cryogens [117]. To show the variation between these correlations, they are plotted in Fig. 4.8 for both nitrogen and hydrogen. Hydrogen has a higher nucleate boiling coefficient, resulting in higher heat fluxes for the same wall superheat, T_{w}, compared to nitrogen.

$$C_{\mathrm{p_f}}\frac{(T_{\mathrm{w}}-T_{\mathrm{sat}})}{\Delta h_{\mathrm{fg}}} = 0.013\left(\frac{q''_{\mathrm{w}}}{\Delta h_{\mathrm{fg}}\mu_{\mathrm{f}}}\sqrt{\frac{\gamma}{g\Delta\rho}}\right)^{\frac{1}{3}}\left(\frac{C_{\mathrm{p_f}}\mu_{\mathrm{f}}}{k_{\mathrm{f}}}\right)^{1.7}\text{(Rohsenhow Correlation)} \tag{4.26}$$

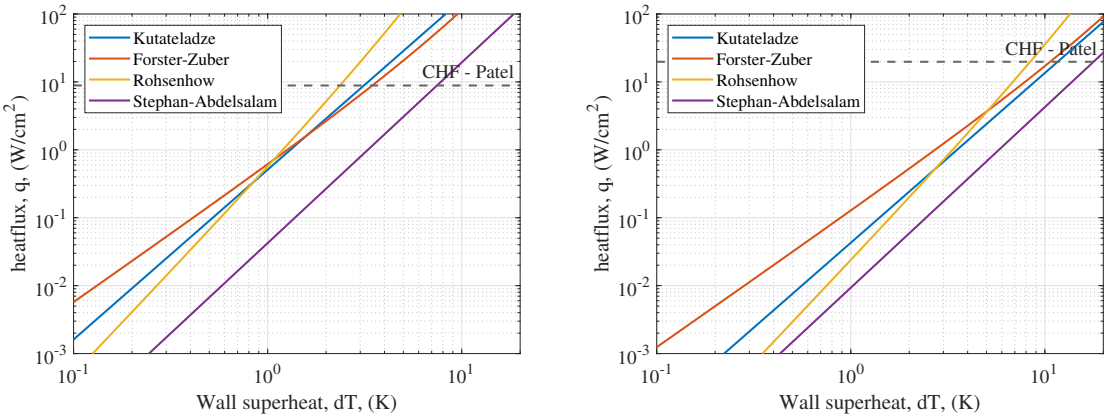
(Forster-Zuber Correlation)

$$\frac{q''_{\mathrm{w}}}{\rho_{\mathrm{g}}\Delta h_{\mathrm{fg}}}\sqrt{\frac{\pi}{\alpha_{\mathrm{f}}}}\left(\frac{\rho_{\mathrm{f}}R^{*3}}{2\gamma}\right)^{\frac{1}{4}} = 0.0015\left\{\frac{\rho_{\mathrm{f}}}{\mu_{\mathrm{f}}}\left[\frac{(T_{\mathrm{w}}-T_{\mathrm{sat}})k_{\mathrm{f}}}{\rho g\Delta h_{\mathrm{fg}}}\right]^2\frac{\pi}{\alpha_{\mathrm{f}}}\right\}^{\frac{5}{8}}\left(\frac{C_{p_{\mathrm{f}}}\mu_{\mathrm{f}}}{k_{\mathrm{f}}}\right)^{\frac{1}{3}} \tag{4.27a}$$

$$R^* = \frac{2\gamma}{P_{\mathrm{sat}}(T_{\mathrm{w}})-P} \quad \text{(Critical bubble radius)} \tag{4.27b}$$

In Eq. 4.26 and 4.27, the subscript f denotes that the property is for the liquid state. q''_{w} is the heat flux at the wall, and γ is the surface tension of the liquid. All other symbols have their standard meaning.

The CHF can be predicted using the correlation provided in [118] and is plotted on Fig. 4.8 as a horizontal line. The CHF for nitrogen is estimated to be 20 W cm^{-2} occurring at a dT of approximately 10 K (for hydrogen 9 W cm^{-2} occurring at a dT approximately between 2 K to 8 K). If the CHF is exceeded in the simulation an error is reported to constrain the model to the nucleate-boiling regime.



(a) Hydrogen (b) Nitrogen

Figure 4.8: Plots showing four commonly used boiling correlations for liquid hydrogen and liquid nitrogen. The CHF is plotted as a horizontal dashed line.

Assuming a uniform temperature across the heat sink, the heat flux over the wetted area is used to calculate the wall superheat using the Forster-Zuber correlation. This allows an estimate of the heat transfer coefficient to be made. The heat transfer coefficient is then be applied to Eq. 4.20 to give a thermal resistance for the heat sink.

In Chapter 5 a 10 x 10 mm heat sink is selected. The dimensions of this heat sink are used to calculate the thermal resistance, and the result is plotted in Fig. 4.9. The

thermal resistance is plotted against heat dissipation to show the variation caused by the selection of boiling correlation. It can be seen that the thermal resistance decreases with increasing heat dissipation, as a result of the boiling coefficient increasing for larger heat fluxes.

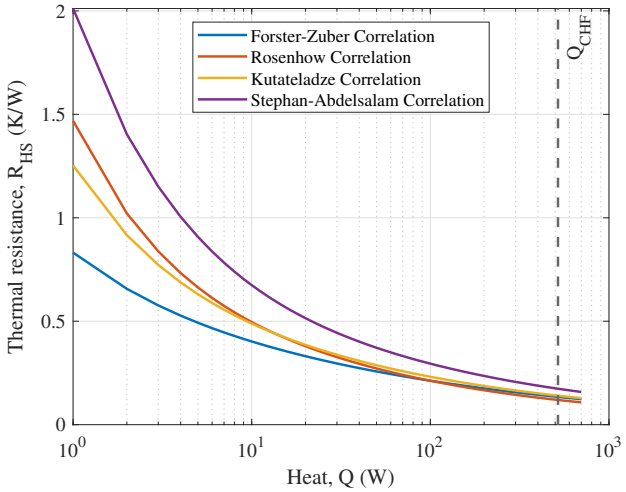


Figure 4.9: Heat sink thermal resistance against heat dissipation using different boiling correlations. The critical heat flux is plotted with a vertical line.

For 10 W of losses per transistor (approximately the largest losses measured experimentally), a junction temperature increase of 7.3 K is predicted when using the Forster-Zuber correlation, and 10 K for the Stephan-Abdelsalam correlation. At these dT the on-state resistance differs by only 1%. The choice of correlation is therefore negligible when the losses are small. The deviation increases as the heat dissipation increases, reaching 6% at 100 W of losses. Despite this, the resulting differences in modelled losses are likely less than the error due to unmodelled thermal paths, such as via the drain and source pads to the PCB which is in contact with the liquid nitrogen.

To check the assumption that the temperature is uniform in the heat sink body, the Biot number is calculated. The Biot number is a dimensionless parameter that relates the thermal resistance due to conduction within a body to the thermal resistance due to convection at the surface of the body. In bodies where the Biot number is significantly less than one, the temperature distribution can be assumed to be uniform. The heat characteristic length of the fin is used to calculate the Biot number for the small 10x10 mm heat sinks used, giving less than 0.01 regardless of correlation or heat dissipation. The assumption of a uniform temperature is, therefore, justified.

Cooling Method	Max Power (kVA)	Peak Efficiency (%)	Peak Efficiency Power (kVA)
Air	14.5	99.65	4.5
LN2	102	99.82	10

Table 4.3: Summary statistics for the simulated performance of the prototype inverter. Results for 20 kHz switching frequency.

The properties for hydrogen and nitrogen were obtained using the COOLPROP fluid properties library [12].

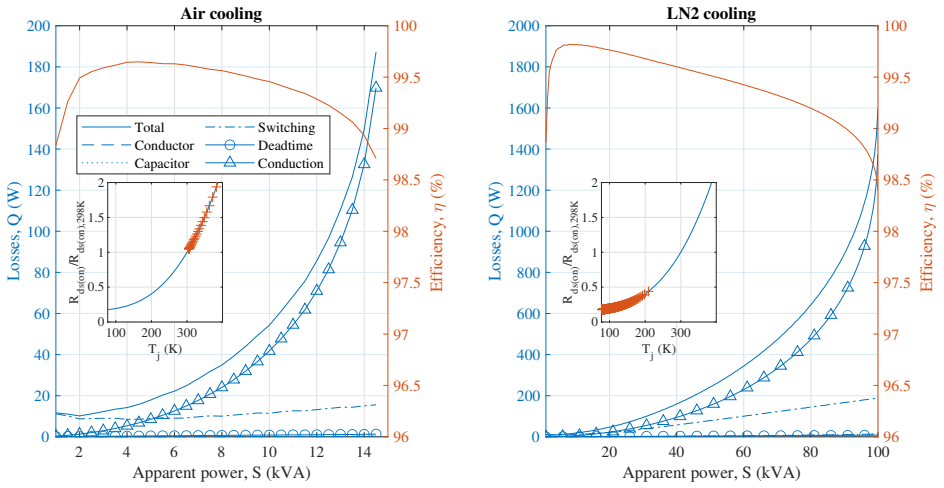
4.4 Prototype Inverter Modelling Results

In this section the modelled losses and efficiency for the prototype cryogenic inverter (discussed in Chapter 5) are presented. The modelled losses are plotted against apparent power, S.

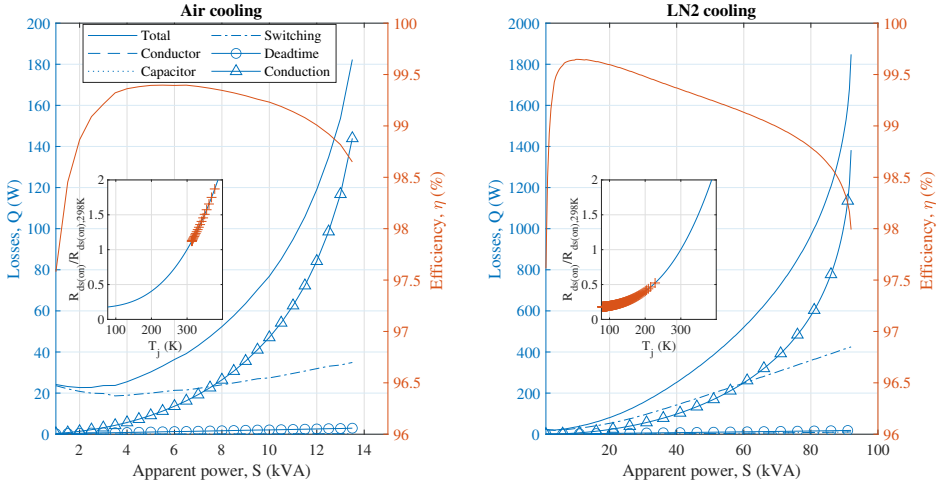
The simulation is run for the inverter using both the cryogenic pool-boiling thermal model (Section 4.3.2.2) and the room-temperature air-cooled thermal model (section 4.3.2.1). This allows an assessment of the performance gains made by cryogenically cooling the inverter compared to air cooling.

The simulation is allowed to run for increasing apparent power until the junction temperature exceeds the maximum rated temperature of the transistor, 423 K, or the system becomes thermally unstable and the simulation fails to converge. The mechanism that causes the instability is explained in Section 3.1.2.5.

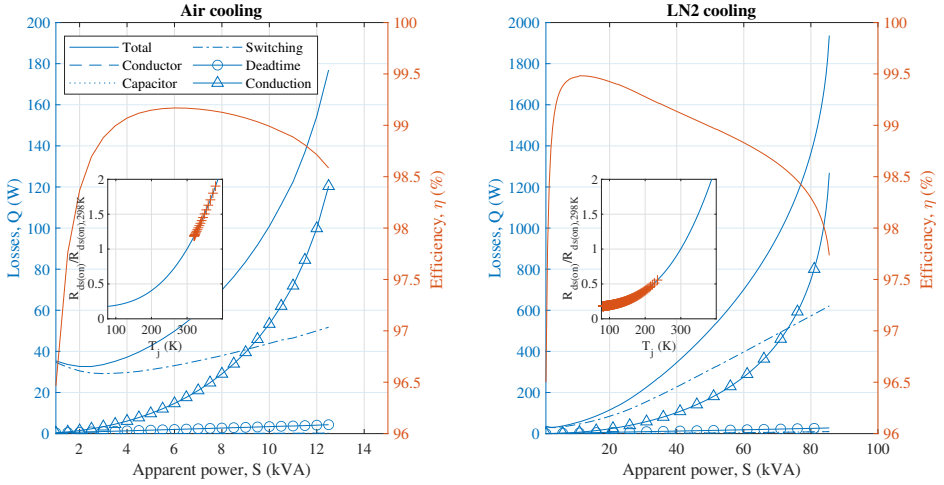
In Fig. 4.10 the inverter losses and efficiency is plotted for both air cooling and liquid nitrogen cooling. The axes are scaled differently in each column of plots. The inset on each plot shows the curve of on-state resistance against junction temperature, with the red markers showing the junction temperature at each simulated power. Plots are shown for the three different switching frequencies used in Chapter 5. The maximum apparent power predicted for the air-cooled inverter (using the lowest switching frequency, 20 kHz) is 14.5 kVA, with the constraint that the maximum junction temperature must not exceed the maximum rated temperature of the transistor (423 K) limiting the inverter power. In comparison a liquid nitrogen cooled inverter becomes thermally unstable at 102 kVA. It can be seen that, prior to failure, the conduction losses rapidly increase, scaling with both the square of the current and the monotonically increasing $R_{\mathrm{ds(on)}} - T_{\mathrm{j}}$ curve.



(a) $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$



(b) $f_{\mathrm{sw}} = 50\,\mathrm{kHz}$



(c) $f_{\mathrm{sw}} = 80\,\mathrm{kHz}$

Figure 4.10: Expected losses for the prototype inverter operating at conventional (left-hand column) and cryogenic (right-hand column) temperatures, plotted up to the thermal limit.

4.5 Model Results for an Aircraft Inverter

To investigate the effect cryogenic cooling would have for an electric aircraft the inverter was simulated for a drive-cycle representative of take-off and climb for a light aircraft. The drive cycle was provided by Ricardo PLC.

The peak power of the drive-cycle is 215 kW, greater than can be achieved with a single transistor per switch, as modelled for the prototype inverter. The hypothetical cryogenic aircraft inverter is therefore modelled with three of the GS66516T transistors in parallel per switch, to achieve the required power rating.

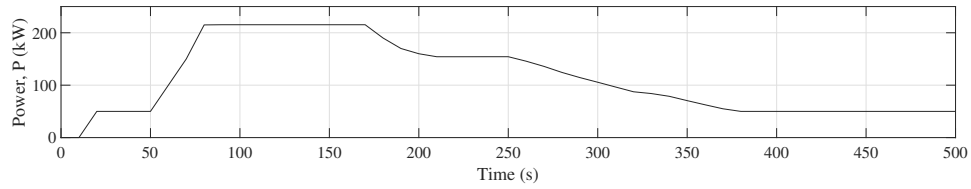
For simplicity, the motor is not modelled and is assumed to be a load with a constant power factor ($\cos\phi = 0.9$). The inverter is assumed to be cooled with liquid hydrogen or nitrogen directly. This is a simplification of a real system where intermediate cooling loops may be used.

There is a clear benefit of operating the inverter with liquid hydrogen, as the lower saturation temperature of the fluid causes reduced conduction losses at peak power. The slope of the $R_{\mathrm{ds(on)}} - T_{\mathrm{j}}$ curve is very shallow across the range of dT's that occur with hydrogen cooling compared to nitrogen, leading to a reduction in the conduction losses, most visibly at peak power.

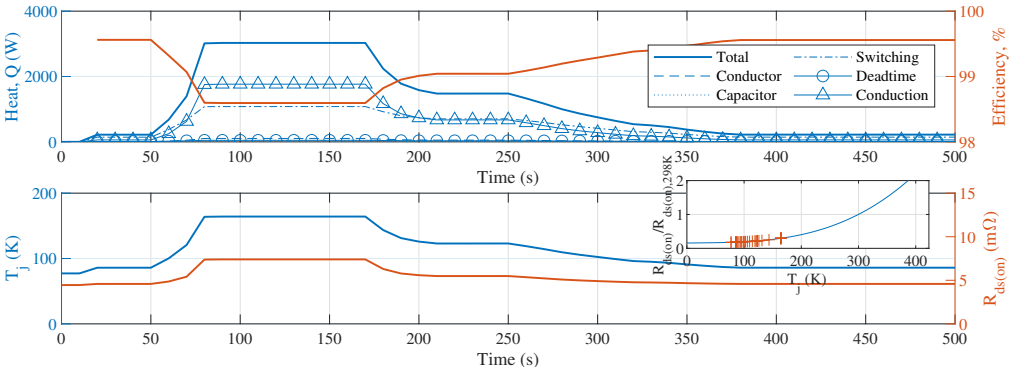
If the same inverter (with three parallel transistors) is modelled with air cooling, the equivalent air-cooled inverter would only be able to supply 17% of the required peak power.

In a practical aircraft application direct air-cooling of the transistors is unlikely to yield a viable inverter design due to the high heat fluxes and large thermal resistance (for the air cooled prototype inverter the heat sink thermal resistance contributed $3.7\,\mathrm{K\,W^{-1}}$ to the thermal resistance path, 14 times larger than the junction-to-casing thermal resistance). To demonstrate the improvement of cryogenic operation versus even the best ambient-temperature cooling, ideal cooling is assumed for the conventionally cooled case, meaning the thermal resistance to room temperature ambient is modelled as only the junction to casing thermal resistance of the package. Even with ideal cooling, five parallel transistors are required per switch to reduce the conduction losses to a level that does not cause a junction over-temperature. A real system with non-ideal cooling would have a significantly lower power rating than modelled.

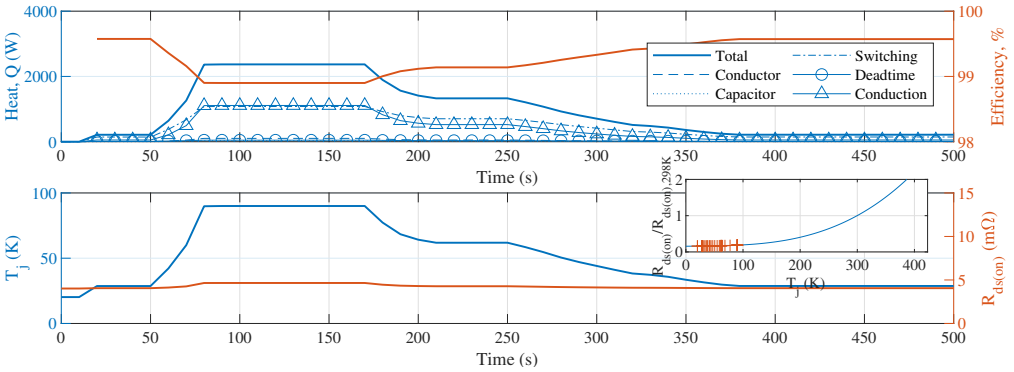
The losses at peak power in the ideal room temperature inverter are three times the total losses incurred with a liquid hydrogen cooled inverter. Resulting in a peak power efficiency of 96.7% compared to 98.9% with hydrogen cooling. For the cruise phase of the flight, the losses are 68% greater in the room temperature inverter.



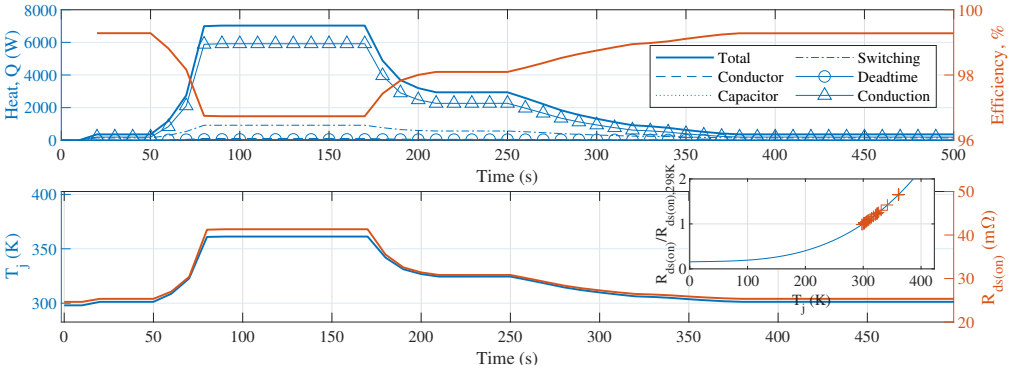
(a) Power profile.



(b) Liquid nitrogen cooling ($n_\mathrm{p} = 3$).



(c) Liquid hydrogen cooling ($n_\mathrm{p} = 3$).



(d) Ideal room-temperature cooling ($n_\mathrm{p} = 5$).

Figure 4.11: Simulated losses and efficiency for an inverter, suitable for a light-aircraft propulsion system. The simulation is run for a representative drive cycle for an electric aircraft take-off. Three cooling methods are plotted with the minimum number of parallel GS66516T transistors required to achieve the peak power of the drive cycle.

Giving a cruise efficiency of 99.3% and 99.6% for the air-cooled and hydrogen-cooled inverters respectively.

The lower losses translate to a 0.4% reduction in the fuel required for a 5 hour flight, with 1.5% less fuel being consumed in the take-off phase. This assumes a hydrogen fuel cell efficiency of 50%, which is typical for current fuel cells [119]. Although the cryogenic inverter shows a significant reduction in losses modelled, both inverters modelled have high operating efficiencies, especially in the cruise phase, so further improvement in efficiency yield only a marginal changes to the overall fuel requirements. It should be noted though that the efficiency and delivery of the required peak power in the conventionally cooled inverter necessitated increasing the number of transistors, increasing the size and complexity of the inverter.

4.5.1 Efficiency Requirements

As described in Chapter 1, to cryogenically cool the inverter using the hydrogen fuel, the losses must be dissipated in the cryogenic hydrogen flow. The flow has a limited cooling potential, if the inverter losses are too great it will not be possible to cryogenically cool the inverter in this way. This suggests a minimum efficiency for the inverter. This can be extended to the minimum efficiency of a complete cryogenic propulsion system using the same analysis.

In an open system, the fluid enthalpy is used to calculate the change in quality and temperature of the fluid in response to heat input and work done, as described by the first law of thermodynamics given in Eq. 4.28.

$$q - w = h_2(P_2, T_2) - h_1(P_1, \chi_1) \tag{4.28}$$

In Eq. 4.28 h_1 & h_2 are the enthalpy of the fluid before and after being heated by the inverter. The work done, w, is assumed to be small.

$$q \approx \Delta\chi \cdot \Delta h_{\mathrm{fg}} + \int_{T_{\mathrm{sat}},P}^{T_{\mathrm{out}}} C_{\mathrm{p}}(T, P)\mathrm{d}T \tag{4.29}$$

This can be approximated as per Eq. 4.29, where χ is the vapour quality of the fluid, C_{p} is the specific heat and Δh_{fg} is the latent heat of vaporisation.

The required mass flow rate of liquid hydrogen fuel, to reject the losses generated by the inverter is found by equating the heat generated, $\dot{Q} = P_{\mathrm{DC}}(1 - \eta)$, and heat dissipated to the fluid, q.

$$\dot{m}_{\mathrm{c}} = \frac{(1 - \eta)P_{\mathrm{DC}}}{\Delta\chi \cdot \Delta h_{\mathrm{fg}} + \int_{T_{\mathrm{sat}},P}^{T_{\mathrm{out}}} C_{\mathrm{p}}(T, P)\mathrm{d}T} \tag{4.30}$$

The fuel flow rate is found simply by calculating the electrical power generated by the hydrogen, Eq. 4.31. HHV efficiency, η_{HHV}, is typically used to evaluate a HFC [120], where the input power is the product of the mass flow rate and the higher heating value, Δh_{HHV}.

$$\dot{m}_{\mathrm{HFC}} = \frac{P_{\mathrm{DC}}}{\Delta h_{\mathrm{HHV}} \cdot \eta_{\mathrm{HHV}}} \tag{4.31}$$

The ratio of the two flow rates λ (Eq. 4.32), must be equal to or greater than one so that the cryogenically cooled components do not overheat. A value greater than one indicates that more hydrogen is used for cooling than for fuelling the propulsion system, and is additional mass that must be transported, and will be vented or consumed by the HFC during flight.

$$\lambda = \frac{\dot{m}_{\mathrm{c}}}{\dot{m}_{\mathrm{HFC}}}, \lambda \geq 1 \tag{4.32}$$

P_{DC} can be eliminated by substituting Eq. 4.30 into Eq. 4.31. Rearranging for system efficiency and substituting in λ for the ratio of mass flowrates results in Eq. 4.33, giving the minimum efficiency.

$$\eta => 1 - \lambda \left(\frac{\Delta\chi \cdot \Delta h_{\mathrm{fg}} + C_{\mathrm{p}} \Delta T}{\Delta h_{\mathrm{HHV}} \cdot \eta_{\mathrm{HHV}}} \right) \tag{4.33}$$

If $\lambda = 1$ (the case when no additional hydrogen is available for cooling), the minimum efficiency is 95.4% during take-off and 96.5% in the cruise phase. The assumptions made for the change of hydrogen vapour quality, change in temperature and HFC efficiency are laid out in Appendix B. The efficiencies calculated are sufficient for hydrogen cooled inverter modelled.

4.6 Conclusion

In this chapter a method for estimating the losses and peak power in a cryogenic inverter is presented. A performance comparison is conducted for the prototype inverter discussed in Chapter 5, operating with room-temperature air-cooling and direct liquid nitrogen pool boiling. This is important as the heat generated and power conducted determines important design parameters for the experimental setup, such as sizing of the supply and load, the size of the heatsinks and conductors. It also allows a prediction of the peak efficiency and power to be made which can then be validated experimentally.

The simulation indicates that the peak efficiency of the cryogenically cooled inverter will be 99.82% at 10 kVA, while the air-cooled peak efficiency is lower at 99.65%

at 4.5 kVA. Due to the low thermal resistance with two-phase pool boiling and reduced conduction losses from the lower $R_{\mathrm{ds(on)}}$, much higher power is expected to be achieved before thermal failure occurs when the inverter is cryogenically cooled. The simulation indicates a seven-fold increase in peak power.

The simulation is used to demonstrate the reduction in active area and the increase in efficiency that could be achieved if a cryogenically cooled motor drive were implemented for a light-aircraft propulsion system, as well as quantifying the reduction in hydrogen fuel consumed, thereby answering research question 1b.

A method for calculating the required efficiency of a cryogenic system, that dissipates its losses to a flow of hydrogen fuel, is presented. The results of this calculation demonstrates that the predicted efficiencies for the inverter are sufficient to meet this requirement. By maximising the efficiency of the cryogenic inverter, greater losses can be dissipated in other elements of the propulsion system such as the motor or DCDC converter that could also be cryogenically cooled.

Chapter 5

Cryogenic Inverter

5.1 Introduction

This chapter discusses the design and testing of a cryogenic prototype inverter. It also explains a method for measuring the losses from the boiling rate of liquid nitrogen and presents the results of the measurements.

This chapter aims to address the following research questions:

1c. *Losses in a cryogenic GaN inverter are expected to be very small compared to the apparent power. How can the efficiency be accurately measured for a cryogenic inverter, in order to quantify the improvement in performance?*

2b. *Do new mechanisms lead to failure for a GaN transistor at cryogenic temperature or are conventional failure modes exacerbated by the change in the properties of the GaN transistor at cryogenic temperatures?*

2c. *A cryogenically cooled GaN inverter has not yet been demonstrated in the literature at a power greater than* 1 kW*. Is a cryogenic GaN inverter suitable for a motor drive application achievable with current technology, and if so, what is its maximum achievable power and efficiency?*

The inverter underwent a significant revision after flaws in the initial design were identified. The focus is on the final inverter design, but reference is made to the initial design to demonstrate the complications of cryogenically cooling an inverter and to justify the design revisions.

The inverter was built around the GS66516T transistors which have been characterised and modelled in earlier chapters.

5.2 Inverter Design

The electrical components of the inverter are divided over three vertically stacked PCBs as shown in Fig. 5.1. They are referred to as:

1. The power board
2. The gate driver board
3. The supply board

The PCBs are mounted to an aluminium tube that forms a vessel for liquid nitrogen. Components for measuring the boiling rate of the liquid nitrogen are mounted to the top of the vessel along with a vented lid. The complete assembly is shown in Fig. 5.2.

5.2.1 Power Board

The power board is a standard FR4, 4 oz, 4-layer PCB. The top side of the power board is directly exposed to the liquid nitrogen, on which the cryogenically cooled components are populated. These are the six GaN HEMTs that form the full-bridge and the decoupling capacitors (Fig. 5.1a). Individual skived copper heat sinks, with similar footprints to the transistors are soldered directly to the thermal pads of the transistors (Fig. 5.1b). Using individual heat sinks means electrically insulating Thermal Interface Material (TIM) is not required. TIMs regularly used in power electronics applications are not rated for cryogenic temperatures and would not be expected to perform adequately at cryogenic temperatures. The power board forms the base of the liquid nitrogen vessel, and is sealed to the end face of the 100 mm OD aluminium vessel wall (Fig. 5.1d).

5.2.2 Gate Driver Board

The gate driver board is mounted to the back side of the power board, and is therefore not exposed directly to the liquid nitrogen. Header pins are soldered to through-hole pads on the power board to provide mechanical and electrical connections (Fig. 5.1c). Solder connections were essential, as press fit board-to-board connections were found to be unreliable in forming electrical connections at cryogenic temperatures. The spacing between the gate drive PCB and the power PCB was controlled using small spacers of 1.8 mm thickness. This was the minimum spacing that ensured clearance between the components on the gate driver PCB and the back

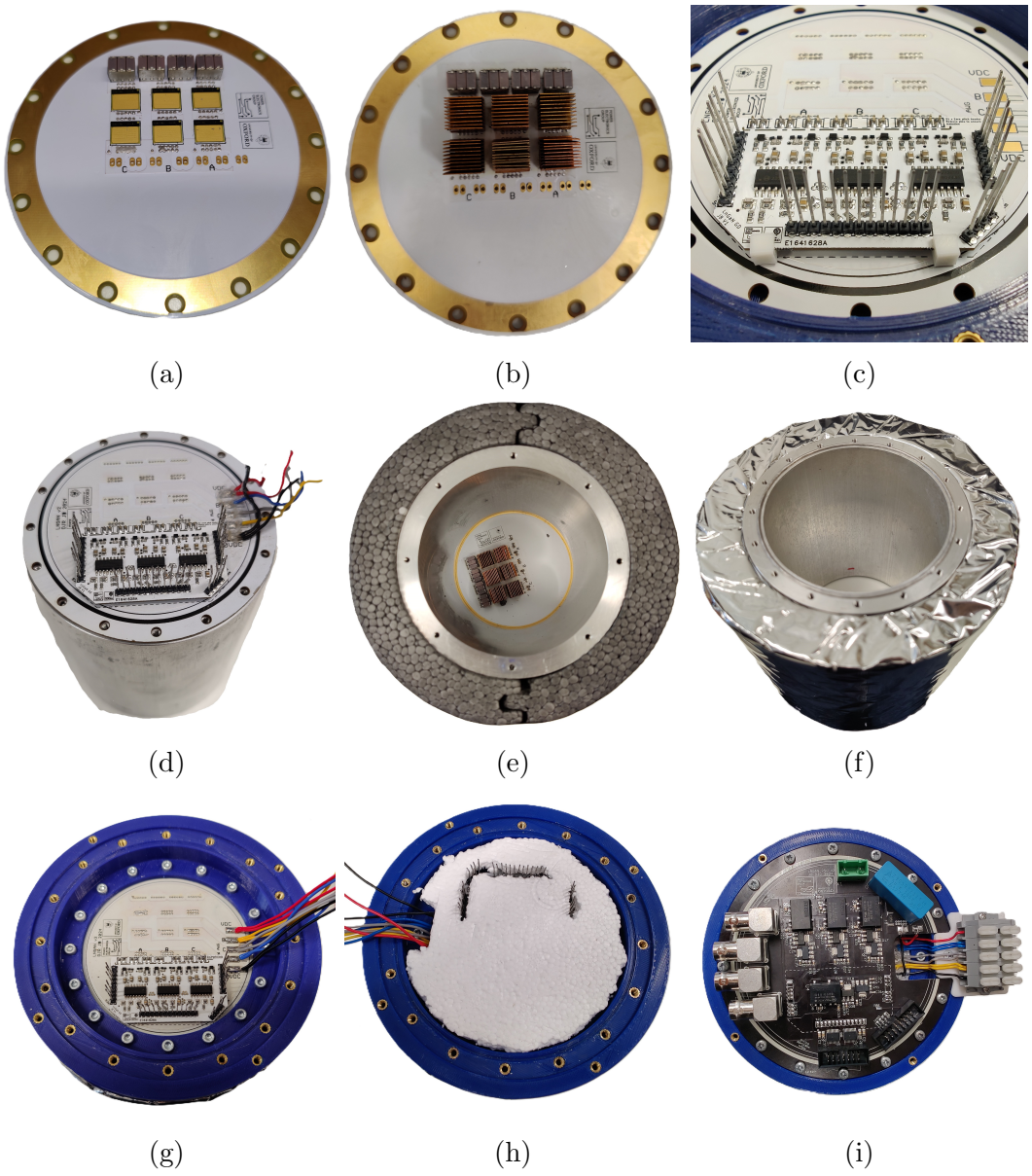
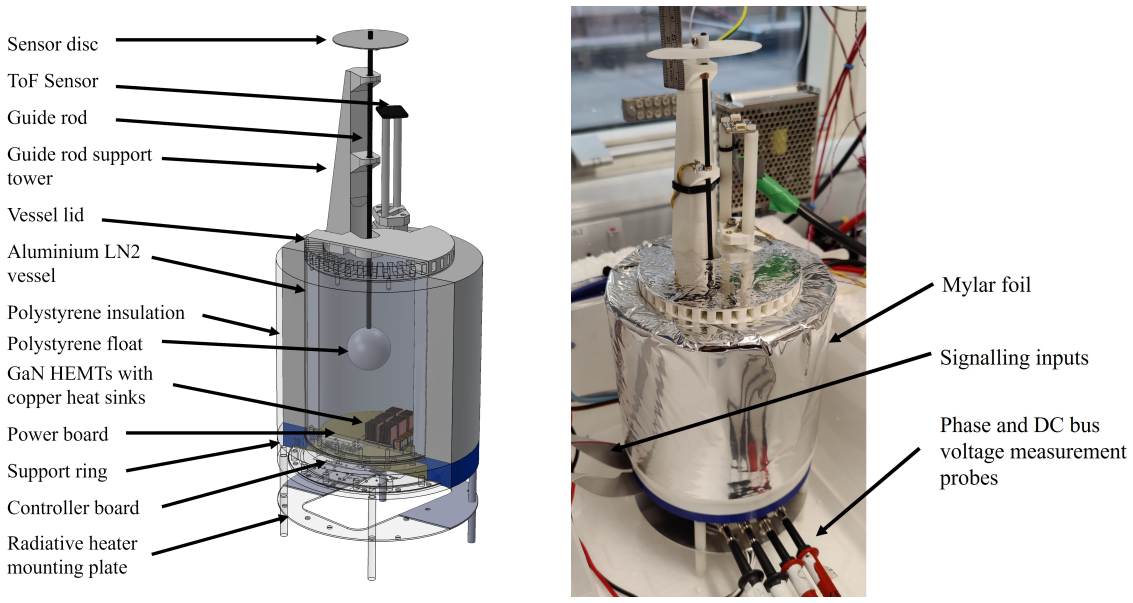


Figure 5.1: Assembly process of the cryogenic inverter. (a) GaN HEMTs are soldered to the power board, (b) finned heat spreaders are soldered to the thermal pad of the transistors with In/Sn solder, (c) gate driver board is attached to the power board with soldered header pins. 3D printed support clips are used to set the air gap. (d) shows how the power board is positioned relative to the LN2 vessel (e) polystyrene insulation is clamped around aluminium LN2 vessel, (f) mylar foil is wrapped around insulation and a ring of indium solder wire is placed into the o-ring groove (g) the power board is clamped to the LN2 vessel with the PETG support ring compressing the indium o-ring, (h) a polystyrene insert is positioned above the power board, slots are cut for the inter-board header pins and power cables, (i) the supply board is mounted to the PETG support ring, the header pins are soldered and the power wires connected to a terminal block.



(a) (b)

Figure 5.2: Section-view taken from CAD and an image of the inverter test assembly.

side of the power board, while minimising the gate loop inductance caused by the inter-board spacing. The design of the gate driver board is detailed in Section 5.3.5.

5.2.3 Supply Board

Electrical components are not typically rated for cryogenic temperatures, and when tested have varying levels of tolerance to these extremes. Components which have not been shown to operate at cryogenic temperatures are populated on a supply board that is kept at or above room temperature. These include:

1. Isolated DC/DC converters and DC/DC regulators for gate voltage supplies.
2. BNC terminals for measuring V_{DC} and the midpoint voltages V_{a}, V_{b} and V_{c}
3. Polypropylene film bus capacitor
4. IDC connector for gate signals
5. IDC connector for providing current to the gate drive power supplies, the gate driver board heater and the PT1000 temperature sensors

The supply board is offset from the power board by 13 mm, with tall header pins bridging the boards to make electrical connections (Fig. 5.1i). A 3D printed support ring locates the supply board to the assembly. The support ring has the additional

function of evenly spreading the compression force over the sealing interface between the power board and the aluminium vessel (Fig. 5.1g). To reduce convective and radiative heat transfer between the supply board and the power board, a polystyrene insert packs the space between boards (Fig. 5.1h).

5.2.3.1 Heat sink

Using cryogens such as liquid hydrogen or liquid nitrogen as a coolant is desirable because of their very low saturation temperatures. The drawback is that cryogens have lower critical heat flux (the point at which a layer of evaporated vapour is formed between the heated surface and the liquid acting as a thermal insulator). For nitrogen, the critical heat flux is approximately $20\,\mathrm{W\,cm^{-1}}$, five times lower than for water. This has been shown to be a limitation for cryogenic power electronic design [84].

The thermal pad of the GS66516T is $0.46\,\mathrm{cm^2}$, which means that the critical heat flux would be exceeded if losses greater than 9.3 W were generated per transistor. This is significantly less than what the modelling conducted in Chapter 4 suggests will be expected. In Chapter 3 it is shown that transistor failure will occur prior to the CHF limit being exceeded if a sufficiently large heat spreader is used.

A skived 10 x 10 mm copper heat sink was selected due to its large surface area and footprint similar to the GS66516T transistors. Methods for determining the thermal resistance and critical heat of a finned heat sink in a pool of cryogenic fluid have been explained in Chapter 4, Section 4.3. These methods were applied to the heat sink showing that a critical heat of 520 W could be expected to be achieved over the $26\,\mathrm{cm^2}$ wetted area.

The heat sink was attached to the thermal pad using an indium-tin alloy (In52-Sn48) solder. The In52-Sn48 solder has a lower reflow temperature than the leaded solder that was used to attach the transistor to the power board PCB. This meant that the assembly could be performed in a two-stage process. In the first stage, the transistors were first soldered to the PCB, using leaded solder and a reflow oven. After inspecting the quality of the solder joints, the heat sinks were soldered by hand to the thermal pads of the transistors at a lower temperature, with no risk of reflowing the leaded solder. In52-Sn48 is also a soft solder compared to typical SAC or Pb solders, reducing the stress at the solder joint caused by CTE mismatches between the transistor and heat sink materials [40]. Solder cracks caused by cyclic thermal stresses are a common failure mode in power electronics hardware at conventional temperatures. In a conventionally cooled converter the typical change in temperature

is approximately 100 K compared to the 278 K differential between room temperature and the boiling point of hydrogen. The larger temperature change will lead to larger stresses in the materials, and compounding this, many materials become increasingly brittle at cryogenic temperatures. A topic of future research would therefore be to investigate the reliability of soldered connections over the expected cycle life of an aircraft motor drive.

5.2.3.2 Vessel insulation

To increase the possible test duration, the LN2 vessel required insulating to limit the boil-off rate caused by heat leak. Insulating the vessel also reduced the variability of the calorimetry measurements to changes in ambient conditions.

The vessel was insulated using polystyrene pipe insulation with 20 mm thickness (Fig. 5.1e). As shown in Fig. 5.3, this effectively reduced the heat leak via the vessel walls to $\sim$ 15 W, a similar magnitude to that produced by the inverter. This was deemed sufficient for the experimental apparatus to function effectively.

The heat leak, Q_{hl}, through the wall of the vessel is calculated iteratively using Eq. 5.1. The temperature of the outside surface of the insulation is calculated as: $T_{\mathrm{ins}} = T_{\mathrm{LN2}} + Q_{\mathrm{hl}} R_{\mathrm{con}}$. The aluminium walls of the vessel have a negligible thermal resistance compared to the polystyrene pipe insulation used (polystyrene has a thermal conductivity of $0.035\,\mathrm{W\,m^{-1}\,K^{-1}}$). A convection coefficient of $5\,\mathrm{W\,m^{-2}\,K^{-1}}$ is used for free convection on a vertical surface in air.

$$Q_{\mathrm{hl}} = \frac{T_{\mathrm{a}} - T_{\mathrm{LN2}}}{R_{\mathrm{con}} + R_{\mathrm{cv}}} + \epsilon\sigma A(T_{\mathrm{a}}^4 - T_{\mathrm{ins}}^4) \tag{5.1}$$

Where ϵ is the emissivity of the insulation and σ is the Stefan–Boltzmann Constant.

The effect of the insulation thickness is shown in Fig. 5.3. Radiation from the surroundings to the assembly was also calculated to be a significant source of heat leak. For this reason, the vessel and lid of the vessel were wrapped in Mylar foil negating the heat leak via radiation by reducing the the emissivity of the surface (Fig. 5.1f). The insulation thickness would have had to been increased by 2.5 times to achieve the same reduction in heat leak that was achieved by wrapping the insulation with Mylar foil.

5.2.3.3 Power board LN2 seal

The power board forms the base of the liquid nitrogen vessel with the top side of the power board exposed directly to the liquid nitrogen, submerging the GaN HEMTs

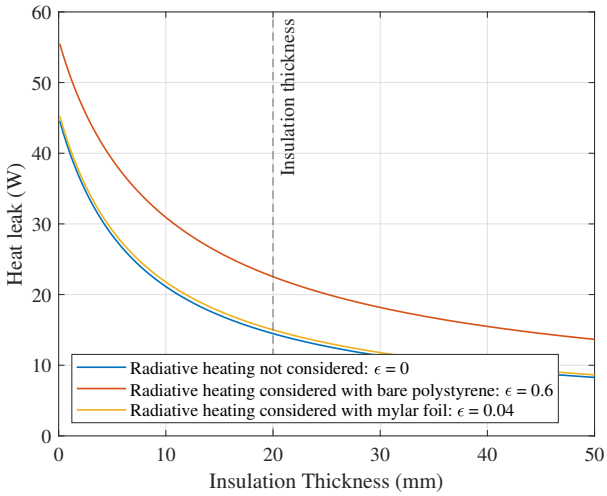


Figure 5.3: Heat leak through the vessel walls as a function of insulation thickness.

and the decoupling capacitors. An aluminium tube with 80 mm ID, 100 mm OD, forms the wall of the vessel. The interface between the end of the aluminium tube and the power board is sealed with a loop of indium wire. Indium is a soft metal that remains ductile at cryogenic temperatures. A circular o-ring groove with a semicircular profile is machined into the end of the aluminium cylinder. The diameter of the semicircular profile matches the diameter of the wire into which the wire is seated. This can be seen in Fig. 5.1f. Compression is then applied to the seal through the PCB and the support ring with 16 equispaced bolts. Using this method, a repeatable seal was achieved. The indium wire is cold-drawn from cast ingots through an orifice of the required diameter using a manual press. Vias on the power board are plugged with Pb-Sn solder to prevent liquid nitrogen from leaking through them.

5.2.4 Electrical Design

The inverter topology is a three-phase bridge composed of six GS66515T transistors, as described in Chapter 4. Four units of inline ceramic C0G capacitors, packaged in metal frames, are positioned close to the drain terminals of the top transistors in the three half-bridges. The metal frames of the capacitors serve to prevent thermally induced mechanical stress on the brittle ceramic capacitors. The switched current commutation loop (SCCL) runs below the transistors on the second PCB layer below the transistors to minimise loop area and in turn inductance. The gate paths are also on this layer, as shown in Fig. 5.4.

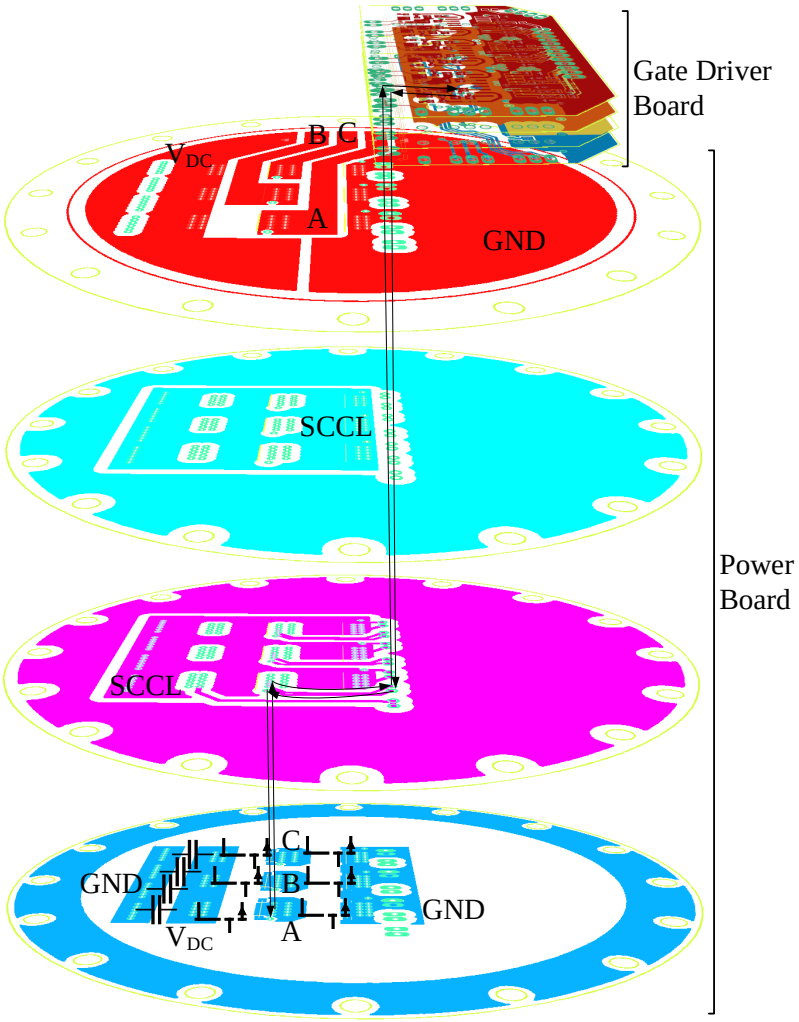


Figure 5.4: Copper layers in the power board and gate driver board, showing the stack-up three-dimensionally. The compromised gate driver loop is drawn for the phase A upper transistor.

5.3 Cryogenic Failure Modes

A number of inverter failure mechanisms were identified that were caused by the cryogenic temperature, these were overcome and are subsequently discussed in this Section.

5.3.1 Frosting and Condensation

The temperature distribution on the supply board indicates that the primary heat leak path is via conduction through the board-to-board header pins. The VDC pin had the shortest thermal path to the liquid nitrogen, and was observed to accumulate frost. This risked causing short circuits between the positive DC rail and the negative or the isolated control circuits. Despite the localised frosting, the heat leak from ambient keeps the supply board at a sufficiently high temperature that the components on this board function as expected. Additional radiative heating was used to prevent frost forming on the supply board in the regions close to the board-to-board connectors. A matt black soldermask was selected for the supply board to increase the fraction of absorbed radiation. After frost was observed on the VDC pin, 3D printed covers were placed over the pins to prevent moist air circulating around them. The exposed high voltage junctions were potted with silicone RTV and conformal coating was applied to the exposed side of the supply board to decrease the risk of short circuit if any moisture were to accumulate.

A slot is milled into the supply board to pass the DC and phase cables through to the power board. In the first revision of the inverter, the high current paths were routed via traces and connectors on the supply board, which created a significant heat path from the liquid nitrogen to the supply board. With this original configuration, frost accumulated on the supply board, despite additional radiative heating.

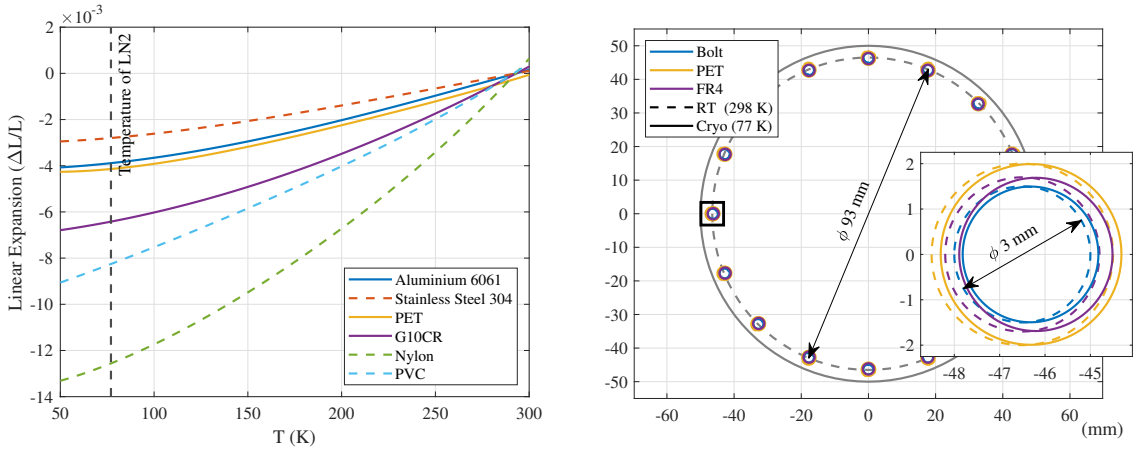
5.3.2 Thermal contraction

When designing assemblies for cryogenic temperatures, it is essential to consider how the dimensions of mated components will contract at cryogenic temperature. For example, on a PCB, with length scales of approximately 100 mm, features such as mounting holes will move significantly, meaning that the mounting hole and the fastener will not align (assuming the part to which it is mounted is made of a dissimilar material). This will induce stresses in the PCB where the edge of the hole and faster interfere. Most materials become increasingly brittle at cryogenic temperatures.

Combined with induced stresses, this can easily lead to components fracturing or shattering.

To locate the PCBs in the assembly, a PETG support ring was 3D printed. PETG was selected due to the lower CTE mismatch of PETG ($60\,\mu m\,m^{-1}\,K^{-1}$) and aluminium ($21\,\mu m\,m^{-1}\,K^{-1}$ to $24\,\mu m\,m^{-1}\,K^{-1}$) compared to other common FDM printing materials. PETG and PLA are both considered durable at cryogenic temperatures, whereas ABS is not recommended [121]. Multiple 3D printed parts, have either been submerged in liquid nitrogen or been exposed to cryogenic temperatures, during this project. With the exception of a part printed from Formlabs High Temp Resin, which shattered when exposed to cryogenic temperatures, 3D printed parts printed in PLA or PETG have been found to be robust and reliable.

Brass-threaded inserts are heat-set into the PETG to mount components. Threaded inserts in the PETG were avoided at locations that experienced cryogenic temperatures because large stresses would be induced in the PETG. The stresses occur as a result of the interference fit of the brass in the PETG and the CTE mismatch of the PETG and brass. The design uses large diameter screw clearance holes to ensure clearance is maintained once the materials have contracted at reduced temperature. The CTEs of the materials in a bolted stackup were selected to have higher CTEs than the steel bolts to ensure that the compression in the bolted joint would not increase, which may cause damage to the parts under compression.



(a) (b)

Figure 5.5: Plots showing the effect of thermal contraction at cryogenic temperatures. (a) Linear expansion of the materials used in the assembly (solid line) as well as other considered materials for comparison (dashed) data from [98], [122]. (b) Position of screw clearance holes at the interface of the powerboard (FR4), support ring (PET) and LN2 vessel (aluminium).

The linear expansion ratio for PET, G10 and Aluminium which were used in the assembly are plotted in Fig. 5.5a along with other materials which were rejected for comparison. No data was available for the coefficients of thermal expansion at cryogenic temperatures for PETG or FR4. Instead, PET and G10 are plotted. PETG is a copolymer of PET, and FR4 is a flame retardant grade of G10, so both should have material properties similar to the materials used.

To ensure clearances were maintained at the bolted interface of the support ring, power board, and LN2 vessel, the temperature-dependent coefficients were used to determine the dimensions of the parts after they had contracted at cryogenic temperatures. The bolts thread into the aluminium vessel and so are fixed relative to the vessel as it contracts. The room temperature and cryogenic dimensions are plotted in Fig. 5.5b. The inset shows the leftmost bolted joint; the relative movement of the holes can be seen with the room temperature dimensions shown with dashed lines and solid lines at cryogenic temperatures. There is the least clearance between the bolt and the FR4 power board, 75 µm, significantly less than the initial 200 µm clearance at room temperature. Due to the uncertainty in the CTE of PETG, a greater hole clearance was allowed to ensure clearance at cryogenic temperatures.

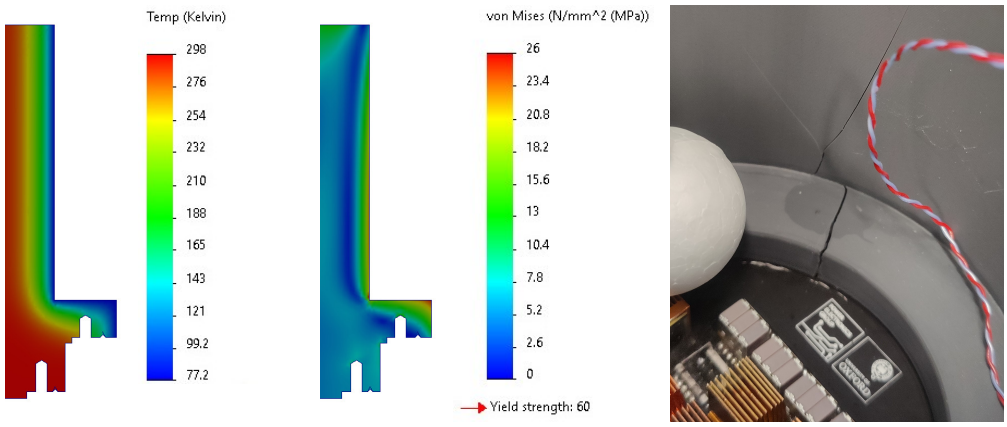
5.3.3 Material of LN2 vessel

In addition to considering how mated parts will contract relative to each other, it is also important to consider how temperature distributions within a part will induce stress that can lead to failure.

In the initial design, it was decided to use a plastic-walled vessel for the liquid nitrogen. This would reduce the heat leak via the vessel walls compared to a more thermally conductive metal vessel, and consequently was machined from nylon.

After multiple thermal cycles, the vessel cracked along the inner surface as shown in Fig. 5.6c. The power board was also damaged by the mechanical shock from the vessel fracturing. This was after withstanding between 5 and 10 thermal cycles before failure.

The cracking presumably occurred due to fatigue in the material caused by the thermal cycling. Stress develops in the material because the region closest to the liquid nitrogen is significantly colder than the outside diameter. Simulation indicates the outside diameter can be expected to be at effectively room temperature even one minute after the liquid nitrogen is added. The low thermal conductivity of the nylon means that the temperature distribution develops over several minutes to a steady state. The thermal gradient and the resultant material contraction create a stress



(a) (b) (c)

Figure 5.6: Results from a thermal-mechanical simulation performed in SOLIDWORKS, to demonstrate the stresses induced by the temperature distribution in the nylon vessel. Plots show the result 60 s after liquid nitrogen is added to the vessel, alongside a photo of the failed part. (a) Temperature distribution, (b) Stress distributions, (c) Image showing the failed vessel which cracked after repeated thermal cycling.

distribution through the plastic that has a peak stresses at the right angle steps in the vessel wall, which act as stress concentrators.

To illustrate the issue, a thermal-mechanical finite-element simulation was performed, estimating the temperature and stress distribution in the wall of the vessel. The simulation assumes that the Nylon is initially at room temperature, and a temperature boundary condition is applied to the surfaces in contact with the liquid nitrogen. The temperature and stress distribution can be seen in Figs. 5.6a and 5.6b, respectively. The simulated peak stresses were significant, 26 MPa, 43% of the yield stress of Nylon.

Small imperfections in the material develop into small cracks as a result of thermal cycling and induced stresses. Once the crack reaches a critical length, rapid crack growth will occur fracturing the component.

The vessel was redesigned from aluminium, which has a thermal conductivity four orders of magnitude greater than that of nylon. Therefore, the large thermal gradients and consequent stresses will not occur within the vessel walls.

5.3.4 Board-to-board connectors

It is important to consider how electrical connections will be affected by cryogenic temperatures. Probing and testing connections to identify issues once the converter

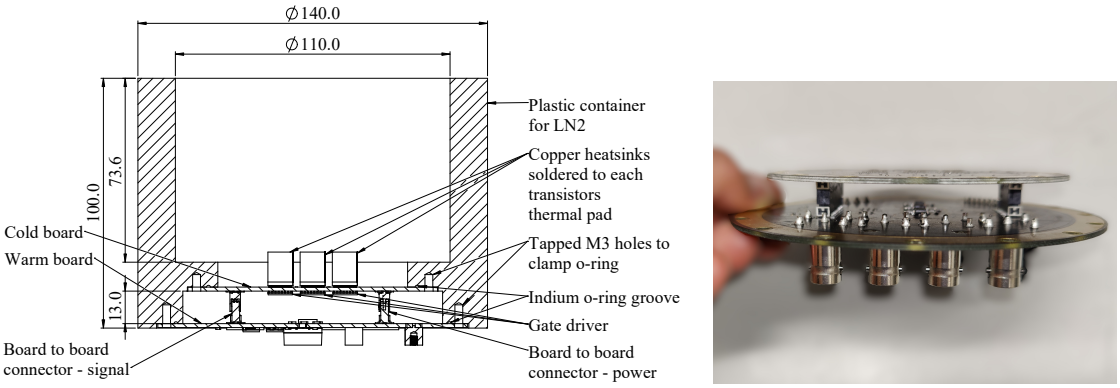
is at cryogenic temperatures is challenging, making the selection of appropriate connector types very important.

In the initial inverter design, board-to-board connectors from Harting's Har-flex family of connectors were used to transfer power and signals between the power and supply boards. These connectors can be seen in Fig. 5.7. Using these connectors made assembling the inverter much simpler, compared to the soldered header connections used in the final inverter design. The shortcoming of the connectors, was that at cryogenic temperatures the press fit connections were unreliable. Mechanical contractions due to the cryogenic temperatures within the mated sprung pins and across the PCBs caused open circuits in the 1.27 mm pitch signal connector and increased connection resistance of the pins in 2.54 mm pitch power connector. The increase in contact resistance was by between a factor of 2 and 3, depending on the pin measured.

When the temperature returned to room temperature, the open circuits and high contact resistance would no longer be present, making fault finding challenging.

For the second inverter design, press-fit connectors were not (used in favour of soldered header pins).

Bolted electrical connections were also found to be consistently reliable, but the bolts could not be loosened until the assembly had warmed to near room temperature, due to CTE mismatch between the steel bolt and the threaded brass terminal.



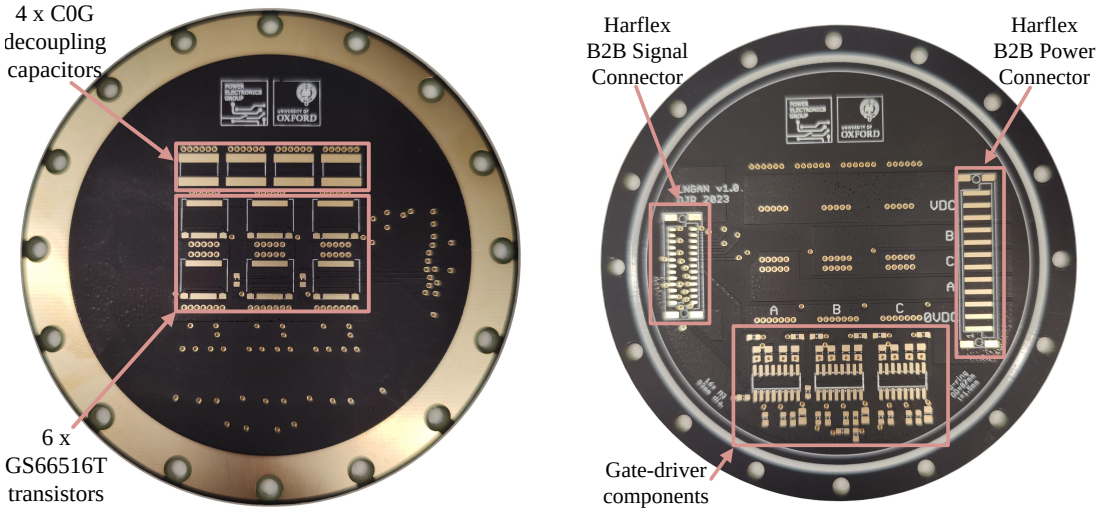
(a) (b)

Figure 5.7: Drawings and photo of the original inverter PCB stack-up. The unreliable board-to-board connectors can be seen. (a) Drawing showing a section view, (b) photo of the original inverter PCBs and board-to-board connectors.

5.3.5 Gate driver failure and resolution

In the final design of the inverter, which has been described in this chapter so far, a separate gate driver board was used to ensure the gate drive ICs operated within

their rated temperature range. Whereas in the first inverter design, the gate driver IC was soldered directly to the back side of the power board, as shown in Fig. 5.8. This design minimises the inductance of the gate drive loop, which is desirable to reduce the ringing in V_{gs}, which could cause overvoltage of the gate, damaging the transistor.



(a) (b)

Figure 5.8: Images of the first version of the inverter power board. (a) Shows the pads for the decoupling capacitors and HEMTs, (b) shows the pads for the back mounted gate drivers.

5.3.5.1 Gate driver anomalous behaviour

The first inverter design used the Skyworks Solutions SI8274GB4D-IS1R gate driver IC, selected after it had been tested at cryogenic temperatures. It is asserted in [82] that the SI8271 gate driver from the same family of gate drivers functions as expected at liquid nitrogen temperatures (77 K). Whereas [73] and [54] report that the same IC does not function properly below 130 K. Our initial testing of the chosen gate driver suggested a reasonable likelihood that the gate driver would function. No unexpected behaviour was observed at cryogenic temperatures, except for the differential propagation delay between the two channels increasing by 5 ns. Even once fully submerged in liquid nitrogen, the gate driver operated, driving a capacitive load that emulated the gate capacitance of the transistor. The gate driver was thermally cycled multiple times without degradation in the observed output. The outputs of the two channels of the gate driver are plotted in Fig. 5.9.

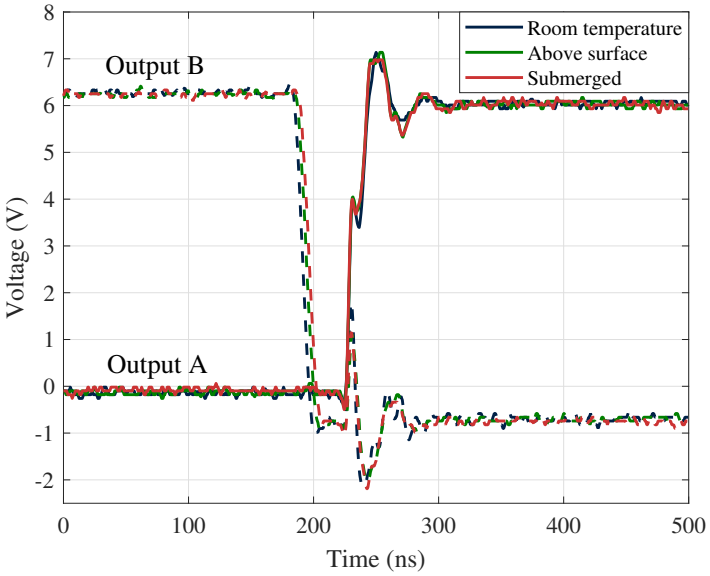


Figure 5.9: Oscilloscope captures measuring the outputs of the Skyworks Solutions SI8274GB4D-IS1R gate driver at cryogenic and room temperatures. The gate driver was tested with: the board at room temperature, the board suspended directly above the surface of the liquid nitrogen, and fully submerged in liquid nitrogen.

When commissioning the original inverter design, anomalous switching behaviour was observed in the midpoint voltage, following a hard-switched turn-on of the bottom transistor. An example of this can be seen in Fig. 5.10a. The midpoint voltage was seen to rise after a period approximately equal to the dead time, with behaviour similar to when the bottom transistor switched off. This is not consistent with a false turn-off induced by $L_\mathrm{s}\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ during a turn-on transition, as spurious behaviour occurs well after the peak $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$. The bus voltage at which the anomalous switching would first occur was inconsistent and it was not possible to determine the cause of the change in the onset voltage.

The best hypothesis for this behaviour is that the SI8274 gate driver was not functioning as designed due to the cryogenic temperature. Inconsistency between gate drivers of the same part number is noted in [82]. It was confirmed that the change in the midpoint voltage was driven by the gate driver by increasing the dead time from 40 ns to 200 ns. The duration of the anomalous gate voltage occurred for increased to the new duration of the dead time. This clearly indicates the fault is internal to the gate driver, possibly due to the dead time and deglitching logic circuits being out of their rated temperature range. This is shown in Fig. 5.10a.

The SI8274 has a single PWM input for the dual HS/LS outputs, with logic

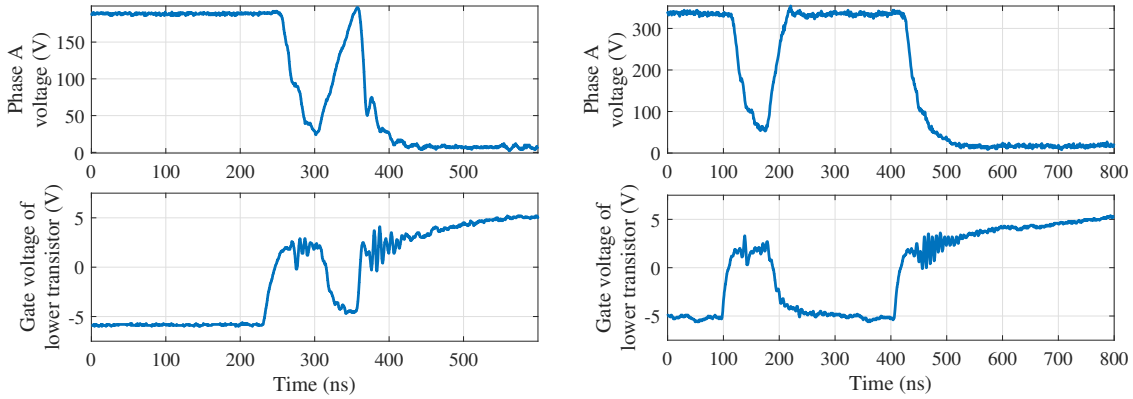


Figure 5.10: Scope captures showing the effect the deadtime had on the anomalous switching behaviour. Increasing the deadtime from (a) 40 ns to (b) 200 ns increased the duration for which the anomalous state was held. This clearly indicates the mistriggering of the gate driver.

circuits to implement the dead time and a deglitching feature. It is unreasonable to expect these to function 150 K below the gate drivers minimum rated temperature.

This result demonstrates that black box testing alone is insufficient to qualify components to cryogenic temperatures. Modern gate drivers incorporate various protection circuits, and without understanding how these features are implemented, it is impossible to understand the effect the cryogenic temperatures will have on a complex IC such as an isolated gate driver.

Another possible, but unlikely, explanation for the behaviour was that noise from the switching transient coupled to the inputs of the gate driver, mistriggering the inputs. A 1 MHz RC filter was soldered directly to the input pins of the gate drivers, to suppress the high-frequency noise that had been observed. This had no discernible effect on the anomalous switching.

5.3.5.2 Redesigned gate driver with thermal break

To achieve reliable switching with the gate driver IC selected, the temperature of the IC's must be significantly above the temperature of liquid nitrogen (reliable operation has been reported at temperatures above 130 K [54], [73], [82]). This requires the gate driver to be thermally separated from the cryogenic temperatures, but it is simultaneously required to be in close electrical proximity to the transistors to minimise gate loop inductance (and therefore cannot be as remote as the supply board). A thermal break designed into the gate driver PCB was used to achieve this.

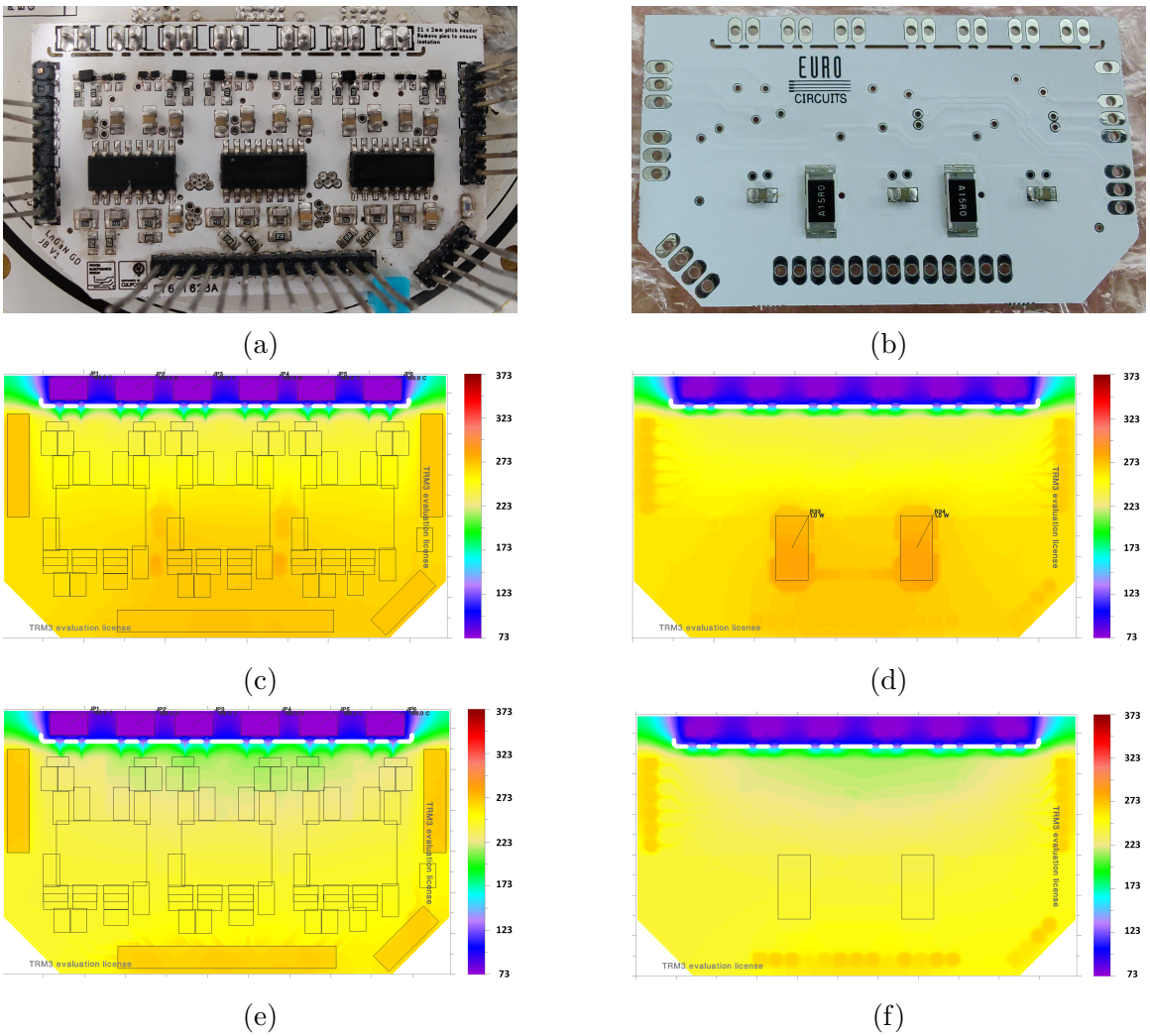


Figure 5.11: Images of the gate driver PCB. (top row): (a) shows the gate driver board assembled on the back side of the power board, (b) shows the heating resistors on the underside of the gate driver board. The second and third row of sub-figures show simulation outputs from Thermal Risk Management [123]. (middle row) for 2 W of heater power: (c) top layer, (d) bottom layer; (bottom row) with no heater power applied: (c) top layer, (d) bottom layer. Note: colourbar units are in kelvin.

The purpose of the thermal break is to create a high thermal resistance between two regions of the gate driver PCB. On one side of the thermal break, the connections between the gate driver board and the power board are made. On the other side of the thermal break (the warm side), the gate driver components are populated. Resistive heaters can then be used to heat the warm side of the thermal break, creating a large temperature differential between the two regions.

Heat is transferred from the liquid nitrogen to the gate drivers primarily through conduction of the header pins and PCB materials. The thermal break minimises conduction via the FR4 by milling slots into the gate driver board to reducing the cross-sectional area heat can conduct through. Electrical connections must still bridge the thermal break, requiring copper traces, which are very thermally conductive. The trace width was kept to the minimum fabrication width, to reduce conduction across the break. The heating resistors are populated on the underside of the PCB, with two large pours on the second layer under the gate drive ICs, spreading the heat to the components on the warm side of the thermal break.

The Thermal Risk Management 3 software package [123] was used to estimate the heating power required to ensure an adequately high temperature on the warm side of the thermal break. The model assumes that the pads for the gate driver to power board header pins, are at the temperature of liquid nitrogen (77.15 K). The connections between the supply board and the gate driver board are modelled as a thermal resistances equal to the conduction resistance of the 13 mm header pins.

No convective heat transfer is assumed to occur on the supply board facing side of the gate driver board, as the polystyrene insert packs the space, preventing air circulation. A $6\,\mathrm{W\,m^{-2}\,K^{-1}}$ heat transfer coefficient is applied to the power board side of the gate driver board with the air temperature set to the liquid nitrogen temperature. Radiative heating is modelled with the emissivity of the boards assumed to be 0.9, which is conservatively high.

2 W of resistive heating was found to be sufficient to keep the components on the warm side of the thermal break above 250 K. The simulation indicated that the header pins between the supply board and the gate driver board are significant sources of heat to the gate driver board, which in turn means only a small amount of resistive heating is required to keep the gate drivers above their 230 K minimum rated temperature. A PT1000 is populated on the gate driver board to measure its temperature, and a simple bang-bang controller is implemented so that excess heat is not supplied when the inverter is not being cryogenically cooled. The simulation results from TRM are plotted in Fig. 5.11. During the experiments, the PT1000 was consistently measured

to be between 250 K to 260 K with 2 W of resistive heating. Without resistive heating, the temperature of the PT1000 was measured to be between 235 K to 239 K. These measurements are consistent with the thermal simulation.

In order determine the fault with the cryogenically cooled gate driver it was necessary to vary the deadtime, as previously described this was challenging as this necessitated a hardware modification. Each time any component required changing, such as dead time setting resistors or gate resistors, the entire inverter must be thermally cycled, which took several hours and risked damage to components.

On the redesigned gate driver board the IC selected (Skyworks SI8273GBD-IS1) had separate inputs for the upper and lower gate signals. Using seperate input signals for each channel allowed the deadtime to be adjusted without modifying hardware or requiring thermal cycling. The gate driver circuit for the final inverter design, implemented on the heated gate driver board, is shown in Fig. 5.12. Zener diodes are used to protect the gate of the transistor from overvoltage during switching transients.

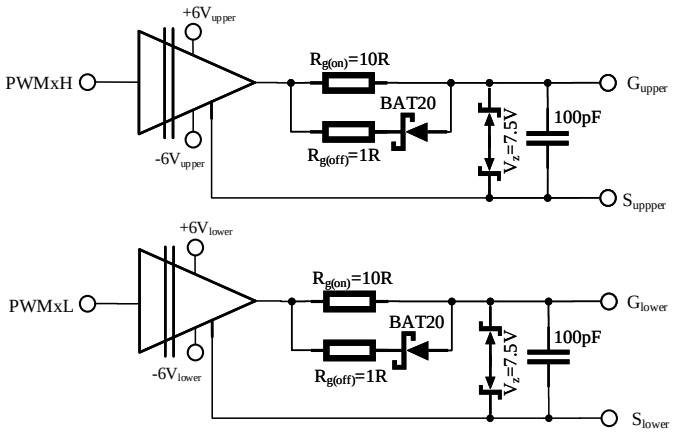
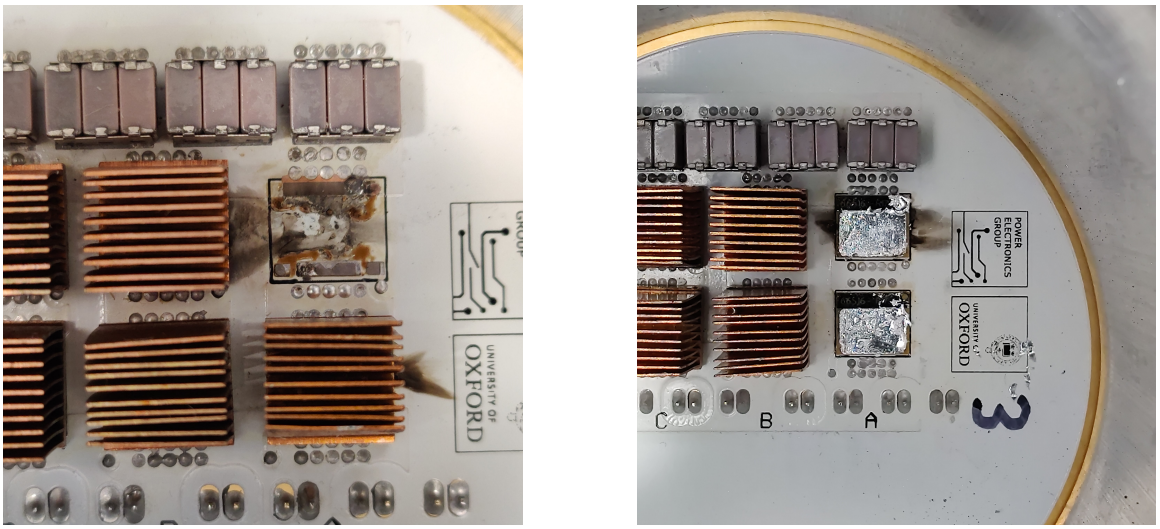


Figure 5.12: Schematic of the gate driver circuit for one of the three phases.

5.4 Inverter Limitation

During the cryogenic testing of the inverter the apparent power was increased incrementally by decreasing the electrical frequency (reducing the impedance of the RL load). This was repeated until the inverter failed at an electrical frequency of 1334 Hz. A second inverter failed at 1485 Hz. This corresponds to approximately 10 kVA apparent power. In both instances, the phase A upper transistor had failed catastrophically, as can be seen in Fig. 5.13.



(a) (b)

Figure 5.13: Photos showing the failed transistors on the power board and damage caused to the PCB. (a) the first inverter to fail, the upper transistor on phase A had detached itself from the PCB. (b) The upper transistor of phase A had again failed, the heat sinks of phase A have been removed in this photo to examine the damage.

The two inverter failures are likely to have been caused by excessive voltage stress on the transistor during switching transients. Less than 50 W of losses were generated prior to failure, which is insufficient to cause thermal instability as described in Chapter 3.1. The heat flux at failure ($0.3\,\mathrm{W\,m^{-2}}$) is also far less than the critical heat flux of liquid nitrogen ($20\,\mathrm{W\,m^{-2}}$) making this unlikely to be the cause of failure.

In the recorded oscilloscope captures, oscillations in the midpoint voltages are observed. The amplitude of the oscillations increases as the switched current increases; this is shown in Fig. 5.14. A final amplitude of approximately 100 V is apparent when the upper transistor switches on commutating the current that is flowing into the bridge.

A common method to slow switching transitions (thereby reducing the excitation of the parasitic elements in the switching circuit) is to increase the turn-on gate resistance until acceptable switching behaviour is achieved. This comes at the cost of increasing the switching losses. The gate resistance was increased from 10 Ω to 30 Ω on this basis. This resulted in significantly worse switching behaviour as seen in Fig. 5.15 with large oscillation at only 180 V. The value of the turn-off resistance did not have an effect on this behaviour.

This is consistent with the oscillations being due to the increased $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ at cryogenic temperatures, exciting the parasitic source inductance, L_s. During a turn-on

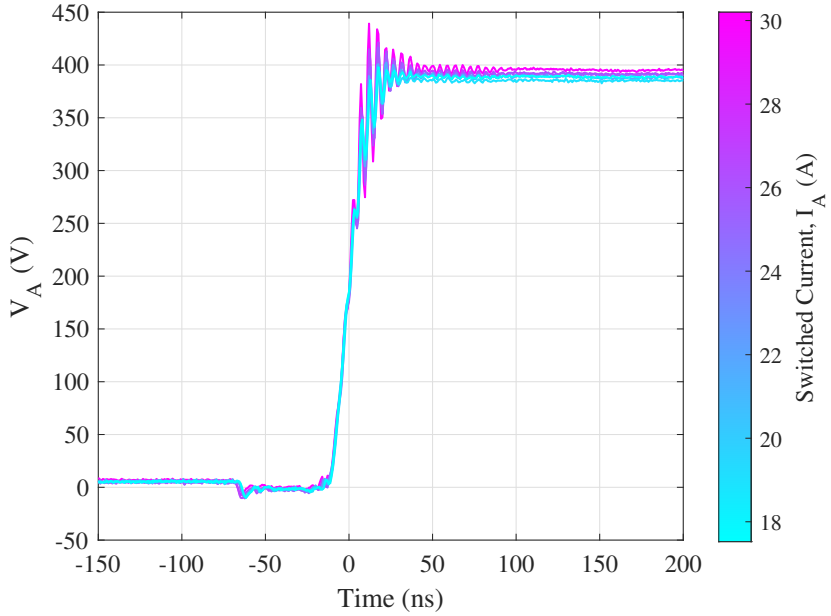


Figure 5.14: Plot taken at cryogenic temperatures showing the that midpoint voltage ringing grows with increasing phase current.

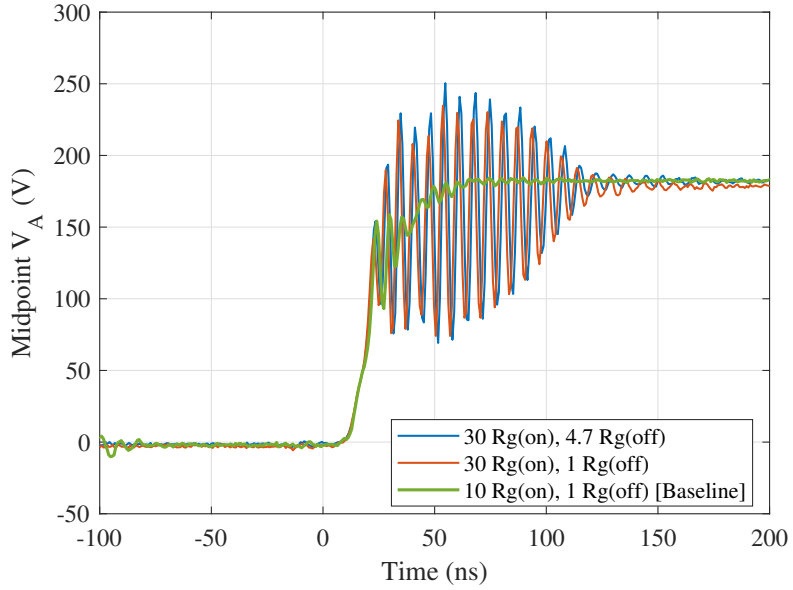
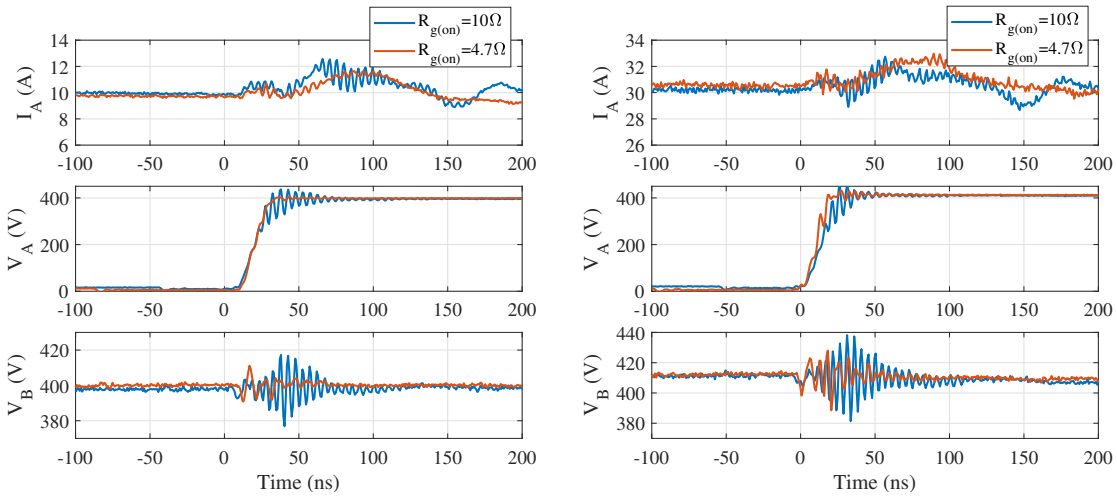


Figure 5.15: Comparison of switching behaviour for $R_{g(on)} = 30\,\Omega$, with two values for $R_{g(off)}$, compared to $R_{g(on)} = 10\,\Omega$. The value of $R_{g(off)}$ has negligible impact on the oscillatory behaviour.

event, once the gate-source voltage has exceeded the threshold voltage, the transistor starts to conduct, causing a voltage spike across the parasitic source inductance. The voltage across the parasitic inductance decreases the effective gate-source voltage, which switches the transistor back off. This can cause oscillatory behaviour as observed. This is caused by the transistor that should be switching on, fluctuating between conducting and blocking current. Increasing the gate resistance means that the gate is charged more slowly, making the voltage of the gate source more susceptible to being driven below the threshold voltage by $L_\mathrm{s}\mathrm{d}i_\mathrm{d}/\mathrm{d}t$.

As shown in Section 3.2, at cryogenic temperatures, the $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ doubles, which in turn doubles the excitation voltage on the parasitic inductance of the package. This can lead to the gate voltage falling below or approaching the threshold voltage during a turn-on transition. The same effect was initially suspected but was ruled out as the cause of the behaviour observed in Chapter 3, Section 3.2.3.2. It was also observed to cause unstable oscillations in [54].

Driving the gate more strongly to the on-state voltage by decreasing the gate resistance was tested as a potential solution to the poor switching behaviour. 4.7 Ω gate resistors were installed and tested. Decreasing the gate resistance was seen to reduce the amplitude of the oscillations, as shown in Fig. 5.16.



(a) $I_\mathrm{A} = 10\,\mathrm{A}$ (b) $I_\mathrm{A} = 30\,\mathrm{A}$

Figure 5.16: Plots of data recorded at cryogenic temperatures showing the reduction in midpoint voltage ringing achieved by reducing the turn-on gate resistance from 10 Ω to 4.7 Ω.

The inverter was tested at the apparent power set-point where the previous failure had occurred. The inverter was tested at all three switching frequencies, demonstrating an improvement in the power rating with the 4.7 Ω gate resistors.

It should be noted that further decreasing the gate resistance may lead to a different failure mode caused by the faster switching speeds. During a hard-switched transition, parasitic turn-on of the opposing transistor can occur due to the miller capacitor if the $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ becomes sufficiently high. This results in shoot-through, potentially damaging the transistors catastrophically. This was observed in Chapter 3 until a $-6\,\mathrm{V}$ off-state gate voltage was applied.

5.5 Calorimetric Loss Measurement Method

The model of the cryogenic inverter described in Chapter 4 suggests that when operating at 30 kVA apparent power (calculated using a 400 V bus voltage and using the 60 A datasheet current rating of the transistors) the computed losses are expected to be 95 W. This small loss constitutes only 0.3% of the total apparent power of the inverter. If the efficiency is calculated from full-scale electrical measurements of the input and output power, it will have significant error.

The result of error in the electrical measurement can be seen in [95] where a power analyser is compared to a custom solution and simulation. There is a 4% error between the two techniques for measuring the efficiency from electrical measurements. In [124] they show that a 99% efficient inverter can be measured to ±0.35% with their calorimetric measurements technique compared with ±2.25% with a high end power meter. [125] and [101] both examine soft and hard switching losses of GaN HEMTs, respectively, using both electrical and calorimetric methods.

As presented in [124], for the electrical measurement method, the input and output power of the inverter are measured and the losses calculated $P_{\mathrm{loss}} = P_{\mathrm{in}} - P_{\mathrm{out}}$. The efficiency calculated using electrical measurements, η_{e}, considering the simple average error in P_{in} and P_{out} due to measurement error can be expressed as:

$$\eta_{\mathrm{e}} + \Delta\eta_{\mathrm{e}} = \frac{P_{\mathrm{out}} \pm \Delta P_{\mathrm{out}}}{P_{\mathrm{in}} \pm \Delta P_{\mathrm{in}}} \tag{5.2}$$

Which can be rearranged and simplified to:

$$\frac{\Delta\eta_{\mathrm{e}}}{\eta} = \frac{\Delta P_{\mathrm{out}}}{P_{\mathrm{out}}} + \frac{\Delta P_{\mathrm{in}}}{P_{\mathrm{in}}} \tag{5.3}$$

In [124] measurement accuracies of 2% and 3% are considered typical for P_{in} and P_{out}, P_{out} being harder to measure accurately due to the high frequency content. This results in an efficiency measurement accuracy of $\frac{\Delta\eta_{\mathrm{e}}}{\eta_{\mathrm{e}}} = \pm 5\%$

Calorimetric methods for measuring efficiency measure the system losses by inferring them from changes in enthalpy that result. The efficiency from calorimetric measurements is calculated as:

$$\eta_c + \Delta\eta_c = \frac{P_{out} \pm \Delta P_{out}}{P_{out} \pm \Delta P_{out} + Q \pm \Delta Q} \tag{5.4}$$

Which is simplified to:

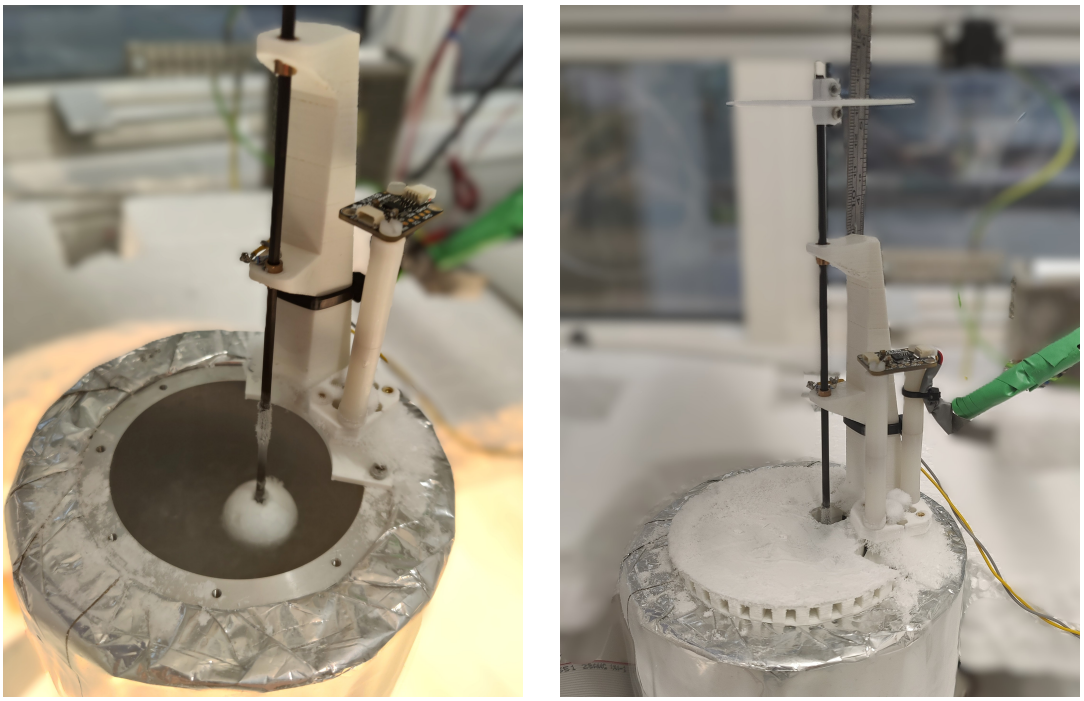
$$\frac{\Delta\eta_c}{\eta_c} = (1 - \eta_c)\left[\frac{\Delta P_{out}}{P_{out}} + \frac{\Delta Q}{Q}\right] \tag{5.5}$$

Where Q is the losses dissipated as heat and $\Delta\eta_c$ is the average error associated with the calorimetrically measured efficiency. It can be seen that as the efficiency of the inverter increases, the average error in the efficiency also decreases, independently of improvements in the measurement accuracy. Assuming the measurement accuracy of P_{out} remains 3% and the losses can also be measured to 3% accuracy, for a 99% efficient inverter, the calculated result would be $\frac{\Delta\eta_c}{\eta_c} = \pm 0.06\%$, meaning the efficiency would be expressed as $\eta_c = 99\% \pm 0.0594\%$ (a hundred times more accurate than by using electrical measurements).

5.5.1 Boiling Rate Measurement

To measure the losses of the cryogenic inverter, the boiling rate of the liquid nitrogen is measured, which is directly correlated to the losses. The boiling rate can be quantified by measuring the change in mass of the liquid nitrogen, by measuring the volumetric flow rate of the evaporated nitrogen gas, or by measuring the change in of the liquid nitrogen surface height.

Measurements of the mass of liquid nitrogen were deemed to be too sensitive to perturbations in this application. For instance the mechanical loads the DC supply and phase cables would exert on the inverter would not be constant as the cable insulation temperature and flexibility would change in response to conducted currents. Measuring the volumetric flow rate of nitrogen gas was considered but discounted in favour of measuring the surface level of the liquid nitrogen. To achieve this a VL6180X optical time-of-flight sensor is used. The sensor cannot measure the height of the liquid nitrogen directly, so a float is attached to a vertical guide rod with a lightweight plastic disc mounted to the top of the rod. The ToF sensor position tracks the position of the disc. This is shown in Fig. 5.17. The level and boiling rate of the liquid nitrogen in the vessel can therefore be measured without directly exposing the



(a) (b)

Figure 5.17: Images of the float, guide rod, and ToF sensor arrangement used to measure the boiling rate.

sensor to cryogenic temperatures. Heated brass bushings are used in the assembly to prevent ice from seizing the vertical motion of the guide rod.

Alternative methods to measure the boiling rate that were considered and discounted include:

- Ultrasonic distance sensor to directly measure the liquid level - this works well with room-temperature fluids such as water. The speed of sound used by the sensor to determine distance is dependent on the temperature of the air, and this is clearly not constant or known above the surface of liquid nitrogen. Ultrasonic sensors were therefore deemed to be inappropriate for this application.

- Capacitive liquid level sensor - this type of sensor works on the principle that the relative permittivity of the fluid and gas are sufficiently different to detect the fluid level. The relative permittivity of nitrogen was found to be too close to that of air for this method to work. The ratio of the relative permittivities of air and water is 80, while it is only 1.4 for air and liquid nitrogen.

- Limit switches actuated by floats - for a reasonable size of float, there was insufficient force from the buoyancy of the float to actuate a limit switch.

- Linear variable differential transducer - this type of sensor is a transformer with a sliding core, the coupling between the transformer windings is dependent on the position of the core allowing displacement to be measured. No suitable LVDT, with low enough actuation force and measurement range, could be found. The mechanical and electrical reliability of the sensor in close proximity to the liquid nitrogen was also a concern.

This method could be extended to measure the small amount of losses incurred in the bus capacitor, which was not submerged or in close thermal contact with the liquid nitrogen in this design. Given that the characteristics of polypropylene film capacitors are not degraded by cryogenic temperatures [40], this would be a worthwhile addition in future work.

5.5.2 Calibration

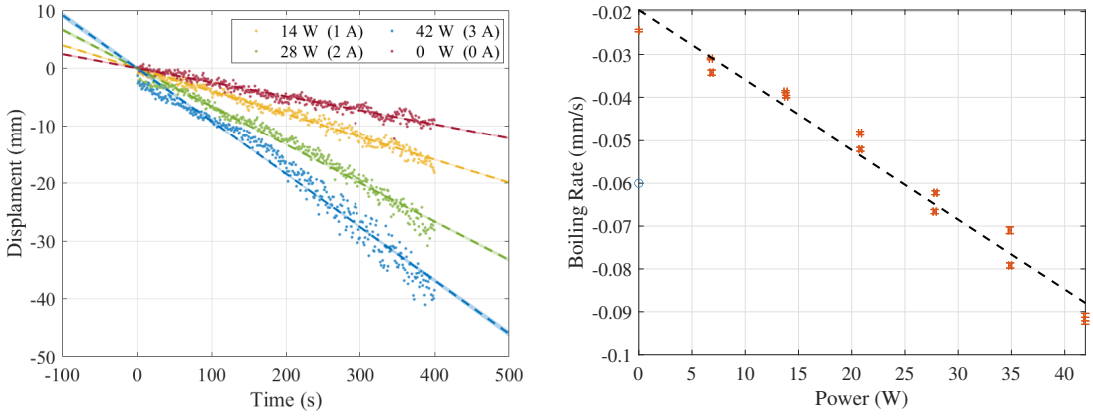
To use the measured boiling rate to predict the inverter losses, the boiling rate must first be calibrated to a known loss. There is an unknown heat leak into the vessel via the vessel walls and base, causing a non-zero boiling rate when no heat is generated by the inverter. The calibration method uses a fixed negative current supplied to the inverter. This reverse-biases the two GaN HEMTs in each bridge with a voltage across them equal to the sum of the off-state gate voltage and the threshold voltage of both transistors ($\sim 14\,\mathrm{V}$). A small DC current can in this way be used to generate significant loss in a representative manner to when the transistors are switching. The liquid level is then measured for 400 s, and the boiling rate determined from the slope of a linear regression to the level displacement measurements. The calibration is conducted with any auxiliary circuits, including the radiative and gate driver heaters switched on to replicate the conditions when the inverter is switching.

The DC voltage and current at the input can be accurately measured using a Pico ADC20 data logger, measuring the bus voltage via a potential divider and the supply current using a Reidon RSA-50 current shunt.

Fig. 5.18a shows the change in displacement of the float over four calibration tests as measured by the ToF sensor. The lines of best fit are overlaid on the datasets, with the standard error of each regression shaded around them. The gradient of these lines are the boiling rates plotted on Fig. 5.18b against the mean measured power over each calibration run. The average measurement errors are shown for both the boiling rate and the power. A single data point was identified as anomalous; this was the

first data point collected and is likely due to the assembly not reaching a steady-state temperature before the test was started.

The heat leak from the surrounding environment results in a non-zero intercept when plotting the boiling rate against the losses. The measured $-0.02\,\mathrm{mm\,s^{-1}}$ intercept implies a heat leak of 6.3 W.



(a) (b)

Figure 5.18: Plots showing the relationship between boiling rate and heat dissipated measured during the calibration step. (a) displacement of the float for a four example calibration tests. Lines of best fit are overlaid. (b) is a plot of the boiling rate against the mean power for all the calibration tests. The measurement error is plotted on (b) as error bars.

5.5.3 Calorimetry

The inverter was tested with the apparent power ranging from 5.2 kVA to 11 kVA. The cause of the upper power limit has been explained in Section 5.4. An RL load was used, making it possible to set the apparent power by adjusting the electrical frequency from 2.7 kHz to 1.3 kHz. This was decreased in increments that would increase the apparent power by approximately 1 kVA. Each apparent power set-point was repeated using switching frequencies of 20, 50, and 80 kHz. For the highest electrical frequencies, a 20 kHz switching frequency was not high enough to generate balanced phase currents. Set-points where $f_\mathrm{e} < \frac{f_\mathrm{sw}}{10}$ were therefore skipped. The level of the liquid nitrogen was measured with the ToF sensor. Each set-point was run for 400 s to give a good estimate of the boiling rate.

5.5.3.1 Loss measurements

The measured boiling rates are shown in Fig. 5.20. The ToF sensor displacement measurements are offset by the initial position of the float. Effort was made to keep this consistent by marking a fill line on the inside of the vessel to which the liquid nitrogen was filled prior to each set-point being run.

Using the boiling rates and heat dissipations measured in the calibration step, a reverse regression is performed, allowing the losses of the inverter, Q, at each set-point to be inferred from the new boiling rate measurement.

5.5.3.2 Power measurements

The power of the inverter was calculated from the measured phase current and the calculated line-to-line voltage. Due to the limited number of channels on the Tektronix MSO54 oscilloscope, only one phase current was measured with an Agilent N2781A current clamp. It was therefore necessary to fit the data to a sine wave to determine its frequency before taking the RMS of a single period. The line to line voltage is calculated from the bus voltage, using the theoretical line-to-line voltage for third-harmonic injection PWM, with a modulation index of $\frac{\sqrt{3}}{2}$. For all set-points a 397.4 V bus voltage was used in the calculation, which was measured at the supply board.

$$V_{\mathrm{ll}} = \frac{V_{\mathrm{bus}}}{\sqrt{2}} \tag{5.6}$$

$$S = \sqrt{3} V_{\mathrm{ll}} I_{\mathrm{ph,RMS}} \tag{5.7}$$

5.6 Loss Measurement Results

The measured displacement of the float for each set-point is plotted in Fig. 5.20, with the lines of best fit overlaid. The initial offset measured by ToF sensor at the start of each set-point is found from the intercept of the line of best fit and subtracted for this plot.

The inferred losses are plotted against the apparent power measured in Fig. 5.21. The set-points measured using 10 Ω of turn-on gate resistance are plotted with circles, while points that were later measured with 4.7 Ω turn-on gate resistors are plotted with crosses (the use of the 4.7 Ω gate resistors has been explained in Section 5.4).

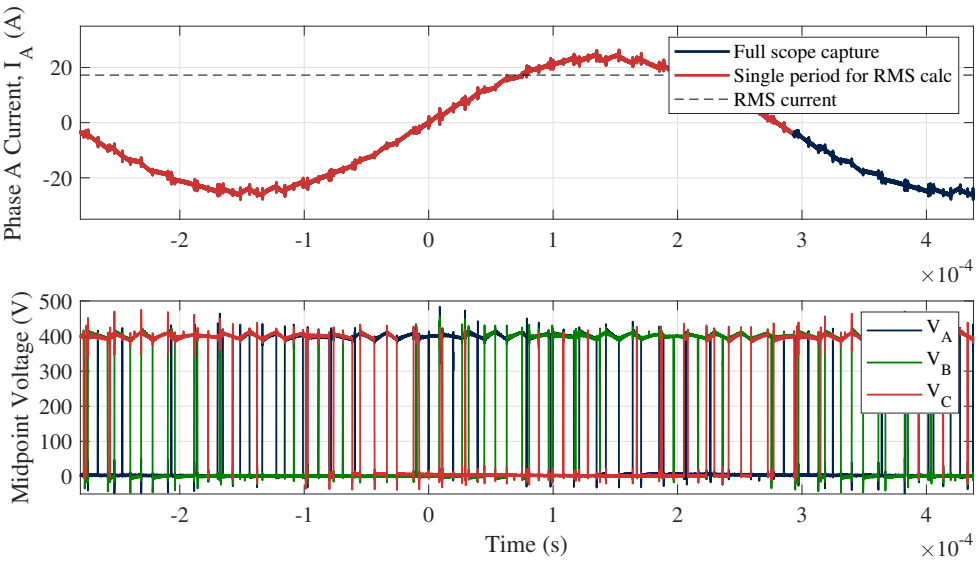


Figure 5.19: Plots showing the electrical oscilloscope measurements for the $S = 8.4\,\text{kVA}$, $f_{\text{sw}} = 50\,\text{kHz}$ set-point. The upper plot shows the phase A current, with the single period used to calculate the RMS current indicated. The calculated RMS current is also marked. The lower plot shows the midpoint voltages of the three phases.

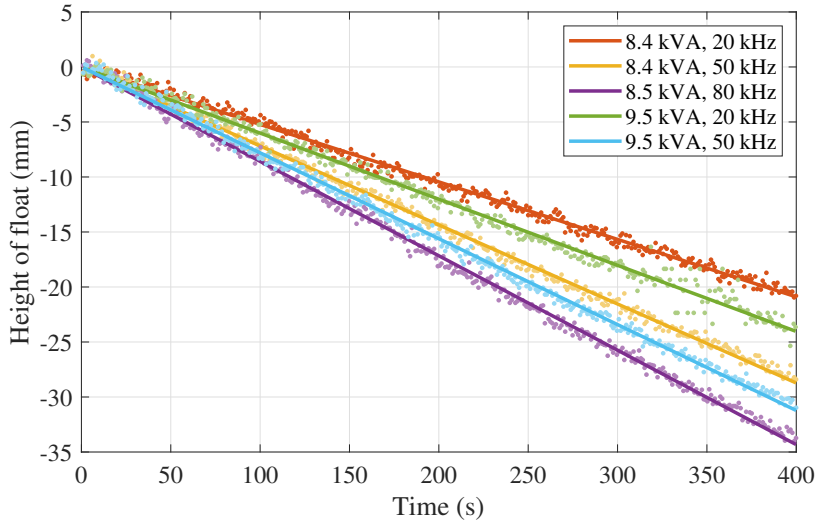


Figure 5.20: Height of the float as measured by the ToF sensor with the inverter operating for five of the set-points.

The smaller 4.7 Ω gate resistors lead to faster switching speeds and consequently lower switching losses, this explains the lower measured losses for these set points.

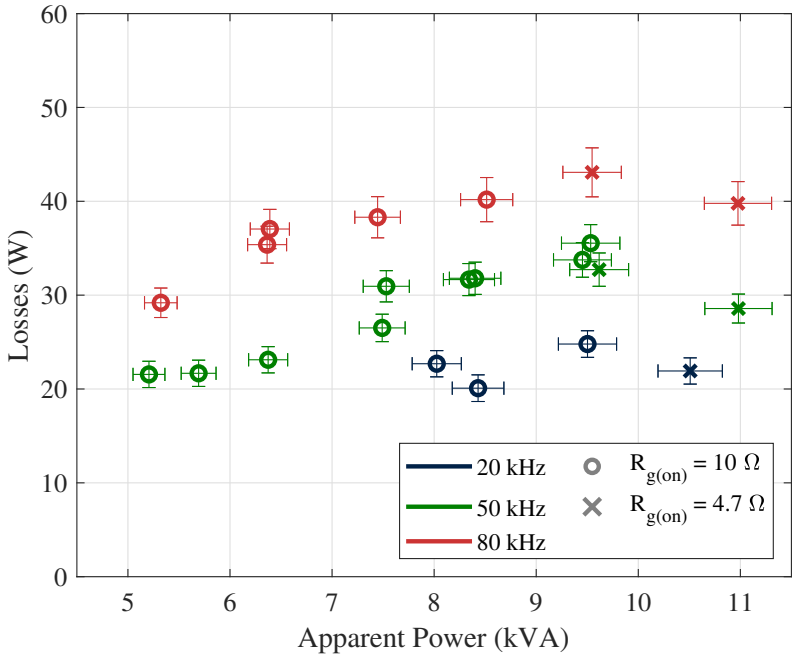


Figure 5.21: The estimated losses inferred from the boiling rate for each set-point. Circles denote measurement made with 10 Ω turn-on gate resistors and crosses 4.7 Ω. Error bars denote the standard errors. The lower losses at the highest power is due to the smaller gate resistors used for these datapoints.

The effect of losses due to the switching frequency is clearly visible, with greater losses occurring at higher switching frequencies as would be expected. There is also a discernible correlation between the losses and the apparent power.

The efficiency of the inverter was calculated as per Eq. 5.8 and plotted against apparent power in Fig. 5.22.

$$\eta = \frac{S}{S+Q} \tag{5.8}$$

The standard error associated with the power, loss, and efficiency measurements are displayed as error bars. More detail on the method used to calculate the errors are given in Appendix A.

A peak efficiency of 99.8 % was measured for the 10.5 kVA, 20 kHz switching frequency set-point with the 4.7 Ω turn-on gate resistors fitted. A slight increase in efficiency with lower gate resistors can be expected as the switching time, and therefore losses, are reduced.

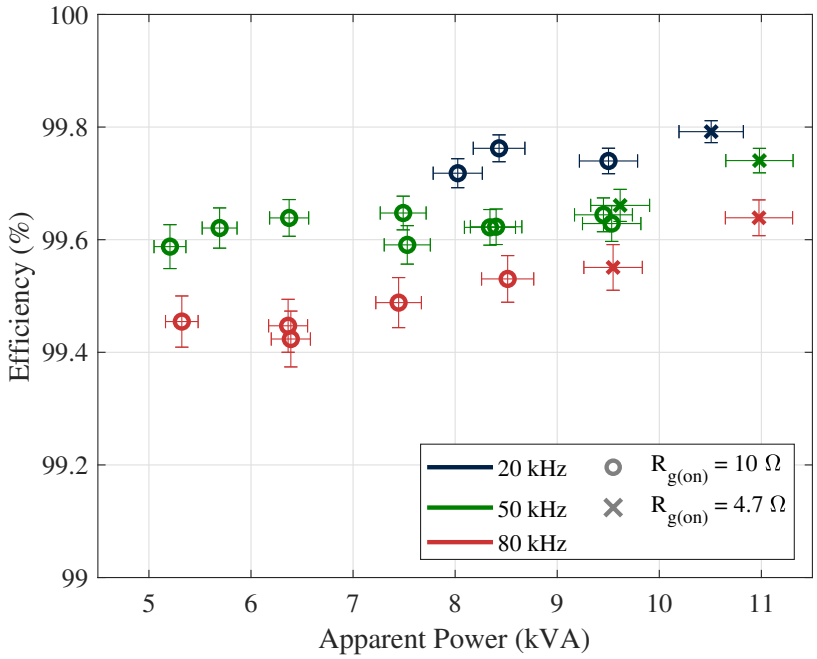


Figure 5.22: Calculated efficiency from the inferred losses and measured power for each set-point. Circles denote measurement made with 10 Ω turn-on gate resistors and crosses 4.7 Ω. Error bars denote the standard errors.

5.6.1 Comparison to Inverter Model

In Chapter 4 a loss model for a cryogenic inverter is presented and explained. This model was used to simulate the prototype inverter; a comparison of the simulation with the experimental results is plotted in Fig. 5.23.

There is a RMSE of 3.94 W between the simulation and experimental results. This close agreement was achieved in part because the junction temperature would not be expected to increase significantly; with 10 kVA and 50 kHz switching frequency, the junction temperature would be expected to increase by only 5 K. This region of the $R_{\mathrm{ds(on)}} - T_{\mathrm{j}}$ curve is very shallow. This negates any error in the thermal resistance modelled as the temperature effects are less prominent than if the junction temperature was elevated over approximately 320 K. If the inverter were tested at higher power, with higher losses, more significant errors in the predicted losses would be seen as the result of the deviation between the estimated R_{th} and its true value.

Larger deviations from the modelled losses were observed for set-points using a 20 kHz switching frequency. To synthesise sinusoidal waveforms using PWM the ratio of switching to electrical frequency must be sufficiently high to prevent distortion and unbalanced phase currents. At 20 kHz distorted phase outputs were observed to

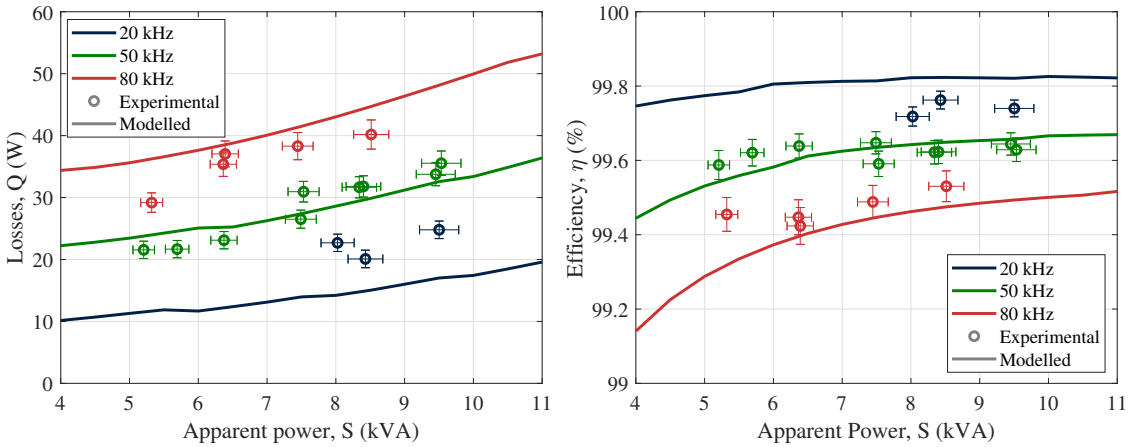


Figure 5.23: Comparison of the experimentally measured losses and efficiency to the cryogenic inverter model described in Chapter 4.

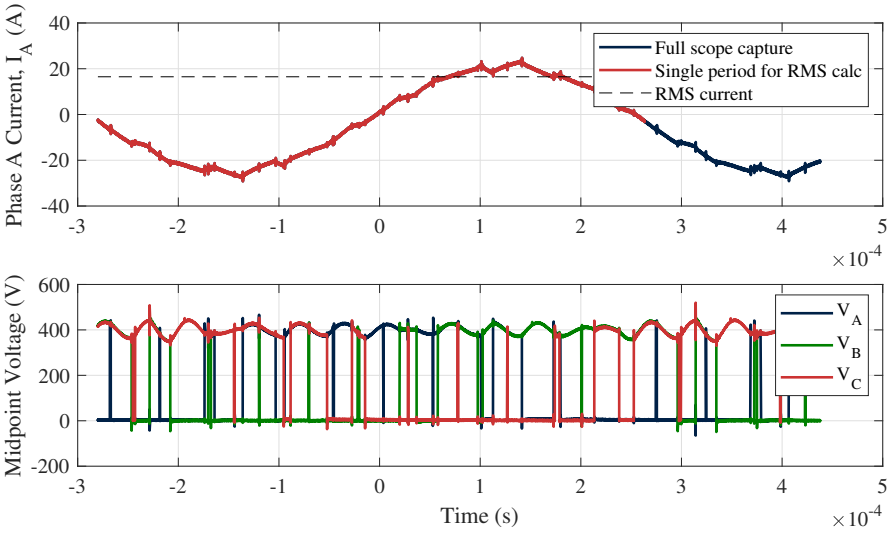


Figure 5.24: Waveform with 20 kHz switching frequency. Large oscillations in the DC bus voltage suggest resonance is occurring leading to greater losses.

occur at the highest electrical frequencies, requiring these set-points being omitted. The cause of the increased deviation from modelled losses may be as a result of the switching frequency only being marginally sufficient, especially considering that the frequency component introduced by the third harmonic injection method used is three times higher than the electrical frequency. An alternative potential source of the additional loss may be suggested by the oscillations in the DC bus voltage that can be observed in the waveforms for the 20 kHz switching frequency shown in Fig. 5.24. These indicate that resonance is occurring between the DC bus capacitor and the wiring inductance of the inverter, due to the switching frequency being close to the resonant frequency.

5.7 Conclusion

The inverter was tested up to 11 kVA where it exhibited an efficiency of 99.74%.An exceptionally high peak efficiency was measured, 99.76%. 11 kVA is the highest reported power for a cryogenic GaN converter and the only cryogenic GaN inverter to be tested at a power greater than 1 kVA. Despite this result being the state of the art for cryogenic GaN inverters, this is insufficient power for a aircraft motor drive. Further research is required to overcome the limitations of the cryogenic inverter tested in this work. Due to the properties of the GaN HEMT at cryogenic temperatures it was not been possible to demonstrate that a cryogenic GaN inverter suitable for a motor drive application is achievable with current technology, as posed in research question 2c.

A calorimetric method for measuring the losses of a cryogenically cooled inverter was developed, and the method was found to be sufficiently accurate to quantify the losses in the prototype inverter to a reasonable degree of accuracy. Answering research question 1c.

Close agreement was achieved between the simulated results from Chapter 4 and the experimental results. The inverter was successfully tested at approximately the predicted point of maximum efficiency. Since the model is used to address research question 1b, this correlation provides confidence in the conclusions drawn. For instance, by varying the switching frequency when operating the cryogenic inverter, an assessment of the fraction of overall losses that could be contributed to the switching losses could be made. By comparing this to the modelled losses it is possible to validate that the switching losses do not excessively deviate from those expected.

A potential cause of inverter failure was identified and a remedial modification was tested and shown to improve switching performance. Additionally a number of potential failure modes for the cryogenic inverter were identified and methods to resolved them detailed in Section 5.3. The observed failure mechanisms are not seen at room temperature and therefore gives a number of insights into research question 2b.

To resolve the root cause of the ultimate inverter failure mode in future designs, the following design modifications are suggested:

1. Select a transistor that has a kelvin source connection.

2. If possible select a transistor with lower source inductance (although the GaNPx package used has a very competitive estimated inductance of only 0.2 nH [126], [127]).

3. Reduce gate loop inductance to reduce the amplitude of the V_{gs} ringing and overshoot.

4. Implement an active gate driver to limit the $\mathrm{d}i_{\mathrm{d}}/\mathrm{d}t$ of the transistors.

It may be possible to use higher bus voltages at cryogenic temperature due to the 20 % to 40 % increase in the breakdown voltage of GaN HEMTs at cryogenic temperatures [51]. It is likely that this would lead to higher efficiency and maximum power. This should be investigated in future work.

Future development of a gate driver that is rated to cryogenic temperatures would allow closer integration of gate driver and transistors, this would reduce the gate loop inductance and potentially improving switching performance and reduce design complexity.

Chapter 6

Conclusions and Future Work

This work has been conducted with the aim of resolving the research question posed in Chapter 1: *Are cryogenically cooled GaN inverters suitable for aircraft applications?* This has been achieved by answering five sub-questions belonging to two distinct topics. The first topic focuses on what improvement there is in performance from the potential reduction in losses of a GaN inverter at cryogenic temperatures. The second topic assesses if a cryogenic GaN inverter suffers any limitations (such as additional failure modes) due to the extreme operating conditions.

Regarding the topic of losses and efficiency at cryogenic temperatures:

1a. *How are switching losses of a GaN HEMT affected by cryogenic temperatures?* A calorimetrically validated test-platform was used to measure the switching losses of a GaN HEMT. The results show that an initial decrease in switching losses occurs as the temperature is reduced, falling to a minimum at 198 K that is 24 % less than measured at room temperature. In contrast, previous measurements of the switching loss for this transistor in literature, have reported a monotonic decrease from room-temperature to the minimum temperature measured. The non-monotonic trend observed here has only been reported in one other work, but for a lower current rated transistor from the same manufacturer, but not for the larger transistor suited for high power motor drives. The use of a validated test-platform has therefore made it possible to robustly demonstrate that non-monotonic switching loss behaviour is repeatable, suggesting either measurement error in the opposing literature or differences in implementation that merit further research. At cryogenic temperatures switching losses form a larger if not dominant proportion of the overall inverter losses, due to the large reduction in conduction losses. Therefore contributions to the literature on the topic of cryogenic switching losses is of particular importance.

1b. *What improvements in efficiency and peak power can be achieved by cryogenically cooling a GaN inverter compared to a conventionally cooled GaN inverter for aircraft propulsion applications?*

A simulation of a cryogenic GaN inverter was conducted using a thermo-electric model of the GaN transistors and inverter. The simulation indicates that a 40% reduction in active area and a 2.2 percentage point increase in efficiency at take-off can be achieved if a cryogenically cooled motor drive was implemented for a light-aircraft propulsion system. During the cruise phase when the when the electrical load is 4.3 times smaller the efficiency improvement is more marginal, 0.2 percentage points.

Additionally, a simulation of a prototype inverter, indicated that the peak efficiency when cryogenically cooled, would be 99.82% at 10 kVA. The same inverter, when air-cooled, results in a peak efficiency of 99.65% at 4.5 kVA. The simulation indicates a seven-fold increase in (thermally limited) peak power when the inverter is cryogenically cooled (compared to conventional cooling).

The peak power of the prototype GaN inverter was shown in simulation to increase from 14.5 kVA when air-cooled to 100 kVA with liquid nitrogen cooling, assuming the design is thermally limited.

The prototype inverter was built and shown to operate at the expected peak efficiency at cryogenic temperatures. The peak power was limited though by electrical limitations.

The model of cryogenic GaN inverters is a significant improvement on the methods used to simulate a cryogenic inverter in existing literature and will benefit aircraft level studies such as that in [3] where constant values of inverter efficiency were assumed.

1c. *Losses in a cryogenic GaN inverter are expected to be very small compared to the apparent power. How can the efficiency be accurately measured for a cryogenic inverter, in order to quantify the improvement in performance?*

It was determined a calorimetric method was required to achieve a suitable degree of accuracy in the loss measurements. This was implemented by measuring the boiling rate of the liquid nitrogen coolant. A mechanical float and optical time of flight sensor were used to achieve this. A number of sensors were considered to find a measurement solution compatible with the cryogenic temperatures and fluid properties of liquid nitrogen. The calorimetric method

was found to be sufficiently accurate to quantify the losses in the prototype inverter to a good degree of accuracy.

On the topic of limitations and cryogenic failure modes:

2a. *Does large heat generation in the transistor junction and resultantly large temperature gradients across the transistor package degrade the performance of a GaN HEMT at cryogenic temperatures, and what determines the maximum thermal dissipation of the transistor at cryogenic temperatures?*
Using a continuous high current test setup it was found that the GaN HEMT studied was limited by thermal instability. This occurred at an average temperature of 170 K, 250 K lower than the maximum rated junction temperature of the transistor. The thermal loads increased junction temperature which increased the on-state resistance and also increased the thermal resistance of the thermal path. The thermal conductivity of silicon (from which the die is mostly composed) increases by a factor of 9.4 at 77.15 K compared to room-temperature. This has a significant role in determining the point of thermal instability.

2b. *Do new mechanisms lead to failure for a GaN transistor at cryogenic temperature or are conventional failure modes exacerbated by the change in the properties of the GaN transistor at cryogenic temperatures?*
It was determined that thermal instability is the mechanism by which thermal failure occurs at cryogenic temperatures. This was important for the design and modelling of a cryogenic inverter described in this thesis. While it was unexpected that the point of instability occurred when the junction temperatures was 250 K lower than the maximum rated junction temperature, the cryogenic temperatures did not exacerbate this failure mode and in fact the reduced junction-to-casing thermal resistance and $R_{\mathrm{ds(on)}}$ caused the onset of this failure mode to occur at higher currents than would be expected at room temperature.

It was found that due to the reduced threshold voltage and increased $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ that the GaN HEMT was more susceptible to miller current induced shoot-through, this had been previously been reported in literature as a failure mechanism for this transistor at cryogenic temperatures. Here we found reducing the turn off gate voltage, it was possible to suppress the $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ induced shoot-through. It has not previously been demonstrated in literature that this minor modification to the switching circuit can resolve this known issue. This would

have otherwise been a barrier to the continued work on cryogenic GaN power electronics.

It was observed that at cryogenic temperatures, the $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ doubles, which in turn doubles the excitation voltage on the parasitic inductance of the package. This can lead to the gate voltage falling below or approaching the threshold voltage during a turn-on transition. It was also observed to cause unstable oscillations in [54]. It was found by driving the gate more strongly to the on-state voltage, by decreasing the turn-on gate resistance, it was possible to suppress the oscillatory behaviour. This insight is an important design consideration for future gate driver circuits intended for driving GaN transistors at cryogenic temperatures.

2c. *A cryogenically cooled GaN inverter has not yet been demonstrated in the literature at a power greater than* 1 kW*. Is a cryogenic GaN inverter suitable for a motor drive application achievable with current technology, and if so, what is its maximum achievable power and efficiency?*
A prototype inverter was designed and testing using COTS parts and custom PCBs, specifically designed for the application. The design thermally separated components using thermal-breaks to enable them to function. The inverter achieved a peak efficiency of 99.79 % and was tested up to 11 kVA where it exhibited an efficiency of 99.74%. This is the highest reported power for a cryogenic GaN converter and the only cryogenic GaN inverter to be tested at a power greater than 1 kVA.

The overall research question was: *Are cryogenically cooled GaN inverters suitable for aircraft applications?*

Cryogenic GaN inverters show promise as being suitable for aircraft applications, due to the highly efficient operation which was modelled and demonstrated in this thesis. Additionally, the modelled uprating of the inverter's peak power when cryogenically cooled is beneficial for delivering the required take-off power, helping to overcome the limitations caused by the low thermal inertia of semiconductor dies compared to a conventional combustion engine. Conversely it has been shown that further work will be required to overcome the constraints of inverter power identified in this thesis. These limitations currently prevent cryogenic GaN inverters reaching the required power suitable for aircraft propulsion applications. Developments are needed in GaN transistor technology to achieve the required low parasitic inductance for good switching behaviour at cryogenic temperatures. This may potentially require

transistors designed specifically for cryogenic applications, where the lower threshold voltage and higher $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ at cryogenic temperatures are accounted for in the design, potentially compromising the design at room temperature, such that it has useable properties at the desired cryogenic operating temperature. This will enable higher-power operation closer to the thermal limit of the transistors.

6.1 Future Work

While a significant improvement on the state of the art was made with the prototype cryogenic inverter, the parasitic source inductance of the HEMT appears to limit the maximum current it can switch. To increase the amplitude of the phase current, the following could be attempted:

1. Trial an alternative transistor that has a kelvin source connection.
2. If possible, select a transistor with lower source inductance (although the GaNPx package used has a very competitive estimated inductance of only 0.2 nH [126], [127]).
3. Reduce the inductance of the gate loop to decrease the amplitude of any V_gs ringing and overshoot. This could be achieved by using a gate-driver IC that is compatible with the cryogenic temperature.
4. Implement an active gate driver to limit the $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ of the transistors. However, slowing down the $\mathrm{d}i_\mathrm{d}/\mathrm{d}t$ will increase switching losses and reduce efficiency.
5. Work with transistor manufacturers to develop a GaN transistor that is optimised for cryogenic applications, e.g. by tuning the threshold voltage and/or transconductance to suppress parasitic turn-off.

Additional topics of interest were identified in the course of this work, but time did not permit them to be explored; these include:

1. Using liquid nitrogen allows testing at temperatures that are 80 % of the difference in temperature between room temperature and the saturation temperature of liquid hydrogen. Testing the inverter at temperatures that are representative of a hydrogen cooled system could be performed using a cryo-cooler. To overcome the limitation of low heat dissipation of a cryo-cooler a large thermal inertia could be initially cooled, and short-duration tests of the inverter could be conducted before the temperature rises.

2. In systems using liquid nitrogen to cool HTS, the heat from a cryogenic motor drive would be rejected into the flow of LN2. This would occur in a two-phase heat exchanger. A heat sink optimised for the large heat fluxes from the GaN dies and the two-phase flow of liquid nitrogen or hydrogen will be required if inverters operating closer to their thermal limit are developed.

3. The thermal conductivity of silicon increases at cryogenic temperatures, resulting in it being three times more thermally conductive than copper at the temperature of liquid nitrogen. The high thermal conductivity of silicon could be exploited in power device designs specifically for cryogenic applications.

4. The prototype inverter could be integrated into a fully cryogenic motor drive, incorporating cryogenically cooled EMI filters and bus capacitors. The pool boiling cooling method could also be modified to be suitable for a motor drive application with a liquid nitrogen coolant flow. This could be achieved either with a cooling plate or by enclosing the power board in a chamber through which liquid nitrogen is flowed.

5. In [51] it is observed the breakdown voltage of the GaN HEMT used in this work increases by 20 % to 40 % at cryogenic temperatures. It may therefore be possible to use higher bus voltages at cryogenic temperatures, improving the efficiency of the inverter.

Appendix A

Calorimetric Measurement Uncertainty

The uncertainty in the calorimetric loss method predominately results from the measurement uncertainty in the power measurement and the experimental uncertainty in the calibration of the boiling rate.

A.1 Calibration Measurement Accuracy

The measurement uncertainty in the heat dissipated and boiling rate are calculated in this section.

A.1.1 Heat dissipation measurement uncertainty

The heat dissipated in the reverse conducting transistors during a calibration test is calculated as:

$$Q = \frac{1}{N}\sum_{i=1}^{N} V_i \cdot I_i \tag{A.1}$$

Where V and I are individual voltage and current measurements. The uncertainty in the DC power measurement is therefore given by:

$$\sigma_Q = \frac{1}{N}\sum_{i=1}^{N}\left(Q_i \cdot \sqrt{\left(\frac{\sigma_{V_i}}{V_i}\right)^2 + \left(\frac{\sigma_{I_i}}{I_i}\right)^2}\right)^2 \tag{A.2}$$

Where:

$$V_i = \frac{V_{\mathrm{ADC},i}}{G_{\mathrm{v}}} \qquad \sigma_{V_i} = V_i \cdot \sqrt{\left(\frac{\sigma_{\mathrm{ADC,V_{ADC,i}}}}{V_{\mathrm{ADC,V_{ADC,i}}}}\right)^2 + \left(\frac{\sigma_{G_{\mathrm{V}}}}{G_{\mathrm{V}}}\right)^2} \tag{A.3}$$

$$I_i = \frac{V_{\mathrm{shunt},i}}{R_{\mathrm{shunt}}} \qquad \sigma_{I_i} = I_i \cdot \sqrt{\left(\frac{\sigma_{\mathrm{ADC,V_{shunt,i}}}}{V_{\mathrm{ADC,V_{shunt,i}}}}\right)^2 + \left(\frac{\sigma_{R_{\mathrm{shunt}}}}{R_{\mathrm{shunt}}}\right)^2} \tag{A.4}$$

Table A.1: Values used in the uncertainty analysis.

Variable	Value	Error, σ
R_1	$14.9404\,\mathrm{k\Omega}$	$\pm 1.7978\,\Omega$
R_2	$99.8862\,\mathrm{k\Omega}$	$\pm 10.0386\,\Omega$
G_V	0.1301	$\pm 2.2937 \times 10^{-5}$
R_shunt	$2\,\mathrm{m\Omega}$	$\pm 5\,\mu\Omega$

The ADC error, σ_ADC, can be estimated from the maximum 0.2% gain error and the $400\,\mu\mathrm{V}$ offset error given in the datasheet for the Pico ADC20 used.

$$\sigma_{ADC} = \sqrt{\left(2 \times 10^{-3} \cdot V_\mathrm{ADC}\right)^2 + \left(4 \times 10^{-4}\right)^2} \tag{A.5}$$

The voltage gain error $\sigma_{\mathrm{G_V}}$ is from the measurement error of the two resistances in the potential divider. Which are combined using propagation of errors for a potential divider function to give:

$$\sigma_{\mathrm{G_V}} = \frac{\sqrt{\left(R_1\sigma_{\mathrm{R_2}}\right)^2 + \left(R_2\sigma_{\mathrm{R_1}}\right)^2}}{\left(R_1 + R_2\right)^2} \tag{A.6}$$

The error of the resistance measurement is estimated from the DMM6500 datasheet for a 4 wire measurement in $100\,\mathrm{k\Omega}$ range.

$$\sigma_{\mathrm{R_x}} = \sqrt{\left(10^{-4}R_x\right)^2 + \left(10^{-5} \cdot 100 \times 10^3\right)^2} \tag{A.7}$$

The shunt resistor error is taken from the Reidon RSA datahsheet as $\pm 0.25\%$ meaning $\sigma_{\mathrm{R_{shunt}}} = 0.0025 R_\mathrm{shunt}$.

A.1.2 Boiling rate measurement uncertainty

The boiling rate is calculated by performing an ordinary linear regression on the ToF displacement measurement, x, giving the boiling rate $\frac{dx}{dt} = B$. Assuming that the error in the range measurement is normally distributed, the standard error for the boiling rate, σ_B, can be calculated. Any offset error in the range measurement is assumed constant and therefore results in zero error in the boiling rate.

$$\sigma_B = \sqrt{\frac{1}{n-2}\frac{\sum_{i=1}^{n}\left(x_i - \bar{x}\right)^2}{\sum_{i=1}^{n}\left(t_i - \bar{t}\right)^2}} \tag{A.8}$$

The result of this calculation is plotted as shaded regions overlaying each line of best fit on Fig. 5.18a. It can be seen the uncertainty is small.

A.1.3 Calibration experimental uncertainty

It can be seen from the error bars in Fig. 5.18b, which show the measurement error of the boiling rate and heat dissipation, that the measurement uncertainty is negligible compared to the random variation in the experiment. A single data-point was identified as anomalous; this was the first data-point collected and is likely due to the inverter not reaching a steady-state temperature before the test was started. The standard error of the regression of the known losses to the measured boiling rates is calculated and plotted in Fig. 5.18b as a shaded red region.

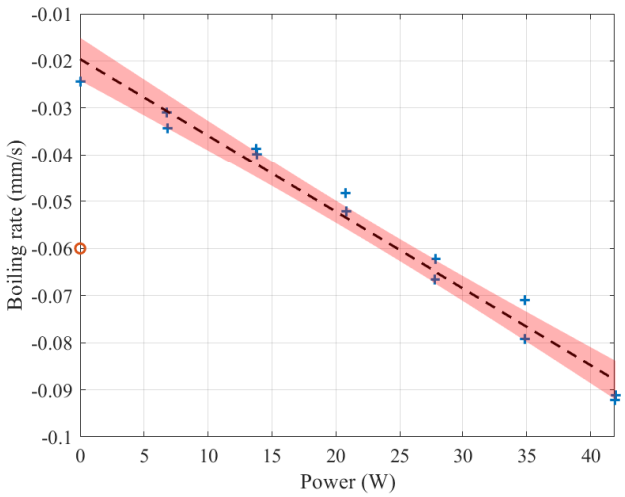


Figure A.1: Plot of the boiling rate against heat dissipation with the standard error of the regression shown shaded.

A.2 Loss and Efficiency Uncertainty

A reverse regression is performed, using the known losses and boiling rates measured in the calibration step, to estimate the inverter losses from a new measurement of the boiling rate. It is clear from 5.20 there is minimal uncertainty in the new measurement of the boiling rate. The largest source of error in the loss measurement is the error associated with reverse regression performed on the calibration data. For each loss estimate plotted, the vertical error bars indicate the standard error of the reverse regression. The largest error on any of the loss estimates is $\pm 2.6\,\mathrm{W}$. This method is a simplification as the regressor is assumed to have zero error, which is not the case, but it is suitable for the level of accuracy required. Inverse and reverse estimation in an engineering context is discussed in [128].

The error in the efficiency is calculated using the standard propagation of errors technique as explained in Section 5.5. The maximum uncertainty in the efficiency measurement is calculated as $\Delta\eta_{c,max} = \pm 0.0496\%$. This is of the magnitude predicted by the analysis in Section 5.5.

The typical uncertainty of an AC power measurement is ± 3 % [124]. This error is shown with horizontal error bars on the loss and efficiency plots.

Appendix B

Efficiency Requirement Assumptions

In this appendix, the assumptions that lead to values for the HFC efficiency (η_{HHV}), the change in the fluid quality ($\Delta\chi$), and the change in temperature of the hydrogen (ΔT) that are subsequently used in the calculation in Section 4.5.1 are explained.

B.1 Modelling Assumptions

B.1.1 Hydrogen Fuel Cell Efficiency

Efficiency for a reversible chemical reaction, such as the redox reaction that occurs in a HFC, can be expressed as

$$\eta_{\text{HHV}} = \frac{W}{m \cdot \Delta h_{\text{HHV}}} \tag{B.1}$$

Where W is work done, Δh_{HHV} is the higher heating value of the reaction [120], and m is the mass of the reacted hydrogen. For a fuel cell, the theoretical potential work that can be extracted is the Gibbs free energy, ΔG. In practice, the voltage efficiency limits the efficiency of a HFC, such that:

$$\eta_{\text{HHV}} = \frac{\Delta G}{\Delta h_{\text{HHV}}} \left(\frac{V}{E^0} \right) \tag{B.2}$$

The output voltage of a cell, V is lower than the reversible voltage of the reaction E^0 due to the activation losses (V_{act}), ohmic losses (V_{ohmic}) and the concentration losses (V_{conc}).

$$V = E^0 - V_{\text{act}} - V_{\text{ohmic}} - V_{\text{conc}} \tag{B.3}$$

For the values for hydrogen $\Delta G = 118\,\mathrm{MJ\,kg^{-1}}$ and $\Delta h_{\mathrm{HHV}} = 142\,\mathrm{MJ\,kg^{-1}}$, it is found that the upper limit ($V = E^0$) for the efficiency of HFC is 83%.

A reasonable example of the current state-of-the-art can be found in the Toyota Mirai HFC-powered road car. A technology assessment report [119] maps the system efficiency (including balance of plant) of the 82 kW HFC stack over the full range of its net system output power. It should be noted that in the report, the lower heating value rather than the higher heating value was used to calculate efficiency, which led to higher values of efficiency being reported. Using the LHV is appropriate when the excess heat from the reaction can be used to do useful work, which is likely not the case in an aircraft application. In this work, we have recalculated the efficiency using the HHV.

The peak HHV efficiency, η_{HHV}, of 54% is reported for an output power in the range of 3 kW to 11 kW. At the peak power of 82 kW, the efficiency is 33%. The output power of the HFC system is scaled so that during the cruise phase of flight, the HFC operates in the maximum efficiency range, as shown in Fig. B.1. We refer to this as the baseline efficiency. The peak HFC net output power is 400 kW, 54% of which is used during take-off.

The results presented in [119] and the observation regarding the linear voltage drop with respect to current density in [129] suggest it is reasonable to model the efficiency of the HFC as linear between the point of peak efficiency to the maximum power of the HFC. This approximation is plotted along with data from [119] in Fig. B.1. In the following sections we perform the analysis for the baseline case described, a low-efficiency case (10% lower than baseline), and a high-efficiency HFC case (10% higher than baseline). The peak efficiency of 66% in the high-efficiency HFC case is less than the theoretical maximum efficiency of the HFC, 83%. It is obvious but important to note that a higher fuel cell efficiency results in a lower hydrogen fuel rate and consequently lower cooling potential. This necessitates higher propulsion system efficiency.

B.1.2 Change in the fluid quality, $\Delta\chi$

As the temperature of the liquid hydrogen is far lower than the ambient environment, heatleak will occur from the surroundings to the hydrogen through the tank walls, transfer lines, and propulsion system components, in addition to the heat generated through losses. Of principal concern is the heatleak via the tank walls, due to the large surface area and time period the hydrogen must be stored in the tanks (multiple hours).

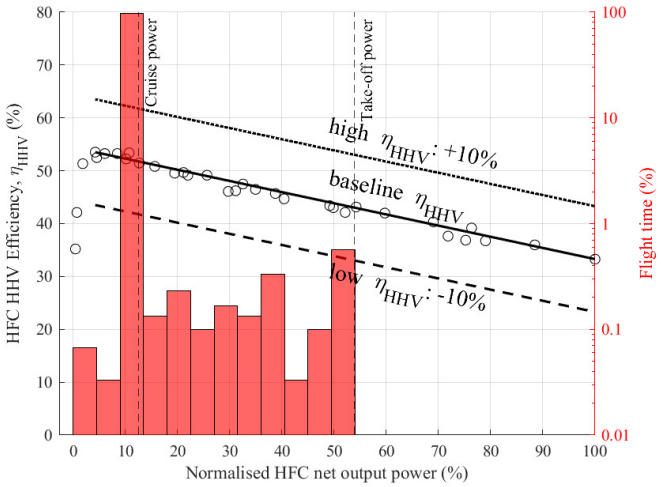


Figure B.1: The assumed hydrogen fuel cell efficiency is plotted for three cases, along with a histogram showing the fraction of flight time at each power output (note log scale). This highlights that the HFC operates near its peak efficiency for the majority of the flight. Data-points extracted from [119] for the Toyota Mirai HFC are plotted.

When computing the minimum required efficiency, the full cooling potential of the flow must be maximised and therefore the fluid at the outlet can be assumed to be fully evaporated ($\chi_{out} = 1$). For the inlet quality we consider two factors. The amount of heatleak that occurs in transfer lines between the tank and the propulsion system inlet, and the ratio of the hydrogen drawn from the tank as a liquid or a gas.

B.1.2.1 Tank heatleak

The power requirements for an aircraft can be approximated by considering the take-off and cruise phases of the flight. For a typical light aircraft, the take-off power is close to peak power for up to 10 minutes, while for the remainder of the flight, the cruise phase, 25 % to 35 % of peak power is required [20]. The mechanical shaft power for the representative flight profile is plotted in Fig. B.2. An altitude profile is also plotted (the flight profile does not model the decent phase of the flight). The aircraft is assumed to climb at a constant rate during the take-off phase to a typical cruising altitude.

Two approaches bound the design of the tank insulation:

I. A small amount of tank insulation designed to limit heatleak such that the boiling rate is equal to the consumption rate during the cruise phase of the flight. This minimises the insulation mass whilst not requiring venting of hydrogen during cruise.

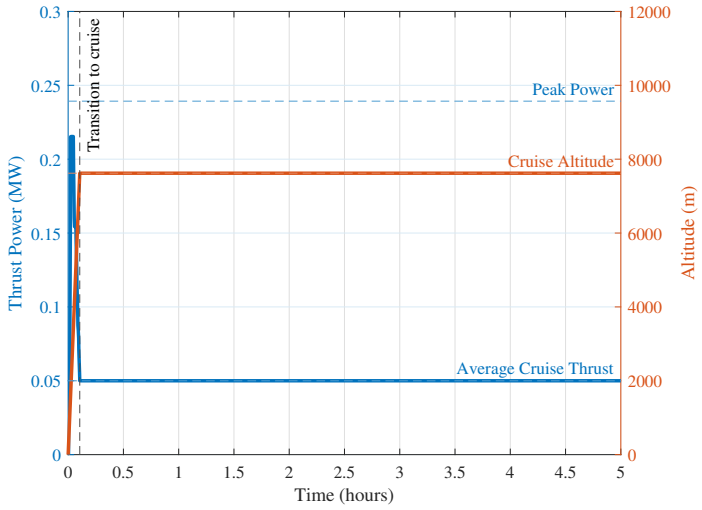


Figure B.2: Exemplar flight profile provided by Ricardo Ltd. The transition from take-off to the cruise phase of flight is marked with a vertical dashed line and the average cruise power.

II. The tanks are heavily insulated, resulting in a negligible boiling rate due to heat leak.

In Approach I, during the cruise phase, the heat leak evaporates sufficient gaseous hydrogen such that no liquid hydrogen will be drawn from the tank, except during take-off. During the cruise phase, the heat leak evaporates sufficient gaseous hydrogen to meet the required mass flow. In the take-off phase, liquid hydrogen will be drawn from the tank to supplement the gaseous hydrogen. This results in a larger cooling potential during take-off, due to the additional latent heat of vaporisation of the LH2. This is beneficial for a cryogenically cooled propulsion system, which can be expected to be less efficient during the peak power take-off phase. To limit the boiling-rate of the hydrogen, $\Delta\chi_{\text{tank}}$, adequate tank insulation is required. This can be achieved either with low thermal-conductivity insulation material, such as polyurethane foam [130], [131], or by using vacuum-jacketed vessels and multi-layer insulation (MLI) [132].

Approach II does not minimise the tank insulation, but may be necessary, especially if composite tanks are used. Although composite materials are viable for cryogenic storage tanks [133], delamination and other defects in the matrix structure are less predictable compared to aluminium tanks, where material behaviour is better understood. There may also be additional insulation requirements, either due to the dwell time of the aircraft between fuelling and take-off, or due to night flying restrictions and the need to avoid thermally cycling the tanks when the aircraft is on

the ground for extended periods. These may push the tank insulation requirement away from the small amount of insulation described in Approach I and towards the heavily insulated Approach II. A boiling rate of 0.1% per hour by weight is suggested by [134] and is used for analysis of Approach II.

B.1.2.2 Transfer-lines

For a flexible transfer line, a heat leak into the fluid of $1.2\,\mathrm{W\,m^{-1}}$ can be expected [135]. Considering the $P_{\mathrm{DC}} \approx 10\,\mathrm{MW}$ of cruise phase power and using the baseline case for η_{HHV}, the flowrate of hydrogen is $\dot{m}_{\mathrm{HFC}} = 126\,\mathrm{g\,s^{-1}}$. For the heat leak from the transfer lines to cause a 1% change in the fluid quality the length of the transfer lines would need to total 430 m. We therefore consider the effect of the transfer lines to be negligible.

B.1.2.3 Effect of ambient temperature

The effect of the change in ambient temperature between sea level and cruising altitude on the tank boiling rate was examined by modelling the tank insulation as a constant thermal resistance and adjusting the ΔT across the insulation using the International Standard Atmosphere Model [9]. It was found that the effect on the required propulsion system efficiency was negligible, as the majority of the cooling potential of the hydrogen is in the sensible heat, ie. a fractionally lower $\Delta\chi_{\mathrm{tank}}$ has negligible impact on the cooling potential. The same logic applies to the effect of the liquid level inside the hydrogen tank: although this will change the thermal resistance of the heat-leak path, its effect on the required propulsion system efficiency is negligible.

B.1.3 Maximum useful coolant temperature, T_{out}

At the inlet, the hydrogen is a saturated fluid meaning the fluid temperature is the saturation temperature, which is a function of the pressure. This is shown graphically in the P-h graph plotted in Fig. 1.3.

The coolant potential is very sensitive to T_{out}, so it is important to accurately determine this. The coolant temperature must be below the coldest component it cools with some margin to facilitate heat exchange.

We assume that the maximum useful temperature of the hydrogen is 223 K, equal to the temperature at cruising altitude. This assumption implies that the hydrogen

can be fully utilised to cool subsystems that do not require very low cryogenic temperatures, such as copper conductors, and that using the hydrogen as a coolant is not beneficial when lower coolant temperatures can be achieved through air cooling.

B.2 Results for $T_{\text{out}} = 223\,\text{K}$

The flight profile used in Section 4.5 is used as a case study to demonstrate the required efficiency change at the different flight stages. As per Section B.1 the variation in fuel cell efficiency and the change in fluid quality as a function of peak power is accounted for. The results of the analysis, shown in Fig. B.3, highlight the need to consider the different stages of flight when determining the efficiency requirements for a cryogenic aircraft propulsion system.

It can be seen that the efficiency of the propulsion system must increase by 1 % to 2 % between the take-off and cruise phases, with greater differences occurring when the HFC has lower efficiency and the tank insulation has been minimised.

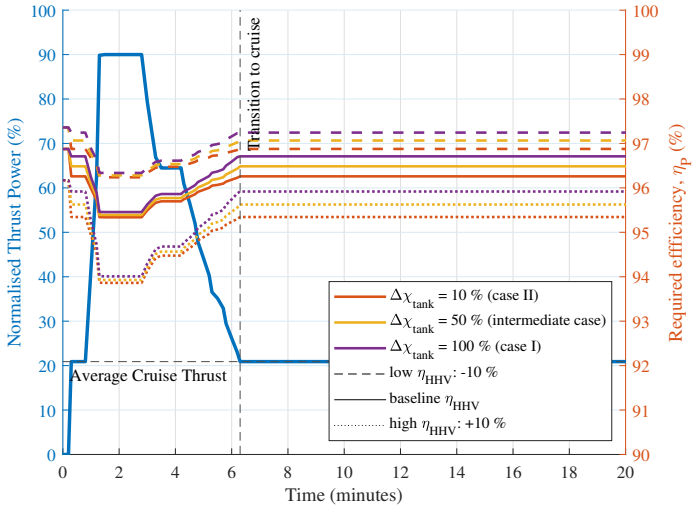


Figure B.3: The thrust power during take-off and start of the cruise phase are plotted along with the required efficiency of the propulsion system. The efficiency of the hydrogen fuel cell is denoted by the line style. To show the variation in required efficiency due to tank boil-off rates, three different design cases are shown with coloured lines.

Calculating the minimum system efficiency using Eq. 4.33 (assuming $\lambda = 1$), it is found that under the assumptions for approach I and a baseline η_{HHV}, a cryogenically cooled/fuelled propulsion system with an outlet temperature of 223 K must have an efficiency above 95.4% during take-off and 96.5% during the cruise phase.

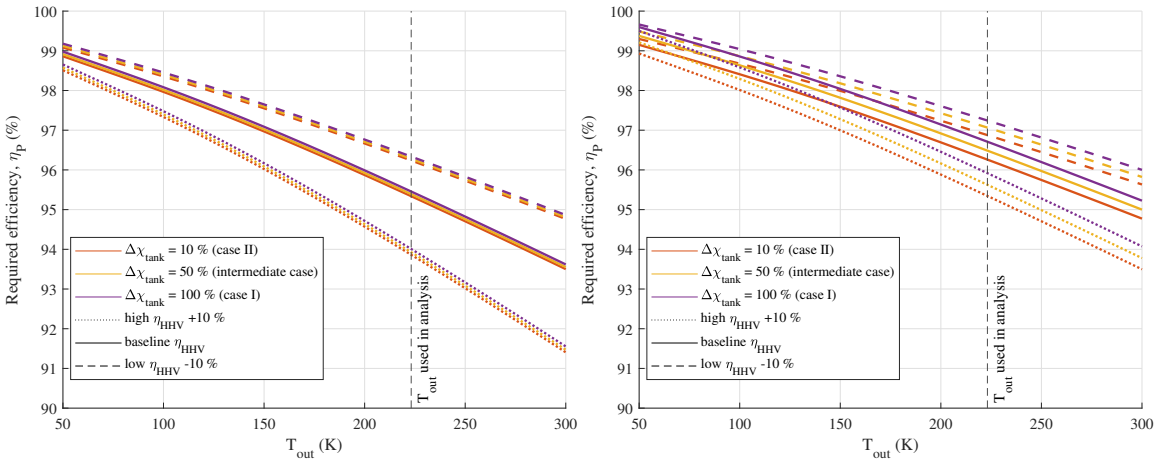
Values for α in Eq. 4.33 for the different assumptions at $T_{\text{out}} = 223\,\text{K}$ are given in table. B.1.

Table B.1: Computed values for α

Variable	Unit	Approach I	Approach II
$\Delta\chi_{\text{tank,cruise}}$	%	0.1	100
$\eta_{HFC,max}$	%	44	64
$\alpha_{\text{take-off}}$	-	0.038	0.026
α_{cruise}	-	0.047	0.028

B.3 Effect of T_{out}

The effect of varying T_{out} on the required efficiency of the propulsion system is presented graphically in Fig. B.4. The required efficiency during the take-off and cruise phases are plotted in Fig. B.4a and Fig. B.4b respectively.



(a) (b)

Figure B.4: Required efficiency as a function of T_{out}. (a) during take-off, (b) during cruise phase.

In the take-off phase, the required propulsion system efficiency is more sensitive to the HFC efficiency than the tank boiling rate. This is increasingly so for greater T_{out} as η_{HHV} determines the flow rate and the majority of the flow will be liquid (regardless of $\Delta\chi_{\text{tank}}$).

During the cruise phase at low T_{out}, the change in $\Delta\chi_{\text{tank}}$ has a larger effect on the required propulsion efficiency than η_{HHV} as the majority of the cooling budget comes from the remaining latent heat of vaporisation, which is proportional to $1 - \Delta\chi_{\text{tank}}$.

At higher T_{out}, $\Delta\chi_{\text{tank}}$ becomes a less significant variable and HFC efficiency is the dominant variable.

The sensitivity of the required efficiency, η_{P}, to the efficiency of the HFC, η_{HHV}, helps the designer of a cryogenic powertrain. At higher power, where the power electronics and motor can be expected to operate less efficiently, the HFC also operates less efficiently, resulting in a larger cooling budget.

It might be thought that the hydrogen could be used to cool the HFC, but it can be seen that the HFC has a much lower efficiency than the minimum efficiency of the propulsion system set by the cooling budget of the liquid hydrogen. Therefore, it is necessary to employ conventional cooling systems for the HFC, using external air as the coolant medium. External air is a suitable heat sink, as the HFC has an optimum temperature of approximately 353 K.

In [20] a target of $\geq 93\%$ is given for the average cruise efficiency. The analysis shown in Fig. B.3 suggest that this would be insufficient if the propulsion system is to be entirely cryogenically cooled.

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