Impurity and defect mitigation for silicon photovoltaics



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Declaration

I confirm that the work presented in this thesis is my own. Where I have consulted the work of others, it has been clearly stated.

Abstract

This thesis details a number of techniques designed to improve the efficiency of solar cells by reducing the impact of efficiency-limiting defects. The defects targeted by this work include transition metal impurities located within the as-cast silicon wafer, and dangling silicon bonds located at the wafer surfaces. This thesis has been divided into three techniques that have been studied.

Firstly, saw damage gettering which is designed to remove impurities from low quality silicon wafers which may have otherwise been discarded. Saw damage gettering removes impurities from the active region of the solar cell by capturing them in a surface region which can then be removed before solar cell processing. This technique therefore allows low quality silicon wafers to be 'upgraded' such that they can be re-introduced into conventional processing lines. In this thesis it has been shown that saw damage gettering can stably reduce the iron concentration in wafers, a notable factor in reducing solar cell efficiency. It has been shown that this technique can result in a 68% reduction in iron concentration, even after further thermal processing.

Secondly, gas phase gettering is a technique that removes impurities from the silicon wafer by enabling the impurities to react with a gaseous atmosphere which can then be removed from the silicon. In this work, the thermodynamics and kinetics of reactions between impurities and gettering agents are investigated and an optimal gettering agent, molecular chlorine, is proposed. Gas phase gettering using this species was then tested and found to enable gettering at all temperatures trialled. It was seen to reduce iron concentrations to the detection limit, which is notably a reduction in interstitial iron concentration of three orders of magnitude.

The final technique developed was shielded hydrogen passivation. In this technique, monatomic hydrogen is provided to a silicon/dielectric interface where it reduces the density of dangling bonds, improving the cell efficiency. The monatomic hydrogen is provided by a plasma, which can introduce damage to the surface regions. A significant body of this work was focussed on

mitigating this damage, without preventing the passivation process. Ultimately, shielding the samples with palladium enabled very high lifetimes of 4 ms on 1 Ωcm n type material.

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Peter Wilshaw was my supervisor during this project.

Thesis work contributions

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"Saw damage gettering" (5th international conference on silicon photovoltaics, siliconPV, 2015)

"Extrinsic passivation of silicon surfaces for solar cells" (5th international conference on silicon photovoltaics, siliconPV, 2015)

"Investigation of parasitic edge recombination in high-lifetime oxidized N-Si" (GADEST, 2015)

"Minority carrier lifetime improvement of multicrystalline silicon using combined saw damage gettering and emitter formation" (GADEST, 2015)

"Saw Damage Gettering to Upgrade Low Quality Multicrystalline Silicon for Solar Applications" (GADEST 2013)

Papers

"Saw damage gettering for improved multicrystalline silicon" (Energy Procedia 2015)

"Minority carrier lifetime improvement of multicrystalline silicon using combined saw damage gettering and emitter formation" (Solid State Phenomenon 2015)

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Glossary

Boe	barrels of oil equivalent
DI	de-ionised water
F_f	Fill factor of a solar cell
fz-Si	float zone silicon
FEP	field effect passivation
FGA	forming gas anneals
GPG	gas phase gettering
HF	Hydrofluoric acid
HCL	hydrogen chloride
H:Si_xN	hydrogen rich silicon nitride
IC	Integrated circuit industry
I_{SC}	Short circuit current of a solar cell
IV curve	The relationship between the voltage and current of a solar cell
J_{oc}	Open circuit current density of a solar cell
mc-Si	multicrystalline silicon
PL	photoluminescence decay
PTFE	polytetrafluoroethylene
PDG	phosphorous diffusion gettering
PD	phosphorous diffusion
PSG	phosphorous/silicon glass
P_{max}	Maximum power produced by a solar cell
(r)PECVD	(remote) plasma enhanced chemical vapour deposition
p/n type	Silicon with either holes of electrons as the majority carriers
pn junction gradient	The space between p and n type regions where there is an electrical field
PV	Photovoltaics
QSSPC	quasi steady state lifetime measurement
RZ	Red Zone (discarded from a multicrystalline ingot)
RCA	radio corporation of America clean
SD	Saw damage

SDG	saw damage gettering
SHP	shielded hydrogen passivation
SiP	Silicon/phosphorous precipitate
SOG	spin on glass
TMAH	trymethylammoniumhydrate
UMG-Si	Upgraded metallurgical grade silicon
V_{oc}	Open circuit voltage of a solar cell
$Watt_{peak}$	The cost of a solar system averaged over the number of watts produced by the system operating at peak solar illuminance.

List of symbols

B	PL adjustment constant
c	concentration of mobile impurities
C_p	heat capacity
D_T	impurity diffusivity at temperature T
D_0	diffusivity correction factor
D_{mc}	minority carrier diffusivity
d	sample thickness
Ea	Activation energy for a process including impurity release from a sink
$E_c/E_v/E_t$	Energy of the edge of the conduction/ valence/ trap levels.
F	number of collisions between the solid and gas particles per unit time and area
$F_{(Fe)}$	collision rate between a surface (impurity atom) and a specific gaseous species
G_{en}	generation rate of electron hole pairs under illumination
G	Gibbs free energy
g	geometric constant for diffusion
$(\Delta)G_{(reaction)}$	Gibbs free energy (change when the reaction proceeds)
$H_{(x)}$	enthalpy (of some component of the system)
i	the number of cooling steps at a given point in a diffusion model
J	impurity flux
k	Boltzmann's constant
L	characteristic diffusion length for a given time
l	mean free path of molecules in a gas
n	number density of gaseous species in a gas
N_c/N_v	Effective densities of states in the conduction/valence band
N_t	Density of defects (type t) within the band gap
Δn	Excess concentration of carriers introduced by illumination
m	mass of gaseous species
σ_p/σ_n	A trap's capture cross section for holes/ electrons
$\phi_{PL}(t)$	time dependent PL signal
P	Partial pressure of a specific gaseous species
p	pressure

p_0/n_0	Equilibrium concentrations of holes/electrons in the silicon in the dark
R_t	Recombination rate due to trap t
R_s	Series resistance in a solar cell
R_{SH}	Shunt resistance in a solar cell
r	radius of a molecule
S_{RV}	surface recombination velocity
$S_{(x)}$	entropy (of some component of the system)
T	Absolute temperature
t	time
τ_{total}	The lifetime of a silicon wafer
τ_n	How the variable n limits the lifetime of a silicon wafer
v_{th}	Thermal velocity of electrons
V	rate constant
$[X]_{is/bulk}$	concentration of atom X in an impurity sink/ in solution
x	distance
X_0	a pre exponential term used to find how X varies with temperature
{X}	fraction of atoms in solid which are species X

Preface

This thesis details the work that I have undertaken while at the Materials department in the University of Oxford. An introduction chapter will provide an overview of the current status of solar power and a background to silicon photovoltaics. The remainder of this thesis can then be split into two broad topics; gettering and passivation. My work on the former is split into two chapters, and has a chapter dedicated to a more specific literature review. Passivation is a stand-alone chapter with an incorporated literature review. All results chapters contain a conclusion and discussion on further work, and therefore this thesis will not have a dedicated further work chapter.

1 Introduction

In this chapter, the economic case for solar power, focussing on silicon based photovoltaics will be discussed. This is be followed by an explanation about how solar power works, including the major challenges that it faces. Finally, this chapter will detail the different types of silicon used in this work.

1.1 Economic case for solar power

The economic case for solar power requires a broader understanding of the global energy markets. This is detailed below.

1.1.1 Global energy usage

Readily available energy is required for modern society to function, and therefore understanding global usage, costs and supply methods is of great importance to a number of entities, both public and private. Hence, energy usage is carefully studied and predictions about how it will change are made by a number of organisations. World power consumption was estimated to be 1.55×10^5 Terrawatt-hours per year in 2012 [1]. Although different models do not completely agree on how this figure will change in the future they all agree that the demand for energy will continue to grow significantly[1] [2] [3] (Table 1). There are a number of technologies which may be able to provide this additional energy but a number of them are associated with some undesirable consequences as will be discussed.

Modelling institution	Predicted energy increase by 2040 (%)
BP plc	47 (extrapolated from prediction to 2035)[2]
US Energy Information Administration	56[1]
Exxon Mobile	35[3]

Table 1 A number of predictions for global energy consumption.

1.1.2 Fossil fuels

There is still a very large quantity of known, unconsumed fossil fuels. If proven reserves of oil, gas and coal are combined there is 7 trillion barrels of oil equivalent (boe), which rises by 66

trillion boe if all estimated reserves are included, the majority of which (5.5 trillion boe) is coal. At current consumption rates the proven oil reserves would last approximately 40 years, and other fossil fuels such as coal could then be used to provide further power. However, there are other issues associated with increased fossil fuel use.

The consumption of fossil fuels releases large quantities of carbon dioxide into the atmosphere (in 2010, 9×10^{12} kg of carbon dioxide was released [4]). The prolonged, intense, use of fossil fuels has already caused the concentration of carbon dioxide in our atmosphere to increase significantly (from ~315 ppm in 1960 to ~395 ppm in 2013[5]), see Figure 1. These gases reduce the energy radiating away from the earth's atmosphere, which subsequently heats. These gas releases have been strongly linked with increasing mean global temperature [6]. It is predicted that these temperature changes will have a number of detrimental effects. These include extensive flooding caused by rises in global ocean levels, changes to ecosystems [7] which in turn are likely to adversely affect food supply, and distortion of weather systems leading to an increase in the frequency of extreme weather events and reduced water security [8]. Due to the detrimental nature of these effects, the development of alternative power sources which do not produce these effects is highly desirable.

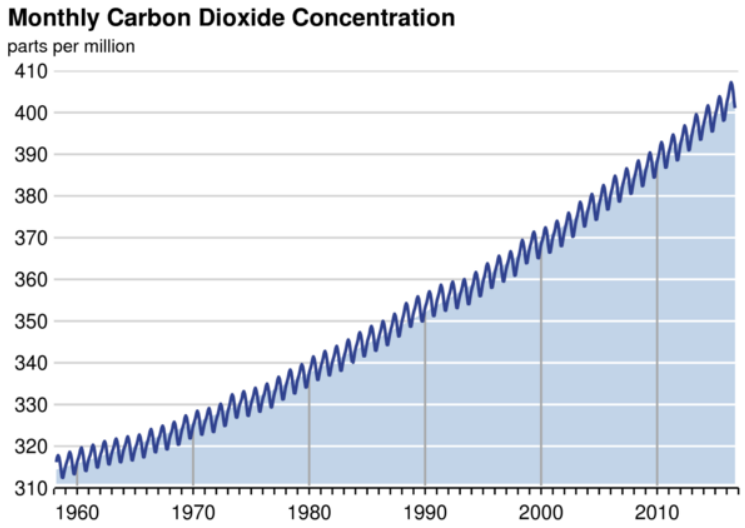


Figure 1. Monthly average atmospheric CO_2 levels at Mauna Loa [5]

1.1.3 Nuclear power

Nuclear reactors can produce large amounts of power with minimal carbon dioxide emissions. It is a relatively advanced industry which produced 10.9 percent of global electricity in 2012 [9]. However, there are issues associated with significantly increasing its output. Firstly, there is quite significant public fear associated with its usage. This fear has periodically been enhanced by devastating accidents such as the Chernobyl disaster in 1986, and more recently at Fukushima. The latter resulted in Germany aiming to phase out all of its nuclear reactors by 2022 [10]. In addition nuclear reactors produce hazardous waste products which must be stored for extensive periods of time, ~1,000 years, before they cease to be dangerous [11]. Currently this waste material is manageable, but may become more problematic if produced in significantly greater quantities. Additionally, even if these safety concerns are completely addressed, nuclear power is anticipated to be too expensive to be a complete replacement for fossil fuels [12]. This may become more pronounced if additional safety measures are required.

1.1.4 Renewables

There are a large number of techniques which extract energy from naturally occurring processes to generate electricity. The most important of these are wind, hydro-electric and solar power. The vast majority of the energy driving these natural processes originates from the sun [13]. Table 2 and Figure 2 highlight the amount of usable energy that these sources could provide. From this it can be seen that these renewable sources could easily satisfy global power demands. The potential offered by solar power is particularly notable.

Renewable energy source	Fraction of available energy source needed to supply total global energy demand
Wind	0.05 [14]
Hydroelectric	1 [15]
Solar	0.0003 [15]

Table 2. The fraction of the renewable source which must be utilised if the world's energy demands were to be satisfied by this technology alone.

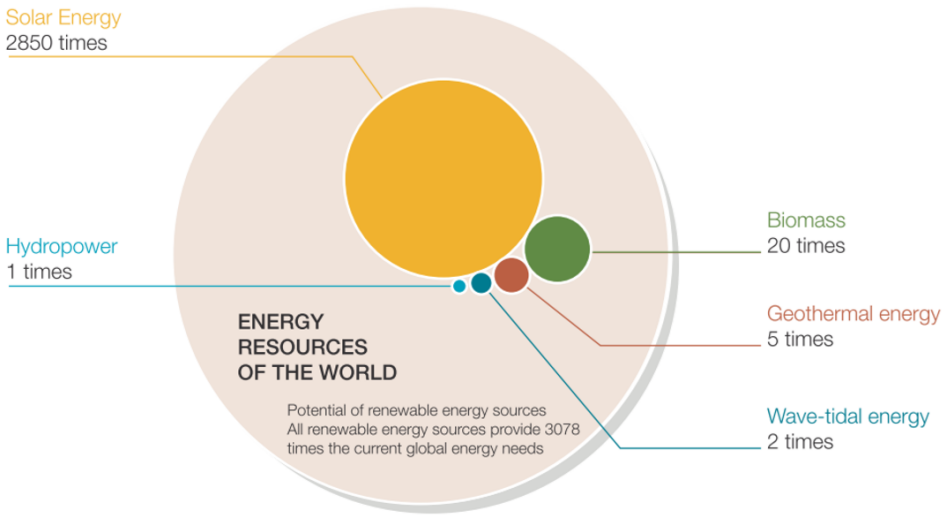


Figure 2. The amount of energy available from each major renewable energy source is highlighted. Solar power can be seen to be capable of supplying all global energy needs [15].

1.1.5 Solar Power

As discussed, solar power is technically capable of satisfying all global energy demands. It is capable of doing so with minor ecological impact. It can also be installed at locations undesirable for other uses, such as in deserts. However, there are three major challenges which must first be overcome. Firstly, a method of storing the generated power must be developed such that the fluctuations in supply and demand can be overcome. Secondly, a power grid must be developed so solar power generated in remote locations can be transported to the place of usage with minimal resistive loses. Finally, the price per kilowatt-hour generated must be reduced, such that solar power becomes economically competitive. The latter issue is the focus of this thesis. Economic competiveness can either be improved by reducing the cost of a like for like system, or increasing the efficiency of a system without significantly increasing its costs. The costs associated with solar power are overwhelmingly due to production and installation with negligible maintenance costs. Therefore, prices are usually referred to as the price per watt of installed power, assuming some irradiance level ($Watt_{peak}$).

There are two primary ways of generating solar electricity. These are photovoltaics, the primary focus of this work, and concentrated solar power. The latter uses a series of optical devices to focus the irradiation from a large area into a small area. This intense illumination delivers the

heat necessary to create steam, which is then used in a turbine based power plant. This type of power generation can be modified to contain thermal storage, enabling the system to provide power at times of low irradiation. However, one of the principle drawbacks of this technique is that its use of a concentrator system means that it is ineffective in indirect sunlight, which limits its utility in many climates.

Solar photovoltaics (PV) directly converts irradiation into electrical power within the solar module. Currently, the dominant industrial technique is to use a crystalline silicon substrate to form the solar cell. This technique is used as it provides a modest efficiency cell <26% [16] at an economically favourable price. The remainder of this thesis focusses on crystalline silicon solar cells and this technique will be discussed at length over the remainder of this chapter.

The cost of silicon ingots makes a large fraction of the total cost of a silicon solar module, see Figure 3. The exact amount is dependent on the type of feedstock silicon used. For example silicon costs \$0.45 per $Watt_{peak}$ when using high quality single crystal silicon wafer [17], compared to \$0.1 per $Watt_{peak}$ when using multicrystalline silicon [18], although it should also be noted that cells produced from multicrystalline silicon are less efficient than single crystal cells, and as such some of the other costs associated with the complete system are higher. The silicon used for solar cells is expensive as strict purity and defect concentration criteria must be satisfied or the resultant modules would have low efficiencies. This link can be seen by comparing the efficiency of multicrystalline silicon cells with single crystal cells (21.3 % and 25.6 % record efficiencies respectively [19]) the latter has lower concentrations of impurities and crystallographic defects. If new processing techniques enabled cells to be made from lower quality, as cast, silicon without compromising on the final cell efficiency it would be possible to reduce the costs associated with solar power. This is one of the major goals of this work.

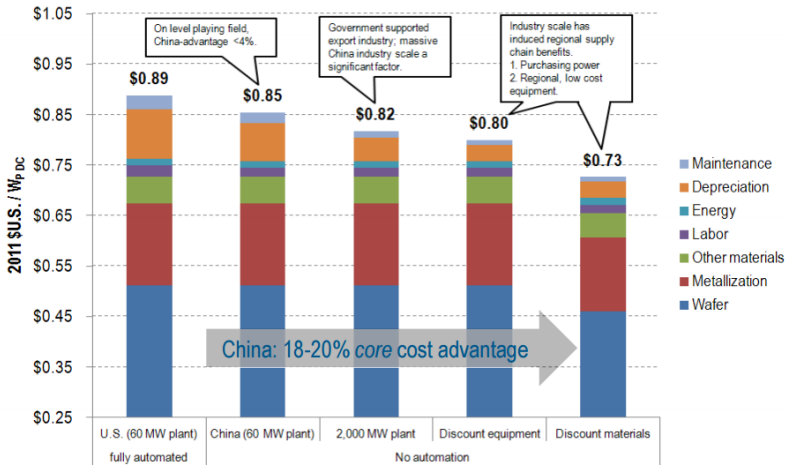


Figure 3. The costs associated with manufacturing a silicon PV module. The wafer costs can be seen to be highly important. From [17]

As seen in Figure 4, approximately half of the cost of a solar power system is associated with installation. These costs include purchasing and preparing land, additional electrical items such as wiring and inverters, and installation costs. These costs are strongly affected by the area of modules installed, but are largely independent of the modules' power. Thus the installation cost per watt can be reduced through the use of more efficient modules, which produce more power per unit area. The costs of solar power can be reduced by manufacturing more efficient modules, providing modules' costs do not increase significantly. This is the second major goal of this thesis.

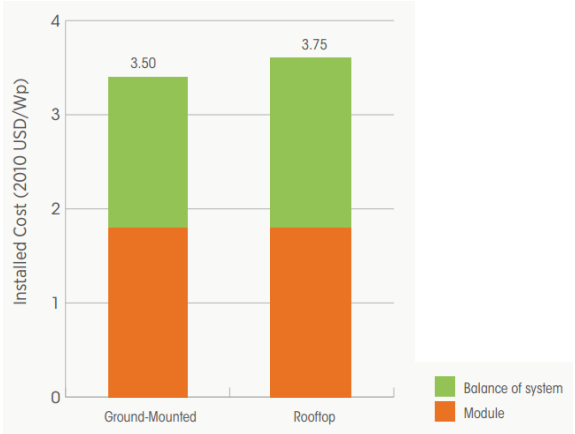


Figure 4. The costs associated with the complete installation of a solar power facility. The balance of system costs include business, installation, racking, site preparation, and electrical fitting costs. From [20]

1.2 Silicon solar cells

In this section the operation procedures, and typical manufacturing routes of silicon solar cells are discussed.

1.2.1 Principles of operation

The majority of silicon solar cells operate using the same principles. They all have regions of p-type and n-type doping separated by a pn junction, see Figure 5. The predominant, mobile, charge carriers in these regions are holes and electrons respectively. These are each connected to opposite poles of the external circuit. Incident photons with energy of more than 1.1 eV excite electrons from the silicon's valence to conduction band simultaneously generating a hole, producing two mobile charge carriers. The minority carriers in the vicinity of the junction drift across it to become majority carriers at the other side. Their energy is reduced in this process. This depletes the concentration of minority carriers adjacent to the junction so carriers diffuse to this region. Drift across the junction leads to charge build up at either side of the junction, and therefore a potential develops across the cell. This can be used to drive a current through an external circuit where it provides usable energy.

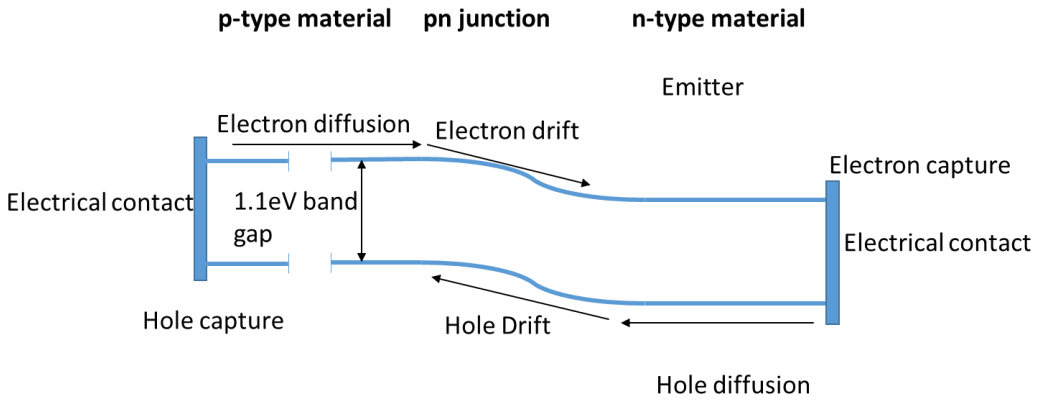


Figure 5. A schematic of a solar cell showing the movement of the different charge carriers. In this example, the majority of the wafer is p-type and the emitter is an n-type region. This diagram shows a solar cell under illumination, this schematic will be valid at all conditions between short circuit and open circuit conditions. The difference between the two will be a relative downwards shift of the n-type region when moving to open circuit conditions. The motion of the carriers when they have reached the regions where they become majority carriers is not shown as this will be determined by the resistance across the whole circuit including the external load.

The current/ voltage (IV) curve of a solar cell can be used to find its maximum efficiency, and also to find the resistance that should be applied if the cell is to deliver maximum power. Figure

6 shows the IV curves of a solar cell in the dark and under illumination. The maximum power will be supplied when the product of the current and voltage are at a maximum. This means the external load must be appropriately chosen. There are three important parameters which are used to determine the efficiency of a solar cell. These are the open circuit voltage (V_{oc}), short circuit current density (J_{sc}), and the fill factor (F_f). The latter is determined by:

1.2.1

$$F_f = \frac{P_{max}}{V_{oc} J_{sc}}$$

Where P_{max} is the power density produced by the cell at the optimum power point.

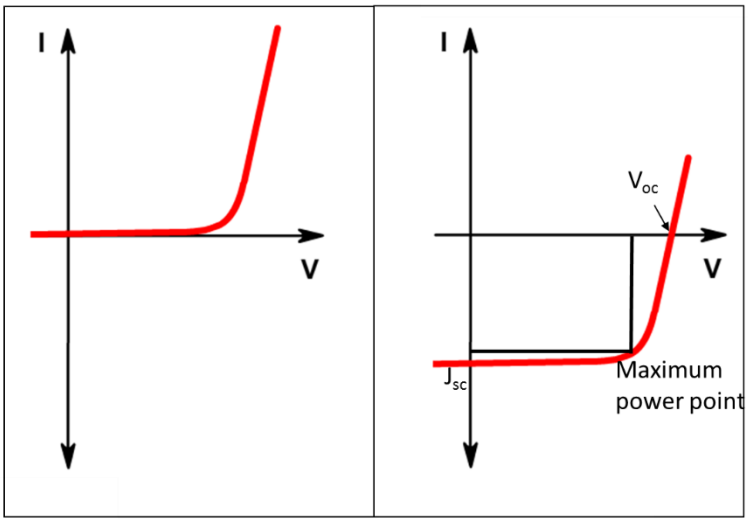


Figure 6. The IV curves of a solar cell, left without illumination and right with illumination. The optimal load for maximum efficiency is indicated on the right hand figure, from [21]**.**

A number of different solar cell geometries have been developed. The traditional solar cell is demonstrated in Figure 7A. It has its pn junction near the top of the cell so the majority of carriers are generated near the junction. This reduces the time between their generation and capture, reducing the probability of a recombination event, see section 1.3.2. This allows lower quality material to be used. However, this structure requires a metallic contact to be made on the top of the solar cell. The metal shadows the silicon, reducing the number of incident photons, and thus the number of electron hole pairs generated. Figure 7B shows a back contact, back junction solar cell. The electrical terminals are at the rear of the cell so there are no shading losses. However, the minority carriers generated at the front of the cell must now diffuse through the majority of the wafer thickness before reaching the junction. Recombination is thus more important in these cells. While recombination in the bulk of the cell can be

controlled by using high purity single crystal silicon, the surfaces can be more problematic, see chapter 6.

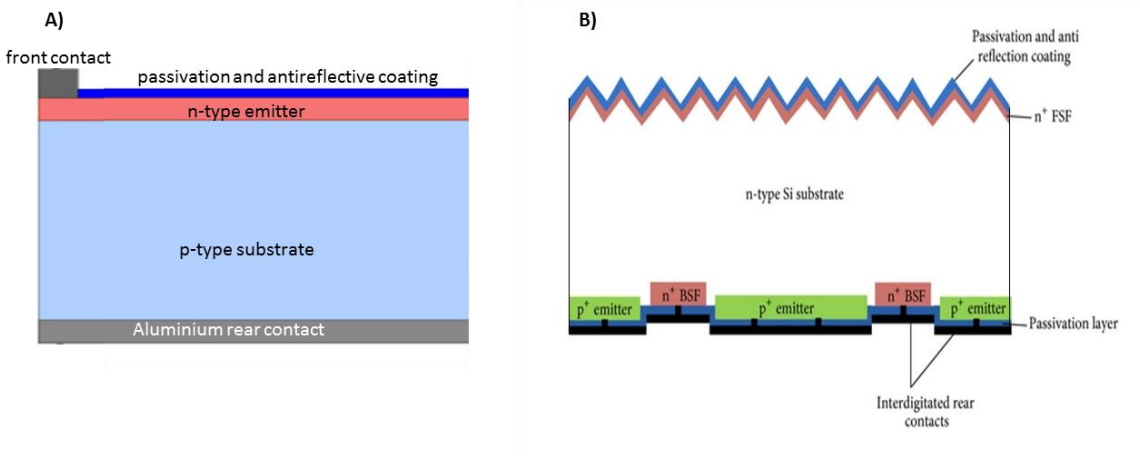


Figure 7. A). A schematic of a conventional solar cell with contacts on the top and bottom of the cell, modified from [21]**. B). A schematic of a rear contact, rear junction solar cell from** [22]

1.2.2 Cell manufacturing

The majority of current solar cells are manufactured in comparable ways. Firstly, the silicon used as the feedstock is purified. This silicon is then moved to a crucible and dopant is added. This dopant is typically boron which produces p-type silicon, although sometimes the wafer is doped with phosphorous instead if an n-type ingot is required. There are a number of alternative casting processes which produce silicon with very different properties. These are discussed in greater detail in section 1.4. Once the silicon ingots have been cast, they are sawn into wafers approximately 210 μm thick. During the sawing process, damaged regions are generated at the wafer surfaces [23]. These regions are highly detrimental to the cell efficiency and so are removed via chemical etching which removes approximately 10 μm of silicon on either side [21]. This etching process is also used to generate a pyramidal structure at the surface of the silicon, a process called texturing [24]. The textured surface reflects less light than an equivalent flat surface, increasing the number of photons entering the silicon and thus available for power generation. It is easier to produce a textured surface when using single crystal silicon as a pyramidal structure can be obtained through the use of an anisotropic etchant [25].

The wafers are then annealed in an atmosphere which contains dopant of the opposite type to that in the bulk of the wafer. This produces the emitter region at the surface of the silicon, and so also generates the pn junction needed to separate the charge carriers. The doping process typically leaves a dopant rich glass layer which is removed before further processing. The wafers are then coated in a dielectric layer to further reduce the reflectivity of the wafers. This layer also passivates the surfaces improving the cell efficiency, see chapter 6. Metallic contacts are then printed onto the surfaces of the wafer and are fired to produce an ohmic contact between the metal electrode and the underlying silicon. The rear surface often has full coverage, typically using aluminium paste, to minimise resistance. However, at the front it is important to optimise the surface coverage. Too little coverage can lead to resistive losses, and too much will shadow the silicon reducing the amount of light absorbed. This is typically achieved by using a number of thin "fingers" which ensure that the distance between any part of the silicon and a metallic contact is small. These fingers are thin, and thus have relatively high resistivity. They are then connected to less numerous, but thicker and more conductive, busbars which then carry the current to the external circuit. Finally, the cells are incorporated into modules and installed.

1.3 Efficiency limiting factors:

In this section the most important factors which limit a cell's efficiency are discussed.

1.3.1 Optical losses

The efficiency of a solar cell will be reduced if any of the light which shines upon it does not generate carrier pairs. There are a number of causes of this. Firstly, the light could be blocked by the top metal contacts. Secondly, the wafer could reflect the light. This is normally reduced by texturing and the application of an antireflective coating. Thirdly, photons could be absorbed without generating carrier pairs, for example if they were absorbed within the dielectric antireflective coating layer. Finally, it is possible that photons could pass through the silicon and be re-emitted from the rear side [26].

1.3.2 Recombination

Recombination is a process where an excited, and therefore conducting, electron and a hole annihilate each other. This process results in the restoration of the electron to a non-excited state and the removal of the hole. As such the charge carriers are lost from the system and the minority carriers do not reach the pn junction. This reduces the open circuit voltage, the short circuit current and the efficiency of the cell. This thesis aims to develop techniques to reduce the recombination in solar cells.

Silicon is an indirect band gap material, so electrons must change energy and momentum for recombination to occur. It is not simple to change both of these simultaneously, therefore un-mediated recombination is slow. Instead, recombination is typically mediated by a defect. These defects are associated with the introduction of energy states within silicon's energy band gap, these states are often de-localised in momentum space, Figure 8. As such the defects reduce, or remove the requirement for a simultaneous change in both energy and momentum. Consequently, defects increase the rate at which carriers recombine, decreasing the average time between generation, and recombination. This time is known as the minority carrier lifetime where τ_x is the lifetime of a wafer as determined by the lifetime limiting factor x. Multiple recombination mechanisms can be active simultaneously. The reciprocal of the lifetimes associated with each recombination mechanism can be added to obtain the overall sample lifetime, see equation *1.3.1*.

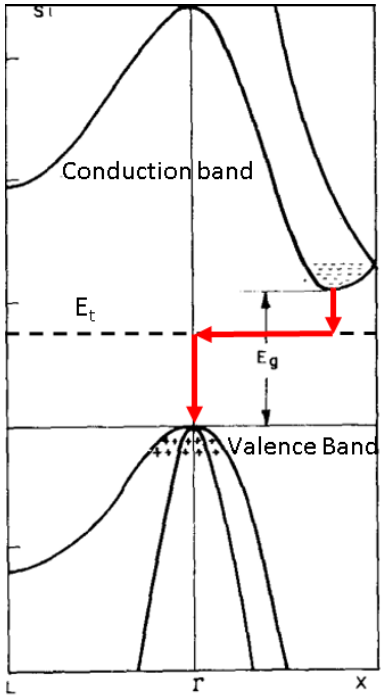


Figure 8. The band diagram of silicon. A recombination active defect level with energy E_t is included. The red arrows show a possible set of transitions which would allow an electron to relax to its ground state.

1.3.1

$$\frac{1}{\tau_{total}} = \frac{1}{\tau_1} + \frac{1}{\tau_{t2}} + \cdots \frac{1}{\tau_n}$$

1.3.2.1 Shockley Read Hall recombination statistics

All silicon, particularly the lower cost silicon used in many solar applications, has impurities present. Impurities in solution are effectively zero dimensional (point) defects, and they can significantly reduce the lifetime of a silicon wafer. The presence of even very low concentrations of transition metals significantly impact the efficiency of a standard solar cell [27], see Figure 9.

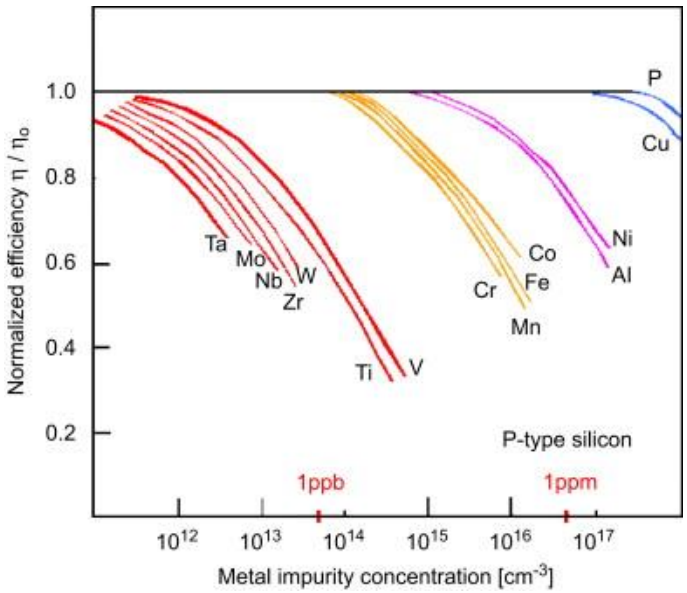


Figure 9. Effect of metallic impurity content in single crystal silicon on the normalized efficiency of solar cells from [27]

Shockley, Read and Hall (SRH) developed an effective model to describe recombination at point defects. In this model a point defect can capture a mobile charge carrier, immobilising it, and changing the charge state of the defect. The defect will then capture a charge carrier of the opposite type, restoring the defect to its original charge state. In this process the charge carriers are annihilated and the defect has facilitated their recombination. The equations which govern SRH recombination are detailed below (1.3.2 to 1.3.6) [28][29][30]. These can be used to determine how a series of defects with some concentration N_t affect the lifetime of a silicon wafer. Dividing the minority carrier density by the SRH lifetime will yield the recombination rate associated with the defect type, see equation 1.3.7.

1.3.2
$$\tau_{SRH} = \frac{\tau_{n0}(p_0+p_1+\Delta n)+\tau_{p0}(n_0+n_1+\Delta n)}{p_0+n_0+\Delta n}$$

Where τ_{SRH} equals the minority carrier lifetime associated with the defect type in question, p_0 and n_0 are respectively the hole and electron equilibrium concentration, and Δn is the excess concentration of carriers injected into the sample. Additionally;

1.3.3
$$n_1 = N_c exp(-\frac{E_c-E_t}{kT}),$$

1.3.4
$$p_1 = N_v exp(-\frac{E_t-E_v}{kT}),$$

n_1 and p_1 are the equilibrium concentration of, respectively, electrons and holes when the Fermi level is at the trap level, N_c and N_v are the effective densities of states in, respectively, the conduction and valence bands. E_c and E_v are the energy of the edge of the conduction and valence bands, and E_t is the energy level of the recombination active defect. T is the absolute temperature and k is Boltzmann's constant. Finally;

1.3.5 $$\tau_{p0} = (N_t \sigma_p \nu_{th})^{-1}$$

1.3.6 $$\tau_{n0} = (N_t \sigma_n \nu_{th})^{-1}$$

Where τ_{p0} is the average time for a negatively charged defect to capture a hole, τ_{n0} is the average time for a neutral defect to capture an electron, the defect recombination parameters would be different, but the math equivalent if the neutral defect captured holes and the charged defect captured electrons. N_t is the concentration of the defect, σ_p and σ_n are the capture cross section for holes and electrons respectively and ν_{th} is the thermal velocity.

1.3.7 $$R_t = \Delta n \frac{1}{\tau_t}$$

Where R_t is the recombination rate at a given trap, Δn is the minority carrier density and τ_t is the lifetime limitation of the trap.

These equations highlight a number of effects. Firstly, the lifetime is inversely proportional to the defect concentration. Secondly, it can be seen that defects act asymmetrically upon electrons and holes. Thirdly, reducing the concentration of minority carriers in particularly low lifetime regions can reduce the total recombination rate in the wafer. This is particularly important for highly defected surfaces.

1.3.2.2 Recombination at dislocations

Dislocations can be active recombination sites when they are contaminated by impurities, although they have minimal recombination activity when uncontaminated [31][32][33]. Dislocations are associated with two shallow defects states, above and below the valence and conduction bands respectively [34]. The dislocations therefore capture charge carriers and become charged with the same sign as the majority carrier type. As the charge concentration in

the dislocation rises, the flux of further majority carriers to the dislocation will fall while the flux of minority carriers will increase. Thus the concentration of minority carriers adjacent to dislocations tends to be higher than in the bulk of the wafer. However, "clean" dislocations (where there are few trapped impurities) typically are not particularly active recombination sites [31]. This is due to the lack of deep defect states needed for recombination. However, when impurities are bound to the dislocations they can introduce deep levels[35]. When this occurs, impurities, and their associated traps, are located next to a high concentration of both majority and minority carriers, and as discussed above, this means the recombination rate in this area will be high. Dislocations are thus highly detrimental unless free from impurities [32].

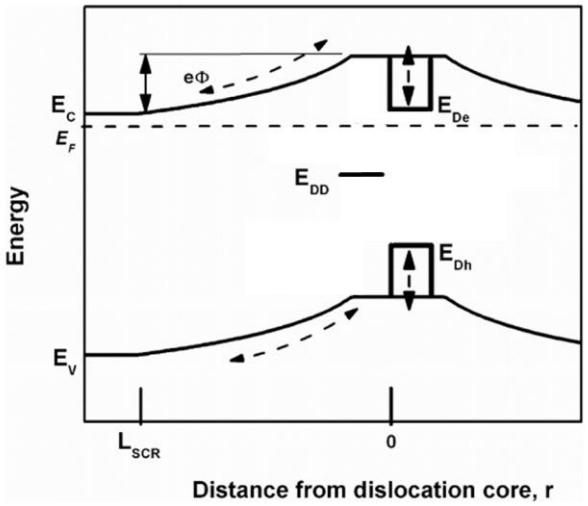


Figure 10. The energy diagram in the proximity of a dislocation core. The charge build up at the dislocation causes band bending. A deep energy level involved in recombination is present (E_{DD}). Adapted from [33]

1.3.3 Bulk Terminations: Surfaces and grain boundaries

Wafer surfaces are terminations in the crystal structure and so are associated with high concentrations of strained and broken silicon bonds. These defective bonds facilitate recombination, which is thus typically faster at surfaces than within the bulk of a wafer. The electrical activity of surfaces can be reduced through a process referred to as passivation which is discussed in greater detail in chapter 6.

1.3.4 Using SRH recombination statistics for characterisation

As discussed, SRH recombination centres significantly affect wafer lifetimes, this can be exploited to develop a sensitive characterisation technique for detecting impurity

concentrations. For this technique to work it must be possible to induce the impurities into two different states, without otherwise changing the silicon [36]. These two states have different SRH recombination parameters. Therefore, the sample lifetime will be different when the impurities are in the two different states [37]. If the SRH parameters of the two states are known, then the lifetime differences can be used to calculate the concentration of impurities which have transferred from one state to the other.

This technique works particularly well using iron as the impurity when the silicon is doped with boron. Iron can either be in an interstitial location or it can be paired with boron atoms. These two states have significantly different recombination parameters [37]. The iron can be induced into the interstitial form through the application of intense illumination for a short period of time. The overwhelming majority will then return to the bound state during a two day long room temperature "anneal". This technique is capable of detecting iron concentrations as low as 10^{10} cm^{-3}. This sensitivity is reduced by the presence of other recombination mechanisms.

1.3.5 Electrical losses

It is possible for power to be lost even after the carriers have crossed the pn junction and developed a potential. There are two causes of this. Firstly, resistances within the cell. These increase the resistance of the overall circuit, without doing useful work. This is referred to as series resistance. The most common causes of this are sheet resistance in the emitter, contact resistance and resistance in the metal contacts. The second loss mechanism is shunt resistance. This occurs when an electrical short is created across the pn junction allowing current to pass between the two terminals of the cell without first passing through the external circuit, see Figure 11.

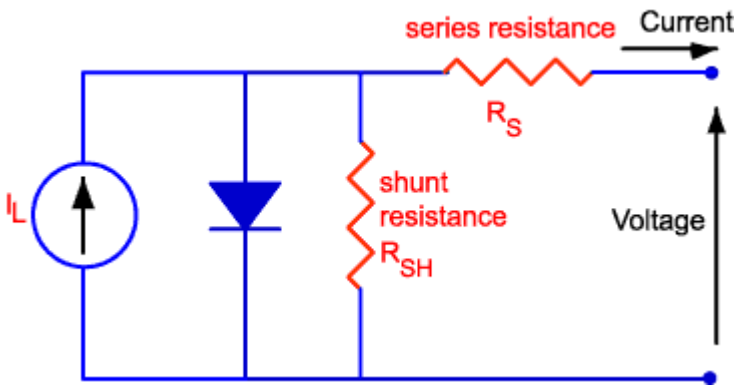


Figure 11. A solar cell which develops a voltage, but also has both series and shunt resistances which reduce the cell's efficiency, from [21].

1.4 Cast crystalline silicon

The silicon used during this work has been produced via a number of different techniques, and different imperfections limit the lifetime of these materials. During ingot casting, impurities segregate into the liquid rather than the growing solid see Figure 12. This is exploited to ensure that the majority of the cast silicon is purer than the feedstock that it is grown from, while the liquid becomes enriched in impurities. The final solid to form, assuming complete freezing, is highly contaminated compared to the feedstock as it will contain all of these segregated impurities.

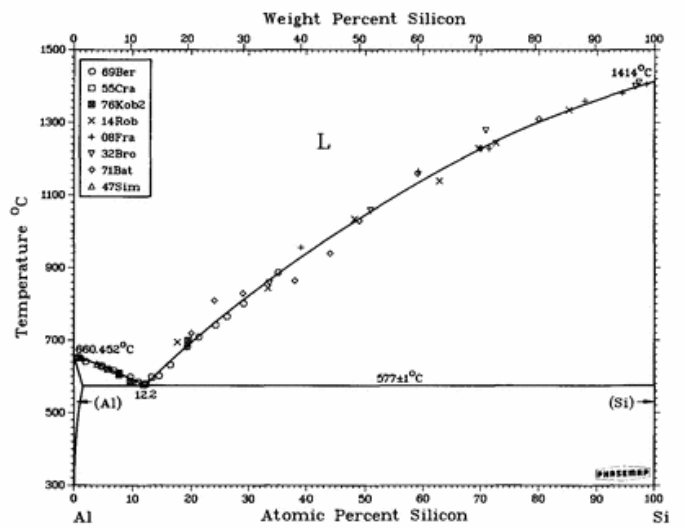


Figure 12. The aluminium-silicon phase diagram. Strong segregation of impurities into the melt can be seen by comparing the liquidus vs solidus gradients at the silicon rich side of this diagram, from [38].

After casting, the silicon is cut into wafers. This is carried out using a set of wire saws which simultaneously slice the whole ingot into wafers. Despite the brittle nature of silicon [39], this process introduces networks of dislocations into the surface regions of the silicon [40]. It also introduces a large number of small cracks. This saw damage is removed prior to solar cell completion as it would otherwise be highly recombination active. It may be polished away, chemically etched to a near flat surface, or chemically etched to a deliberately uneven surface to enhance light absorption [41].

1.4.1 Producing un-cast, polycrystalline silicon

Irrespective of the casting technique, the majority of silicon used for electronic applications is produced in a similar manner. This is based around the Siemens process. Firstly the silicon dioxide ore is reacted with carbon to form impure, metallurgical, silicon. This is then reacted with chlorine to form silicon tetrachloride. This is separated from any impurities through multiple distillation processes. Finally the chloride is electrically decomposed to form polycrystalline silicon [21].

An alternative silicon feedstock material (Upgraded Metallurgical Grade silicon UMG-Si), can be produced more cheaply and with a less energy intensive process. This uses the silicon produced directly from the ore, followed by additional processing. This often includes directional solidification of the material which, as discussed, produces regions of higher than mean purity. To date, UMG-Si cannot produce silicon with the same purity as can be achieved via the Seimens process [42].

1.4.2 Multi-crystalline silicon (mc-Si)

The cheapest method of casting silicon produces multi-crystalline silicon. A large volume of feedstock silicon is melted within a quartz crucible, typically much wider (~1 m) than its height (~25 cm). The heating is then adjusted such that strongly directional solidification starts from the bottom of the crucible. The growth of the ingot, and the associated impurity rejection, results in the majority of the ingot having a higher purity than its feedstock, despite being grown in a low purity crucible. Due to the large size of the ingots, the cooling rate is slow. This

means there is a long time for impurities to diffuse to low energy sites. During this cooling process the impurity solubility will fall so impurities are likely to form precipitates, so the majority of impurities in mc-Si will be located within precipitates [43].

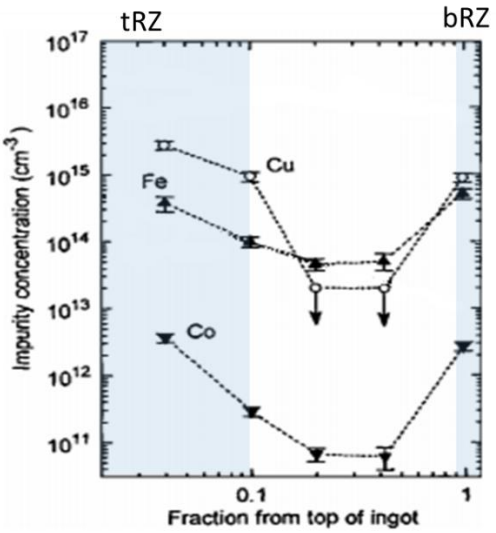


Figure 13. The impurity profile within a mc-Si ingot modified from[44]**. The concentrations of impurities is clearly seen to be elevated at the top and bottom of the ingot.**

The mc-Si casting process produces two regions with very low lifetimes which are normally discarded. The first, the bottom red zone (bRZ), is the first material to solidify and it becomes contaminated by the crucible. Impurities diffuse from the crucible- which is less pure then solidified silicon- into the hot, newly solidified silicon. At these temperatures impurity solubilities and diffusivities are high so the bottom, and edges of the silicon become highly contaminated [45], see Figure 13. The second low lifetime region, the top red zone (tRZ), is the last material to solidify and is undesirable for two reasons. Firstly, it contains all the impurities rejected from the solid into the melt as there is no longer anywhere else to reject them. Secondly, this region also contains a high concentration of dislocations. These form during solidification, and unless removed, grow through the ingot and multiply [46][47]. This dislocation multiplication limits the ingot height, [48] see Figure 14. High dislocation densities are associated with reduced minority carrier lifetimes even after processing to improve the silicon's quality [49]. Reducing dislocation densities has been the subject of much recent work. Significant progress appears to have been made in this area through a reduction in the final

grain size. This reduces dislocation multiplication during the growth of the ingot. Grain size reduction is achieved through either modifications to the crucible [50] or through seeding the solidification process [51]. Both of these increase the concentration of grains at the start of the solidification process.

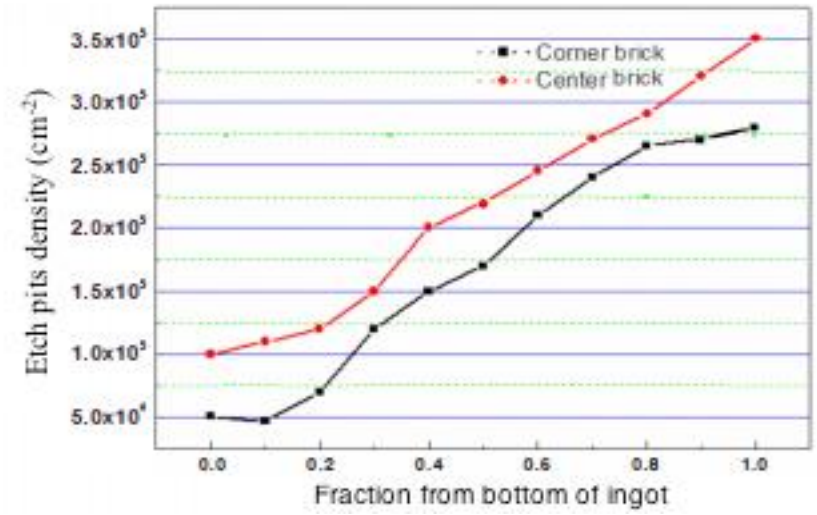


Figure 14. The dislocation profile within an mc-Si ingot from[52]**. In this work the wafer was selectively etched, such that etch pits formed where dislocation cores reached the surface of the wafer.**

The low cost mc-Si casting process produces a relatively low quality form of silicon. Impurities are present in high concentrations both in solution and within precipitates [47], see Figure 15. There are also a high concentration of crystallographic defects including dislocations, as mentioned above, and grain boundaries. These crystallographic defects are typically deleterious. It should also be noted that mc-Si is non-uniform. A mc-Si wafer will contain regions with high and low impurity and defect densities. This means that experiments using mc-Si must be carried out on numerous samples to reduce the importance of a particular region.

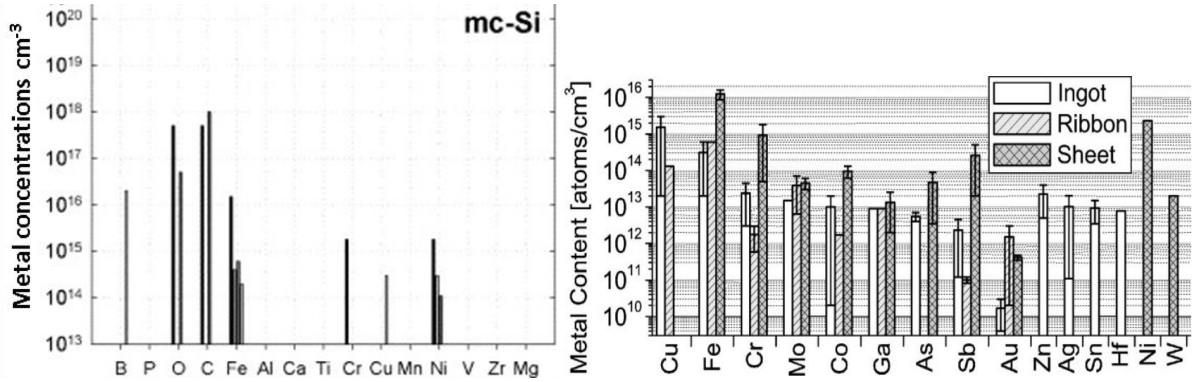


Figure 15. The impurity concentration of typical impurities in mc-Silicon. Where data is missing, this may be because the authors did not collect the data and is not to be taken to mean these impurities were not present. Left is from [53]**, right is from** [43] **where the ingot is mc-Si .**

The mc-Si wafers used in this work were p-type, 170 μm thick, 2 Ωcm wafers with the saw damage initially present. They came from both the top and bottom red zones as well as from the bulk of the ingot. Each of the wafers was cut into 3x3 cm samples, such that 25 stacks of sample were obtained, every sample within the stack had similar crystallography and impurity concentrations, although there were significant differences between stacks.

1.4.3 Float Zone (fz-Si)

The float zone process is used to produce the highest quality silicon (fz-Si). In this process a ring heating element is gradually moved up the cylindrical feedstock billet see Figure 16. This melts a small cross section of the billet, with the high surface tension of the silicon being used to prevent the silicon from pouring out of its ideal position. There are a few major advantages to this process. Firstly, the silicon is not contacted by a low purity crucible, which could otherwise cause contamination. Secondly, each pass of the molten zone, with the segregation processes mentioned earlier, moves a significant proportion of the impurities to one end of the ingot where they can be removed. As such fz-Si is can be very pure with very high lifetimes.

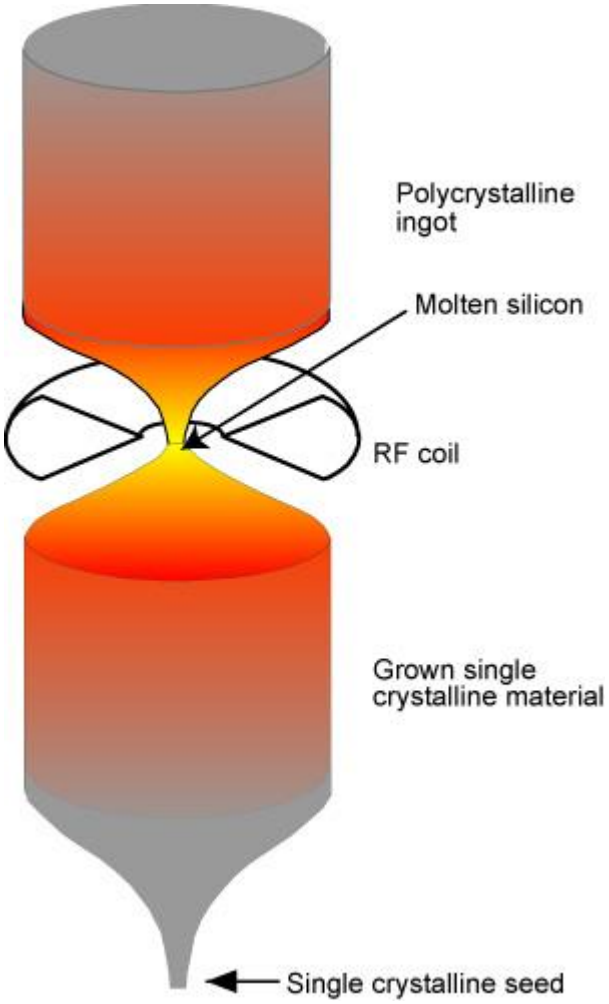


Figure 16. A schematic of the float zone process, this has cylindrical symmetry. From [21].

The float zone silicon used in this work was 1 Ωcm, 170 μm thick n-type silicon chemically polished on both sides. A high quality thermal oxide was then grown in a clean environment before the material was received for testing. These wafers have very low bulk recombination and therefore are excellent for evaluating surface passivation techniques.

1.5 Aims of this work

As has been explained in previous sections, the presence of impurities and defects induce carrier pair recombination, and thus reduce the efficiency of silicon solar cells. It is possible to ensure that few impurities remain in the silicon after the casting process. However, for this to be achieved, the silicon must be carefully purified prior to casting. This process is both energetically, and financially expensive. In addition, casting high purity silicon requires the use

of costly, low throughput casting processes increasing the cost of any resultant solar cell. It is possible to remove impurities from the silicon even after it has been cast, see chapter 4. While current techniques can improve the lifetime of silicon wafers, it is not possible to upgrade very low quality wafers such that they can be used for solar applications. For this to become possible a new technique for improving these wafers must be developed. This work aims to develop two new techniques for removing impurities. One removes impurities by redistributing them to a region which is subsequently removed. The second technique moves the impurities from the silicon into a gaseous atmosphere. These techniques are initially designed to improve the purity of the lowest quality silicon currently used for solar applications. These wafers may then be upgraded such that they become comparable to higher quality silicon wafers. It may subsequently become possible to use the techniques developed in this thesis to upgrade very low quality, low cost UMG-Si such that it can be used for solar applications.

Recombination due to defects at interfaces affects the efficiency of solar cells, particularly those made from high quality silicon. The activity of these defects can be controlled by both electrical, and chemical passivation introduced by depositing a surface coating layer as discussed further in chapter 6. These layers are significantly improved by the incorporation of hydrogen. Hydrogen can be incorporated intrinsically, during the growth of the coating layers, or extrinsically, in a dedicated hydrogenation process. Currently, extrinsic hydrogenation is a slow, and low throughput process, meaning it is not a widely used industrial technique. The second major goal of this work is to develop a new hydrogenation technique which may have a higher throughput. It is important that this technique does not simultaneously damage the samples. Consequently this work also studies the potentially active damage mechanisms to ensure they can be adequately prevented, see chapter 6 for more detail.

2 Experimental Methods

In this chapter the experimental and characterisation techniques used through the body of this work will be discussed. In addition, the work undertaken to set up a number of these experiments including design modifications, commissioning new equipment and developing safe usage protocols will be discussed. Unless otherwise stated, the wafers used in this work were 3 cm squares.

2.1 Wet chemistry

In this work, wet chemistry refers to any process where the reactants are dissolved in a liquid solvent. This has been used extensively for a number of sample processing techniques.

2.1.1 Dielectric etching

Dielectric layers deposited or grown on silicon –e.g. native oxide, silicon nitride or phosphorous/silicon glass (PSG), were removed using a 5 % hydrofluoric acid (HF) solution. Samples were loaded on a quartz wafer carrier and immersed into the HF bath. The samples were kept in the bath until the dielectric layers were fully removed as judged by the lack of wetting of the HF solution on the Si surface. All of the dielectrics used are polar, and thus form polar bonds with water and HF. This means these liquids will readily coat the dielectrics, a process referred to as wetting. By contrast, silicon is non-polar, producing a highly hydrophobic surface so no wetting will occur. This difference can be used to identify if a dielectric has been fully removed, as only then will wetting be prevented. This process is hereafter referred to as an HF dip.

2.1.2 Wafer cleaning

In this work wafers were annealed at elevated temperatures and so any surface contaminants could easily diffuse into the wafers degrading their electrical properties. It was therefore

important to clean the surfaces comprehensively. The cleaning of wafers is split into two processes, both of which are carried out in the departmental cleanroom.

The first process was a preliminary clean used to remove visible contaminants such as sawing dust, blade coolants as well as any other bulk contaminants. These were removed in a dedicated process, to avoid excessive contamination of more expensive cleaning chemicals and equipment. In this process, samples were placed onto a sheet of lint free cleanroom tissue. A second sheet was saturated with acetone and used to wipe the topside of the sample until visibly clean. The wafer was then flipped and the other side cleaned with a fresh tissue.

The second, more important cleaning process is a Radio Corporation of America clean (RCA). This is commonly used by the integrated circuit and solar industries to comprehensively clean silicon wafers. Two RCA cleaning solutions are normally used: the RCA 1 is a mixture of hydrogen peroxide, ammonia and de-ionised water (DI) in a ratio of 1:1:5; while the RCA 2 contains hydrogen peroxide, hydrochloric acid and DI water in a ratio of 1:1:5. These were prepared in-house as required using VLSI (electronic) grade chemicals supplied by Chestech and DI water produced in-house. The RCA solutions were held at 60 ^{o}C through the use of a water bath. In this work the samples were loaded into a quartz holder to enable multiple wafers to be cleaned simultaneously. They were then given an HF dip, and rinsed with de-ionised (DI) water (resistivity 18MΩcm). The samples were then immersed in 60 ^{o}C RCA 1 solution for fifteen minutes, given a one minute HF dip and rinsed in DI water again. This process was then carried out a second time using the RCA 2 solution. All wafer handling used clean plastic tweezers, and after processing the samples were transferred to a fresh, clean sheet of cleanroom paper and were covered to prevent re-contamination. This cleaning methodology is represented in Figure 17.



Figure 17. The standard RCA procedure used in this work

2.1.3 Cleaning quartz ware

It was important to ensure that wafers were not re-contaminated during high temperature processing, so the quartz furnace tubes were also cleaned before annealing. This cleaning procedure differed to that used for wafer cleaning, due to the size of the tubes which necessitated the use of larger volumes of chemicals. This made it prohibitively dangerous for the author to use HF in the cleaning processes. Work with a masters student, Phi Macdonald[54], showed that an RCA 1 clean was sufficient to prevent contamination of wafers during high temperature processing. The RCA solution was heated before it was transferred into a plastic tube. The quartz tubes were then inserted and held there for fifteen minutes, before they were rotated rinsed and re-inserted to allow the other end to clean, after which the tube was rinsed and dried.

A series of quartz disks were used as spacers during annealing and so were also cleaned. These were cleaned in RCA 1 and 2 but were not dipped in HF.

2.1.4 TMAH etching

Etching of silicon was carried out using TryMethylAmmoniumHydrate (TMAH) solutions, which are regularly used to texture wafer surfaces[25]. As this is not able to etch dielectric layers the samples were given an HF dip prior to etching. The samples were then transferred into the pre-heated TMAH solution (~60 ^{o}C). They were then etched for 45 minutes to remove saw damaged layers, work by a master student showed that this removed 20 μm per side[54], or for 10 minutes to remove a phosphorous doped layer.

2.1.5 Phosphorous diffusion

Emitters were made by coating samples with a dopant rich spin on glass followed by annealing.

The samples were first stripped of any dielectric coatings as these might otherwise have limited phosphorous diffusion into the silicon. The samples were then given a full RCA clean, terminating in an HF dip. Simultaneously, a spinner chuck was prepared as follows: Firstly, a double sided tape was applied to the chuck, and then a layer of "loadpoint mounting tape" was placed such that its adhesive side would attach to the silicon samples. This tape is a weakly adhesive, residue free, film which secures samples during wafer spinning. This film enables the samples to be easily removed after spinning without the risk of contamination.

The cleaned samples were then placed upon the prepared chuck. Approximately 2 ml of phosphorous rich, spin on dopant (SOG) (P509, supplied by filmtronics) was applied to the surface. This is represented in Figure 18. The chuck was then spun at 3000 rpm for 20 seconds to allow the dopant film to spread evenly across the samples. They were then removed from the chuck, placed on a clean dummy wafer and baked at 200 ^{o}C for 2 minutes to drive off the solvent. The samples were then transferred to the furnace tube and annealed for 30 minutes at 950 ^{o}C before being cooled to 850 ^{o}C and annealed for a further 30 minutes. This two stage annealing process enhances impurity gettering as explained in chapter 4. This process produced n-type surface regions with sheet resistances of 250 Ωsq $\pm$10 %.

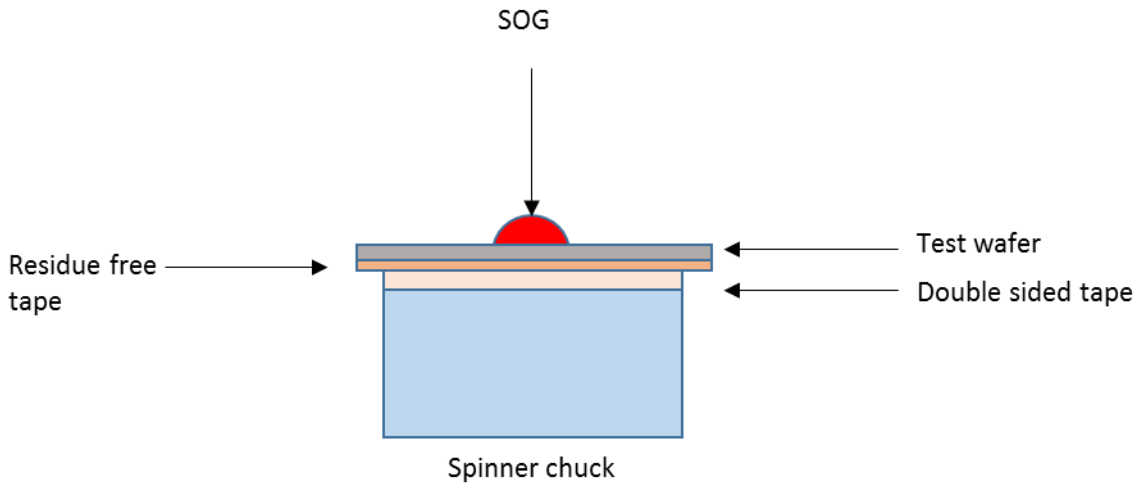


Figure 18. Loaded spinner chuck prior to wafer spinning.

2.2 Dry processing

In this work "dry processing" refers to any process where all of the materials used are either solids or gases.

2.2.1 Thermal evaporation

Thin layers of aluminium were deposited on to substrates using thermal evaporation. This was carried out in a Eurocoater thermal evaporator. A tungsten filament was wrapped in aluminium wire and placed between two thick copper electrodes. The process chamber was then pumped to vacuum, $\sim 2 \times 10^{-6}$ mbarr, and a current supplying 300 W of power was passed through the filament inducing heating. This caused the aluminium to evaporate. The vaporised aluminium then passed through the chamber until it met a cold surface, eg the non-heated sample, where it condensed to form a layer of aluminium, see Figure 19.

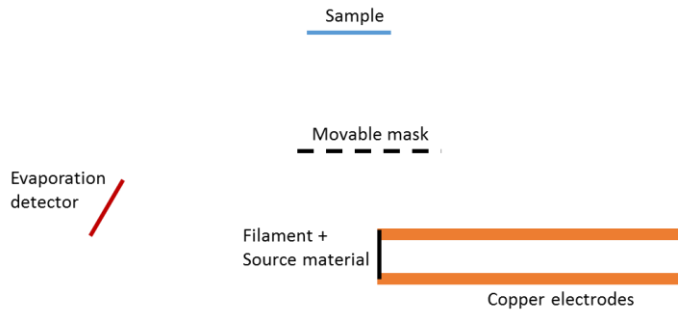


Figure 19. A schematic of the thermal evaporator

The thermal evaporator has a movable shutter which can be placed between the source and target at the start of the process. This ensures that the first material to deposit, including the aluminium oxide and surface contaminants deposit onto the shutter not the samples.

2.2.2 Plasma Enhanced Chemical Vapour Deposition

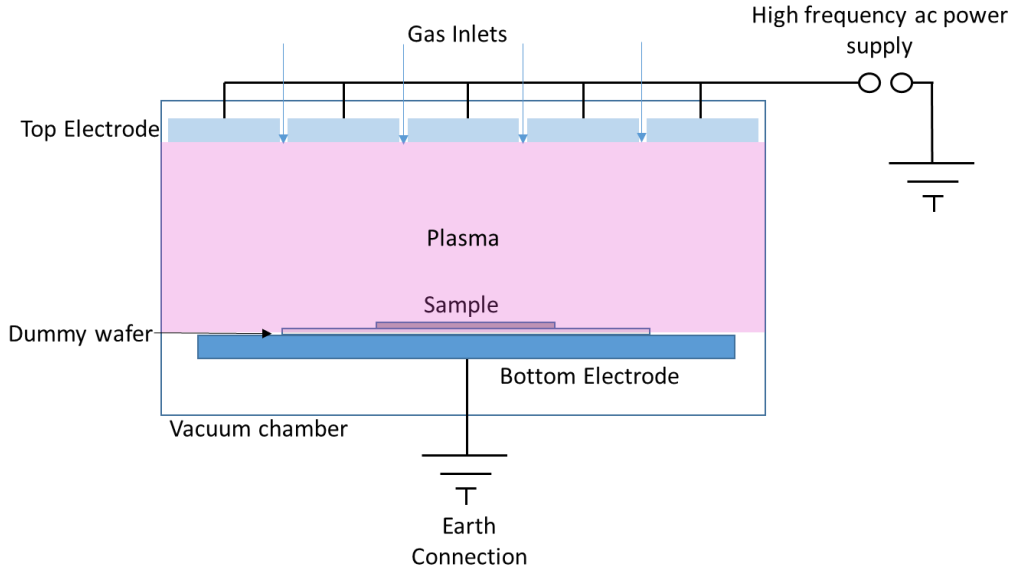


Figure 20. A schematic of a conventional PECVD. Used in this work as both a plasma source and to deposit dielectric layers. The power required to produce the plasma was generated through the application of a 13.6 MHz, a.c. voltage to the top electrode.

Plasma Enhanced Chemical Vapour Deposition (PECVD) is used to deposit dielectric films onto the surfaces of silicon wafers [55]. In this work it was used to deposit hydrogen rich silicon nitride (H:Si_xN) layers, to passivate otherwise bare silicon surfaces. These depositions were carried out in a parallel plate PECVD system supplied by Oxford Instruments (PlasmaLab 80+), see Figure 20. Before insertion into the PECVD chamber the samples were HF dipped, rinsed and dried to remove any dielectric layers. The samples were then placed onto dummy wafers within the PECVD chamber, which was subsequently pumped to vacuum. Once at low pressure the feed gases were let into the chamber, and power supplied to the gas from the two electrodes creating a plasma. The variables for this deposition process are detailed in Table 3. This resulted in the deposition of a 70 nm thick silicon nitride film. 200 µm thick, 1Ωcm, p-type, single crystal samples coated in this manner achieved lifetimes in excess of 100 µs, so it is believed that this is an effective passivation layer.

Process duration (seconds)	240
Process pressure (mTorr)	650
Power (watts)	20
Ammonia flow rate (sccm)	20
Silane flow rate (sccm)	400
Nitrogen flow rate (sccm)	600

Table 3 The chamber conditions for the deposition of a 70 nm thick PECVD silicon nitride layer.

2.2.3 Corona discharge

Corona discharge is used to supply extrinsic charge to sample surfaces, to induce field effect passivation. In this process, atmospheric gasses are ionised and transported to the sample surfaces. Molecules in the air are ionised in regions of high electrical field strength. In corona discharge these fields are supplied by applying a high potential to a sharp needle. The field strength is very high at the tip, and so this is where ions are generated. The ions then move away from the tip and deposit onto the sample. Work by Bonilla et al [56] showed that the current uniformity can be increased by having a large gap between the needle and the sample. This is important because increasing corona charging reduces the surface recombination rate. However, if excess corona charge is supplied, the field it generates across the dielectric can cause electrical breakdown, damaging the surfaces. It is therefore important to avoid applying excess charge to any part of the surfaces if the full benefit of corona charging can be realised without any side effects.

In this work, optimal positive charge was supplied by applying increasing amounts of charge, and measuring the lifetime after each subsequent application. When a plateau was reached, and minimal lifetime improvements were achieved from further charge application, the process was stopped.

Due to the high voltages involved, safety measures are very important. All of the high voltage wires were insulated. However, the needle could not be. Instead it was contained within the

earthed cage seen in Figure 21. The door to the cage was interlocked so that if it was opened the high voltage supply would turn off.

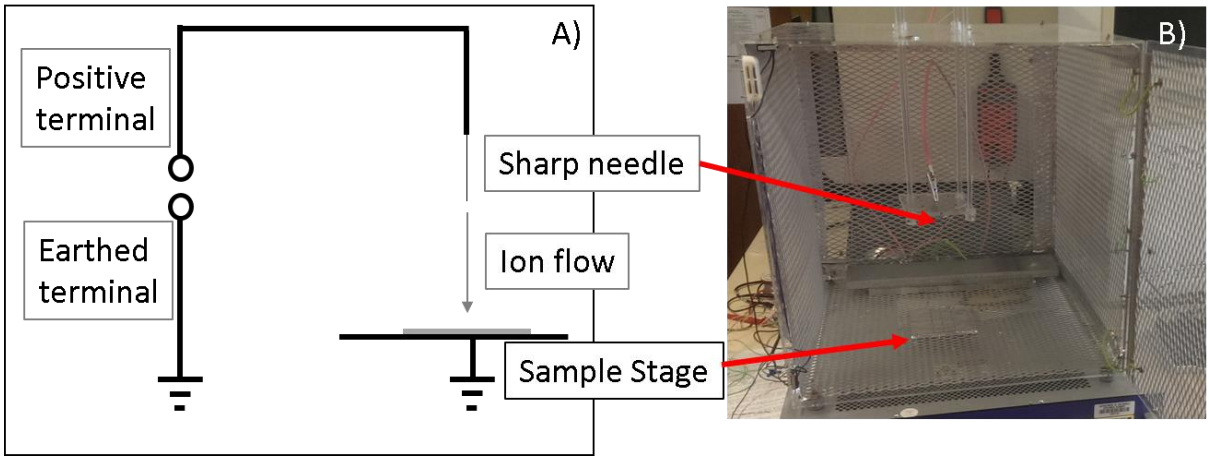


Figure 21 A). A schematic of the corona discharge process. B). An image of the corona discharge equipment used in this work.

2.3 Anneals

The furnace facilities and associated equipment were modified during the course of this project to ensure that the samples could be processed in a sufficiently clean environment for reproducible results to be obtained. Further modifications were made to ensure the atmospheric conditions within the furnace could meet the experimental requirements. The work done to upgrade these furnaces is discussed in section 2.5. This section only discusses the final furnace arrangement used.

2.3.1 Furnace use

Although multiple furnaces were used in this work only one generated results which are presented in this work. This furnace was a, 4 cm inner diameter, tube furnace supplied by Lenton Furnaces with a hot zone approximately 6 cm long, see Figure 22. The maximum temperature of this furnace was 1200 ^{o}C. It has an alumina tube protecting the heating elements, and an inner quartz tube where the samples are placed. This quartz tube can be moved within the furnace such that the samples are moved into, or away from the hot zone as required, allowing rapid sample heating and cooling. However, if controlled wafer cooling was

required, the cooling rate was less rapid. The maximum cooling rate can be seen in Figure 23 below.

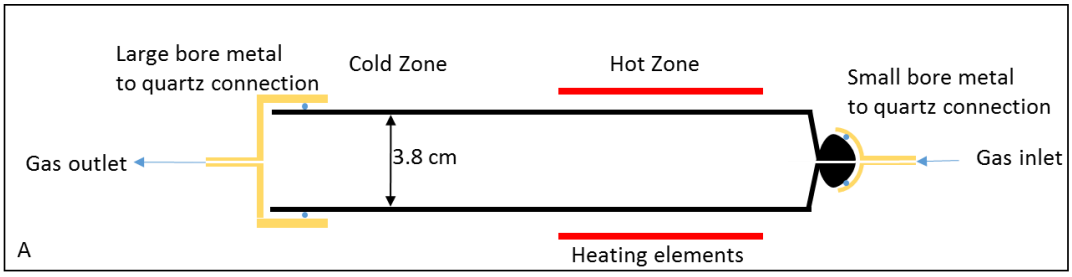


Figure 22. A schematic of the furnace used in this work, it should be noted that the furnace tube, and all the gas fitting can be moved relative to the thermal zones. The samples can be placed in the cold zone while the atmosphere is adjusted, and then moved into the hot zone as required.

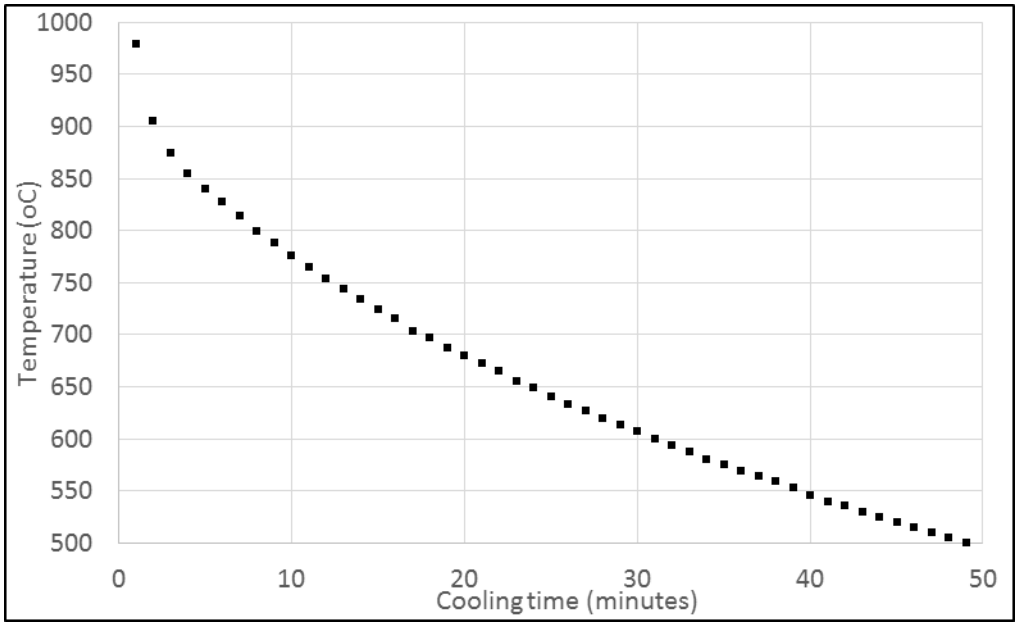


Figure 23. The maximum possible controlled cooling rate when cooling from 980 ^{0}C, it may be possible to cool faster at a given temperature if the prior cool was slower, as the bulk of the furnace would therefore be cooler.

Controlling the atmosphere within the furnace tubes was of great importance for this work. The gases could be fed into the furnace tube while the samples were located within a cold zone, so the samples were only exposed to the desired atmospheres when at elevated temperatures. Up to 4000 sccm, of oxygen, nitrogen and argon and 100 sccm of chlorine could be supplied to the furnace. The furnace dimensions were; inner diameter 4 cm, length 100 cm. This meant that a

gaseous volume equal to the furnace tube volume could be supplied in 6 seconds, so the furnace atmosphere could be rapidly changed. Due to the small diameter of these tubes a wafer holder could not be used, consequently the wafers were arranged into stacks before their insertion into the furnace to increase the number of wafers which could be processed simultaneously, see Figure 24. When required, the quartz furnace tubes could be removed from the furnace and cleaned, as described above. Thermal calibration of the furnace indicated that thermal variation across the hot zone was small (<10 ^{o}C) so any samples placed within it experienced comparable temperatures so could be used as controls for the other wafers, this was important for saw damage gettering work, see Figure 25.

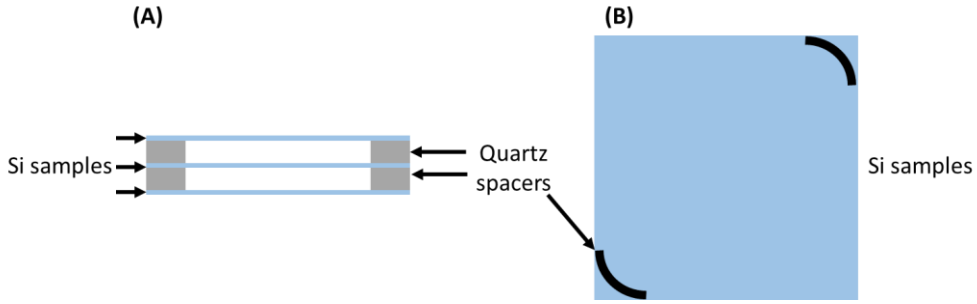


Figure 24. Schematics of the arrangement of wafers in stacks. (A) A side view, and (B) the view from above before another wafer is placed onto the quartz spacers.

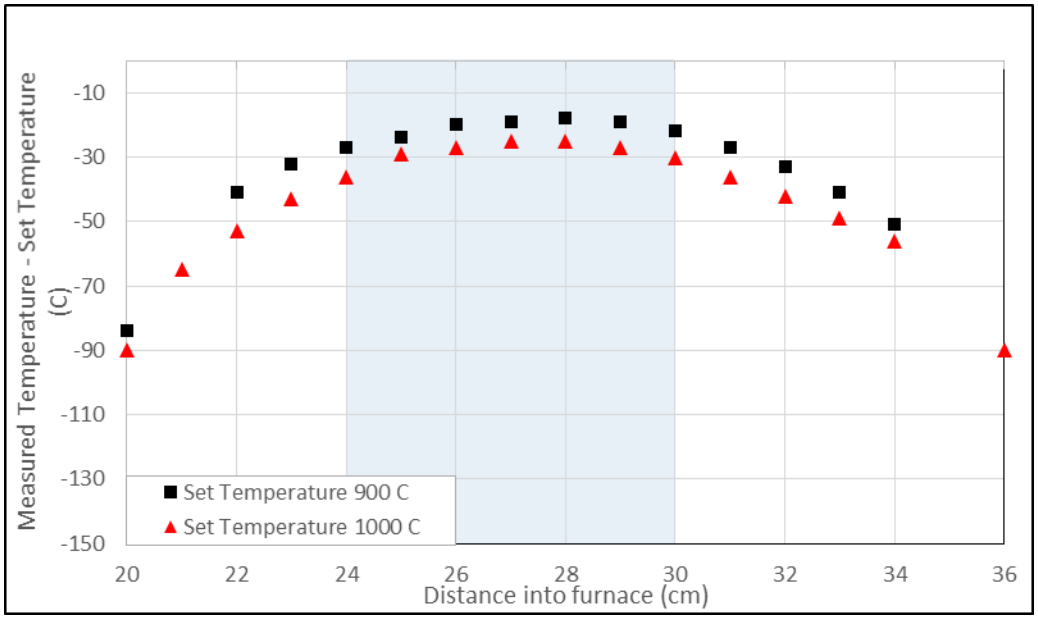


Figure 25. Thermal calibration data. Temperatures within the hot zone (shaded blue) vary by less than 10 °C which is minimal relative to the temperatures used in this work.

2.4 Characterisation techniques

A number of characterisation techniques have been used in this work. They are explained below.

2.4.1 Sinton photo-conductance lifetime tester

The Sinton photo-conductance lifetime tester (Sinton WC-120 lifetime tester) accurately measures sheet resistance within a sample and uses this information to calculate both minority carrier densities and lifetimes. The lifetime tester, has a coil which sits directly underneath the sample. An alternating current is passed through the coil, which generates a fluctuating magnetic field which passes through the sample. This field induces eddy currents within the sample. These currents generate magnetic fields which affect the current flowing through the coil, via mutual inductance[57]. Changes to the sheet resistance of the sample will therefore affect the current flowing through the coil. This effect can be interpreted to find the sheet resistance of the samples. In addition, the relationship between the number, and types, of free carriers and sheet resistance is well known. Therefore, the measured sheet resistance values can be used to calculate the concentration of free carriers. Multiple measurements are rapidly

taken, allowing the change in sheet resistance, and thus concentration of carriers, can be found as a function of time after the illumination.

When making a lifetime measurement using the Sinton lifetime instrument, intense illumination is applied to the wafer to generate excess minority carriers. The resultant concentration of excess minority carriers can be used to calculate the sample lifetime. There are two operating modes for this lifetime tester, and they each calculate the lifetime in a slightly different way. The first is referred to as quasi steady state photoconductance (QSSPC) [58]. In this technique, it is assumed that the carrier concentration is effectively at a steady state, as carriers are annihilated by recombination processes at the same rate that additional carriers are generated by the illumination applied to the sample. For this assumption to be valid the illumination pulse must be long relative to the sample lifetime. Consequently any changes to the generation rate, resulting from changing illumination intensity, takes place over multiple carrier lifetimes, and the carrier concentration can reach the new equilibrium state. This technique is typically used when the sample lifetime is <200 μs. When this is true:

2.4.1 $$\boldsymbol{G_{en} = \tau \times \Delta n}$$

Where G_{en} is the generation rate, τ is the effective lifetime and Δn is the excess minority carrier density, also referred to as the injection level.

In this technique the illumination is supplied in the form of a slowly decaying flash of light, the intensity of which is measured by a separate photodetector. Minority carriers are injected into the silicon at a rate proportional to the illumination intensity. If the reflectivity of the sample is known, the number of photons entering the sample, and thus the generation rate, can also be calculated. In addition, the excess minority carrier density can be found from sheet resistance measurements. Therefore, equation 2.4.1 can then be solved to find the sample lifetime as a function of the injection level.

When the sample lifetime is high (>100 μs), a second mode of operation called transient photoconductance can be used. In this mode it is assumed that injection only occurs at the start

of the measurement. Therefore the minority carrier density will fall as carriers recombine. The rate at which this recombination occurs enables the lifetime to be calculated using equation 2.4.2:

2.4.2 $$\frac{d\Delta n}{dt} = \tau \times \Delta n$$

In this technique it is assumed that the sample lifetime is long compared to the flash length. For this to be valid the sample lifetime must be high, and the flash used must decay rapidly, the flash used had a duration of 0.016 s.

Minority carrier lifetimes vary as a function of injection level, and in this work lifetime values are quoted at an injection level of 1×10^{15} cm^{-3} unless otherwise stated.

Lifetime measurements can also be used to measure the concentration of interstitial iron within boron doped wafers. When a wafer is left in the dark at room temperature for approximately one day, the overwhelming majority of interstitial iron atoms will pair with boron, forming an iron boron pair. However, when the wafer is exposed to intense illumination these pairs will split, releasing the interstitial iron, furthermore, this breaking of the FeB pair is the only significant effect of this illumination. The recombination parameters of the two different states of iron are significantly different and so if the lifetime of a wafer is made after it has been stored in the dark, and it is then re-measured after intense illumination, the change in lifetime can be used to identify the concentration of iron which is free to enter interstitial or paired states [37] [59].

2.4.2 Photoluminescence decay

Photoluminescence decay (PL) is a spatially resolved lifetime measurement technique, which in this work is used qualitatively. In PL, minority carriers are generated through illumination of a small region of the silicon. The minority carriers will then recombine, and a fraction of these recombination reactions will be radiative. These emitted photons are measured as the PL signal:

2.4.3 $$\phi_{PL}(t) = B \int_0^d \Delta n(t,x) dx$$

Where $\phi_{PL}(t)$ is the time dependent PL signal intensity, B is an adjustment constant, d is the sample thickness and $\Delta n(t,x)$ is the excess concentration of minority carriers. This assumes that the wafer does not absorb the generated carriers[60]. If the wafer has a low lifetime $\Delta n(t,x)$ will decay rapidly so the PL signal will also fall rapidly. This can be used to enable PL to probe wafer lifetime. If the illuminated region is rastered over the wafer the lifetime can be found as a function of position. In this work, the PL measurements were conducted by REC solar.

2.4.3 Kelvin probe

Kelvin probe is a technique which can be used to measure the surface potential between the surface of a conducting sample and a vibrating probe tip[61]. This can thus be used to investigate the charge density on the surface of the dielectric layer on a silicon sample. In this work the Kelvin probe was conducted on a system made by Sebastian Bonilla. For a more comprehensive review of the technique see [62] and for the full experimental set up, and comprehensive review of the technique as it applies to dielectric on silicon systems please see[63].

2.5 Furnace design

A significant fraction of the work in this thesis required the use of a furnace to increase the solubilities and diffusivities of impurities within silicon wafers such that the impurities could be moved to less deleterious locations. For these experiments to be effective the furnace had to meet a number of criteria. It had to be able to heat wafers which were at least 3 x 3 cm^2, to temperatures of at least 1000 ^oC. The wafers also had to be heated to and from these temperatures very quickly (<1 minute). Additionally, the concentration of impurities within the furnace had to be sufficiently low that it would not contaminate the wafers being processed. This extrinsic contamination would reduce the purity of the wafers, degrade their lifetime, and conceal the benefits offered by the experimental process. For one section of this work it was important that oxygen could be excluded from the furnace such that oxidation could not occur at the annealing temperatures. In addition, chlorine was to be present in the oxygen free

atmosphere, so it was important that the furnace was able to process this dangerous gas safely. Initially, no furnace which met all of these criterion was available, and so work to modify, and upgrade the existing furnaces had to be carried out. In this section I will discuss the work in the context of setting up a furnace for the use of chlorine as this was the hardest to design, and would be mutually compatible for all other work.

2.5.1 Initially available furnace design

At the start of this work a Lenton furnace was present, this had a quartz tube, with an inner diameter of 24 cm, and a total length of 200 cm. The wafers could be moved within this furnace, which included a cold zone, so rapid temperature changes were trivial. The upstream end of the furnace was a spherical quartz/ metal fitting, and the downstream end opened into an extracted chamber. This chamber was held at negative pressure relative to the rest of the cleanroom to ensure the chlorine would not escape. The gas flow rates into this chamber were 100 sccm of both nitrogen, and a 5 % chlorine/argon mix.

Although this system was safe for chlorine use it was otherwise inappropriate for a number of reasons. Extensive oxygen incorporation was unavoidable and the furnace had become contaminated with deleterious impurities prior to the start of this project. Due to the large dimensions of the furnace, the author was unable to clean the furnace as wet chemical cleaning was prohibitively dangerous. A number of modifications were made to upgrade this system.

2.5.1.1 Atmospheric isolation

The furnace which was initially available had a ~450 cm^2 opening into a gas chamber. For safety reasons, this chamber was held at negative pressure relative to the cleanroom which it was situated within. Therefore this gas chamber contained gases, including oxygen from the cleanroom. Due to the large furnace opening, and low flow rates the net exhaust gas flow rate was very low (~0.5 cm $minute^{-1}$). Consequently, it was possible for gases to diffuse from the gas chamber into the furnace faster than they were removed by the gas flow. One method used to overcome this was to build a door to reduce the furnace opening. This was made from stainless steel, rubber sealants, which also protected the quartz furnace tube, and a mechanical support

structure. This door dramatically increased the exhaust gas flow rate, but alone did not enable sufficient oxygen removal as annealing at 1000 °C for half an hour still resulted in the growth of a visible silicon dioxide layer.

2.5.1.2 Gas flow rates

Initially the furnace was designed to pass <200 sccm of gas. From the volume of the furnace and these flow rates, it can be calculated that it took ~75 minutes for the supplied gas to have the same volume as the furnace. Due to gas mixing, this exchange had to be carried out multiple times before the atmosphere was fully converted, the exact number depends on a number of factors not considered in this work. Consequently, very long purges (lasting multiple days) were required to fully convert the furnace atmosphere, making this process prohibitively slow. In addition the samples had to have been loaded into the furnace before this purge could be started and during the extensive purge, deleterious room temperature oxides could have formed [64].

The gas lines were modified such that higher flow rates could be used, and thus the purge times could be reduced to acceptable levels. As part of this work, new nitrogen dewars and inert gas flow meters were installed. These enabled 4000 sccm of nitrogen to be passed constantly, and an additional 4000 sccm of argon to be passed if required. These increased flow rates of inert gases meant the concentration of chlorine in the furnace would have been reduced (from 2.5%, to 0.1% when using the full nitrogen gas supply), so the chlorine bottle was changed from a mix of ten percent chlorine in argon, to pure chlorine. After these modifications, the discoloration due to the growth of a silicon dioxide layer was significantly reduced, but was still observable after annealing at 1000 °C for half an hour. It was not clear if the oxide growth would be sufficiently slow to allow the intended process, chlorine gettering, to be successfully enacted.

2.5.1.3 Furnace cleaning

After these modifications, it was found that the furnace tube was contaminated. This was confirmed by using a high quality single crystal silicon wafer. This initially had a high lifetime (>100 μs), but this degraded (<1 μs) after annealing at 1000 °C for half an hour. As discussed,

wet chemical cleaning of the furnace tube was not possible. Therefore gas phase cleaning was attempted. The furnace was held at 1000 ^{o}C and the atmosphere was cycled between oxygen and chlorine. It was hoped that the former would react with and remove any organic contaminants and the latter would react with any metallic contaminates, see chapter 5 for details of reactions between metallic elements and chlorine. This gas phase cleaning was unsuccessful, and no significant change in the final lifetime was observed.

2.5.2 Smaller volume furnace

The large furnace was replaced by a smaller volume Lenton furnace, capable of heating samples to 1200 ^{o}C, see section 2.3.1 for further details. The reduced volume associated with this new furnace meant that one gas exchange could be completed in ~ 6 seconds when using the full nitrogen flow rate, this meant that it was easier to control the atmosphere within this furnace than within the larger diameter furnace discussed above. Additionally, the furnace tubes could be cleaned through wet chemistry as discussed in section 2.1.3. However, this furnace was not originally designed for chlorine usage, so a number of modifications were made. These enabled the atmosphere in this furnace to be controlled and enabled the safe use of chlorine.

2.5.3 Chlorine safety concerns

Chlorine is a highly dangerous chemical, and must be used carefully. It is capable of causing severe respiratory and eye damage, and the former can lead to death. The recommended exposure limit is only 0.5ppm [65], so clearly even minor leaks are a significant concern. This meant the furnace system had be carefully designed to ensure users were not exposed to chlorine.

2.5.3.1 Leak detection

One of the most important factors required for the safe operation of a hazardous gas is that a leak must be detectable before the concentration reaches hazardous levels. Fortunately, people are able to detect chlorine at very low concentrations, with minor irritation of the nose and eyes occurring at concentrations as low as 0.05ppm [66]. Unlike a number of chemicals, such as hydrogen sulphide, this detection is not lost after prolonged exposure. Therefore if a person is

present at the site of a potential leak they should be able to take corrective action before the leak becomes dangerous. This was one of the important control measures which was used in this work, and as such it was mandated that one user would be present at the chlorine bottle, and one at the site of the furnace whenever chlorine processing was occurring.

2.5.3.2 Leak avoidance

It was important to ensure that the gas system was designed in such a manner that chlorine would not leak. A number of designs were proposed to the safety office before an acceptable design was chosen. This design included storing the chlorine bottle in an extracted cupboard into which a moistened piece of litmus paper could be lowered. This would enable a leak to be detected before the cupboard was opened. After chlorine passed through the flowmeters, the gases were mixed before being passed into flexible hosing. This ended in a cup which fitted onto a spherical fitting at the end of the quartz furnace tube, this is a standard fitting. The downstream side of the tube did not have any fittings. Instead a compression fitting with PTFE ferules was attached to the outside of the tube. This was then attached to a second flexible hose which fed into the gas extraction system. This system prevented any chlorine release.

3 Introduction to Gettering

This chapter will introduce the concept of gettering, a process used to limit the detrimental impact of impurities in solar cells. It will also introduce a range of industrially important gettering processes and will detail some of their advantages as well as limitations.

3.1 Introduction

Gettering is a process where impurities within a silicon wafer are redistributed such that they are less detrimental to the wafer's lifetime. Impurities can either be removed from the wafer entirely (external gettering) or can be moved to locations where they have less of an impact upon the lifetime (internal gettering). Due to the costs associated with preventing contamination, most solar grade silicon wafers contain transition metal impurities. As discussed in section 1.3.2 this reduces their lifetime, and thus the efficiency of solar cells. As gettering reduces the impact of these impurities it allows lower cost, less pure silicon to be used without reducing the final efficiency. Gettering is therefore required to enable solar cells to be made from conventional mc-Si and is part of conventional cell manufacturing processes[67] [68]. As such, it is a highly important industrial process. This is reflected in the large amount of research carried out into this field [69]–[74]. As a result a number of gettering techniques have been developed, they all have a number of similarities as discussed below.

3.2 Gettering Fundamentals

Any gettering process requires a high temperature annealing step. This provides energy to the impurities, and thus enables them to both enter into solution within the wafer and to diffuse within the silicon. They will remain in solution until they reach a preferential location referred to in this work as a "gettering centre". When impurities reach this location they become trapped and so leave the solution. When the impurities are located in these gettering centres they should be less detrimental to the wafer than they were in their initial location.

It should be noted that there are two types of locations (impurity traps) which can capture impurities. In this work these locations are referred to as gettering centres, which reduce the electrical activity of the impurities when they capture impurities and impurity sinks which do not reduce the electrical activity of the defects.

3.3 Simplified gettering

In the simplest possible model, there is only one type of gettering site, and all of the impurities are initially in solution. Impurities adjacent to the gettering centre are captured by it, reducing the local impurity concentration. This sets up a concentration gradient between the bulk of the wafer and the gettering centre, so impurities diffuse to the latter. This will continue until an equilibrium condition is reached. The equilibrium position is determined by the temperature, and the binding energy between the impurity and the gettering centre.

3.3.1 Gettering centres

A gettering centre must have two important attributes. Firstly, the recombination activity of the wafer must be reduced when impurities are located at the gettering centre. Otherwise impurity capture would be deleterious, which is referred to as impurity trapping for the remainder of this work, to distinguish it from gettering. Gettering centres reduce the recombination activity of impurities in a number of different ways.

Secondly, the gettering centre must bind to impurities such that they are captured and the concentration of impurities in the bulk of the wafer is reduced. For this to be possible, the energy associated with the impurity must be reduced when bound to the gettering centre. The mechanism by which this interaction occurs is different for different gettering processes. The impurity energy loss upon gettering is hereafter referred to as the binding energy. According to Boltzmann statistics the concentration of impurities located at any given impurity sink, divided by the concentration in solution in the silicon will be:

3.3.1

$$\frac{[X]_{is}}{[X]_{bulk}} \propto \boldsymbol{exp}\left(\frac{-Ea}{kT}\right)$$

Where $[X]_{is}$ and $[X]_{bulk}$ are the concentrations of impurities in the impurity sink and in solution in the bulk of the wafer, respectively. Ea is the binding energy between the gettering centre and the impurity, a negative value means energy is released when the impurity is located at the gettering centre. It is possible for Ea to change with temperature, particularly if the gettering process is a reaction between chemical species, see Chapter 5. Equation 3.3.1 assumes that the impurities are in their equilibrium positions and concentrations, and thus highlights the thermodynamic limitations of a given gettering process. If the equilibrium position is not reached, it is assumed that impurity capture is rapid, and it is assumed that the gettering rate is only limited by long range diffusion, then equation 3.3.1 can also be used to determine the impurity concentration adjacent to the gettering centre during gettering see Figure 26.

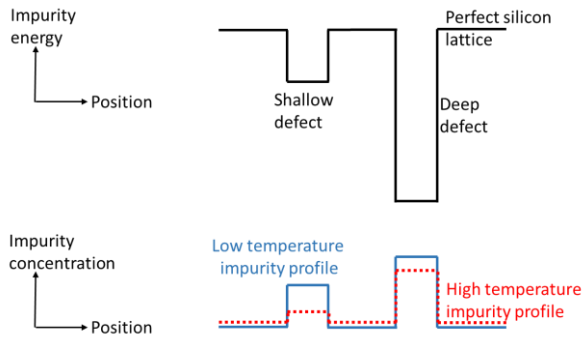


Figure 26. A schematic showing the differing gettering efficacies of different impurity sinks, the deeper sink is much more effective than the shallow sink at high temperatures. However, neither trap is as effective at higher temperatures, as evidenced by the increased concentration of impurities in the bulk in the high temperature profile

Equation 3.3.1 highlights some important features of impurity capture. Firstly, impurities will be more populous in locations of lower energies, where energy is released upon the capture of impurities, as seen in the deep defects in Figure 26. Therefore a gettering centre must be a site which lowers the impurity energies, or it will be unable to capture impurities, and more effective gettering centres are likely to lower the impurity energies more than less effective gettering centres. Secondly, equation 3.3.1 shows that at lower temperatures, gettering centres become more effective at trapping impurities than at higher temperatures. As such, gettering is more thermodynamically favourable at lower temperatures, see Figure 26.

There is one final factor which determines the thermodynamic limitations of a given gettering centre, which is not detailed in equation 3.3.1. This is the quantity of impurities which can be gettered by the centre. This is not a limiting factor for some sinks such as precipitates which can grow to capture further impurities. However, it may be limiting if the gettering centre can become full. For example, it is hypothesised that point defects may be localised to some parts of the wafer, and they bind with impurities to trap them. If so, the quantity of gettered impurities could not exceed the number of point defects in these locations.

3.3.2 Competitive gettering

It is probable that there will be multiple different potential impurity traps within a wafer, particularly if it is made from highly defected mc-Si. Impurities will thus be distributed across all of these potential sinks, as well as within the bulk of the wafer. Impurities located at these different locations will have different levels of electrical activity. As such, the wafer lifetime will vary considerably depending on which impurity traps contain impurities and in what concentrations. For example iron is less electrically, and recombination active when located within a small number of large precipitates. However, it is much more active when located at bulk dislocations which become effective recombination centres when decorated by impurities. It is therefore important to control which impurity traps become populated during a gettering process.

The concentration of impurities in the different sinks is affected by a number of factors. Firstly, the thermodynamics of the system, higher concentrations are expected at sites with larger binding energies as demonstrated by equation 3.3.2.

3.3.2
$$\frac{[X]_1}{[X]_2} = \boldsymbol{exp}\left(\frac{-(E_{a1}-E_{a2})}{kT}\right)$$

where $[X_n]$ is the concentration of impurity X at trap n, E_{an} is the binding energy between the impurity and the trap n, k is Boltzman's constant, and T is the absolute temperature.

The impurity distribution within real wafers is unlikely to follow the distribution indicated by equation 3.3.2. This is due to kinetic limitations which prevent the system from reaching this

ideal distribution. These limitations include, the diffusive flux of impurities within the wafer, and the capture of impurities by the impurity traps. The flux is affected by both diffusivity and concentration gradient. The former is simply temperature dependent, while the latter is more complicated.

The impurity gradient arising from a system with two or more gettering centres is highly dependent on the binding energies associated with each sink. Systems containing multiple impurities will be explained here using a model system where one sink which initially contains a high quantity of impurities (e.g. an as-cast precipitate), one initially empty sink (e.g. a phosphorous rich emitter region), and an initially moderate concentration of impurities in solution. Figure 27 illustrates the gettering process, with A schematically demonstrating the initial impurity profile, B showing the energy levels associated with impurities in different locations within the wafer, and C to F showing how the impurity profile changes as the gettering process proceeds. At the start of the gettering process two things will occur. The precipitate will release impurities and the gettering sink will capture impurities. Both of these processes will generate local equilibrium conditions between impurities trapped in solution and impurities located in the sinks, see Figure 27 D). This results in the formation of concentration gradients in the bulk of the wafer such that impurities diffuse from the precipitates to the gettering centre, see Figure 27 E). As the gettering centre becomes populated with impurities the equilibrium concentration in the adjacent silicon also increases, from equation 3.3.2. This means the concentration gradient between the two sinks falls. Eventually, a true equilibrium situation is reached where the concentrations of impurities in the two sinks and the solution are determined by equations 3.3.1 and 3.3.2, see Figure 27 F). As the precipitate can release impurities after the start of the gettering process, the time required for gettering may be much longer than suggested by a diffusion model which assumes a starting concentration, a fixed impurity concentration at the gettering centre and no source of impurities.

It can be seen that the concentration gradients are highest, and the re-distribution process is accelerated when the local equilibrium concentration of impurities next to the precipitates are high. This is favoured at high temperatures. However, if the temperature is high the gettering centre will capture impurities less effectively so the final equilibrium condition will leave more impurities in solution. Maximising gettering efficacy requires balancing these two effects.

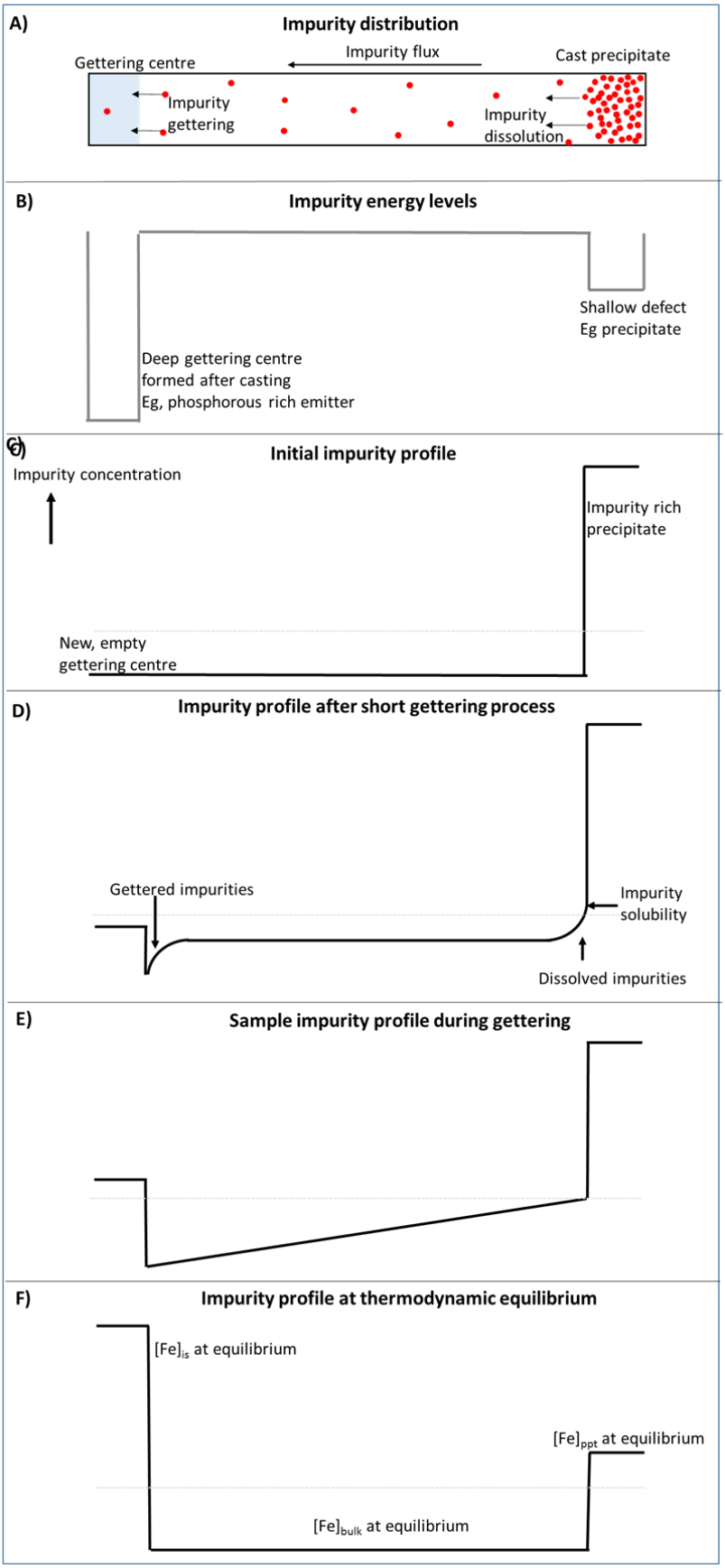


Figure 27. A schematic of gettering from one impurity sink to another.

3.3.3 Important gettering parameters

Previous sections have discussed the kinetic and thermodynamic factors involved in gettering impurities to multiple different impurity sinks. A few conclusions about the ideal gettering conditions can be drawn. Firstly, it is important that the gettering process lasts long enough at high temperatures to enable extensive diffusion of impurities to the gettering centres. Secondly, the binding energy associated with the gettering site determines the maximum temperature which still enables effective gettering. This is important as a higher temperature enables faster diffusion and more complete release of impurities from sinks. Thus a gettering centre with a large binding energy is very useful. Thirdly, the preferred gettering centres should be "large" meaning they are able to capture a large number of impurities with minimal change in the concentration of impurities at the gettering centre. This means they can capture a larger number of impurities for a given binding energy. Finally, if gettering to a specific centre is desired, it is important to remove competing sinks where possible.

3.4 Gettering techniques

A number of different gettering techniques have been developed by other people and reported in the literature. In the next section their mechanisms, benefits and limitations will be discussed. This work will discuss the gettering processes which are relevant to the solar industry, although it should be noted that additional gettering techniques exist for other industries such as the integrated circuit industry (IC).

3.4.1 Phosphorous diffusion gettering

Processing a p-type wafer into a solar cell typically requires the formation of a phosphorous rich, n-type emitter layer. This is created by the diffusion of phosphorous from a phosphosilicate glass (PSG) located on the silicon's surface. The phosphorous in-diffusion creates a n-type region at the surface of the cell, and when this is located within a p-type wafer, the pn junction required to separate charge carriers is also formed. It simultaneously getters impurities such that bulk impurity concentration is reduced by orders of magnitude[75], a process called phosphorous diffusion gettering (PDG). In PDG the impurities are gettered into the emitter region. This reduces net recombination in three ways. Firstly, it re-locates the

impurities into the n-doped emitter. Most transition metals are more recombination active in p-type material than in n-type[76]. Therefore this re-distribution lowers net recombination. Secondly, recombination sites are less important in the emitter compared to the bulk. This is because the minority carriers generated in the bulk of the wafer will not recombine in the emitter as the two regions have opposite doping and are separated by the pn junction, so only carriers generated in the emitter recombine there. As the emitter has a small volume net generation, recombination is minimal therein. Finally, the emitter lifetime is typically very low even if no metallic contamination is present. This is because of the very high doping levels associated with the emitter. These dopants make recombination centres, and also form numerous precipitates which also cause recombination. This means the relative lifetime change caused by metallic impurities in the emitter is marginal.

While empirical studies have provided a good understanding of the conditions required for PDG[77] it is still not fully understood at a mechanistic level. A number of mechanisms to explain PDG have been hypothesised, although there is still no consensus within the literature. Finding the mechanism of PDG is challenging for a number of reasons. Firstly, the concentrations of impurities are small and hard to measure, with spatial resolution. This issue is made more challenging as the phosphorous rich regions is thin ~500nm[78], and there is significant variation within this layer. Secondly, it is hard to separate a number of important variables. The PDG may be affected by the maximum phosphorous concentration at the silicon surface, the depth of the phosphorous profile and the total amount of phosphorous diffused into the silicon. To some degree these can be controlled by choosing the correct diffusion temperatures and times. However the latter parameters strongly affect the effectiveness of any gettering process. As a result it is impossible to identify if the changes are due to altering the phosphorous profile, or the gettering conditions.

3.4.1.1 Phosphorous diffusion

Phosphorous diffusion (PD) is reviewed, as this enables a better understanding of the PDG process. PD is non-Fickian, as evidenced by the exemplary phosphorous diffusion profile in

Figure 28. This complex kink and tail diffusion profile develops because phosphorous diffusion proceeds via two different mechanisms[79], which detrimentally interfere with each other. Near the surface, Figure 28 region 1, the phosphorous concentration is very high ~10^{22} cm^{-3} and so the doping levels are also very high. This leads to the formation of stable, doubly negatively charged, vacancies. Phosphorous atoms, which are positively charged, form complexes with these vacancies. These complexes can then diffuse through the silicon much faster than a lone phosphorous atom, so the phosphorous diffusion is enhanced. Deeper within the silicon the phosphorus and vacancy concentrations both fall, but the concentration of silicon self-interstitials rises. The self-interstitials can form complexes with the phosphorus to facilitate the diffusion of the latter, see Figure 28 region3. However, there is an intermediate region where the point defects annihilate one another and the total concentration is small. Therefore diffusion is slow in this region, see Figure 28 region2.

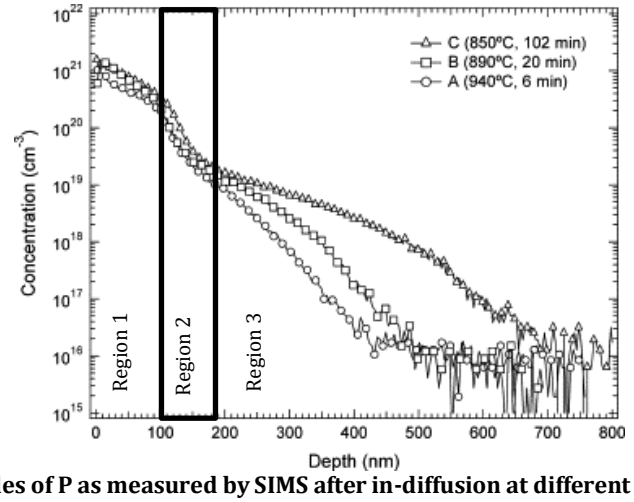


Figure 28. Diffusion profiles of P as measured by SIMS after in-diffusion at different temperatures and durations. From [80]**. The phosphorous profile is clearly non-Fickian, as a kink and tail can be seen in all of the temperatures chosen. Three regions with different diffusion behaviours have been highlighted.**

3.4.1.2 Precipitate gettering

The very high phosphorus concentrations at the surfaces results in the formation of phosphorous rich precipitates [81]. It has been hypothesised that these precipitates bind to and getter impurities. SiP precipitate density can be $10^{17}cm^{-3}$ [82], so they could have a significant impact on gettering. However, no direct evidence supporting this has been seen, potentially due

to the small size of the precipitates. It is also not clear if SiP precipitates would promote the co-precipitation of metallic precipitates, or if impurities would segregate to the SiP/Si interface.

3.4.1.3 Complex formation

It has been suggested that impurity based complexes may form in the phosphorous rich emitter. These complexes, which are states where two or more crystallographic imperfections bind and thus diffuse together until they are split, could reduce the energy associated with the impurities, enabling gettering[83]. This complex formation is supposedly due to binding between the positively charged phosphorous atoms and, presumably, negatively charged, impurities [84]. However, it has been noted that most metallic impurities are positively charged and so these complexes are unlikely to be stable[85].

An alternative complex has also been suggested. This complex consists of a double negatively charged vacancy, a phosphorous atom and an impurity. The former two are known to form complexes [79], and are negatively charged and so could be expected to form complexes with positive metal ions. As such this mechanism may be able to explain PDG.

3.4.1.4 Oxygen facilitated gettering

Another hypothesis claims that the oxygen incorporated during PDG facilitates the gettering process. During PD oxygen diffuses into the wafers from the surface glass. It is known that oxygen rich precipitates can form in wafers with high oxygen concentrations[86][87]. These oxygen precipitates are also known to getter metallic impurities[86][87]. However as pointed out by Syre et al[85] this does not explain why phosphorus must also be present for this gettering process to be effective. It is suggested that the role of phosphorous is to increase the local concentration of vacancies which promotes the formation of oxygen based precipitates. Syre et al[85] claim that this is a probable mechanism due to the similarities seen when comparing the SIMS profiles for iron and oxygen after PDG processing, see Figure 29.

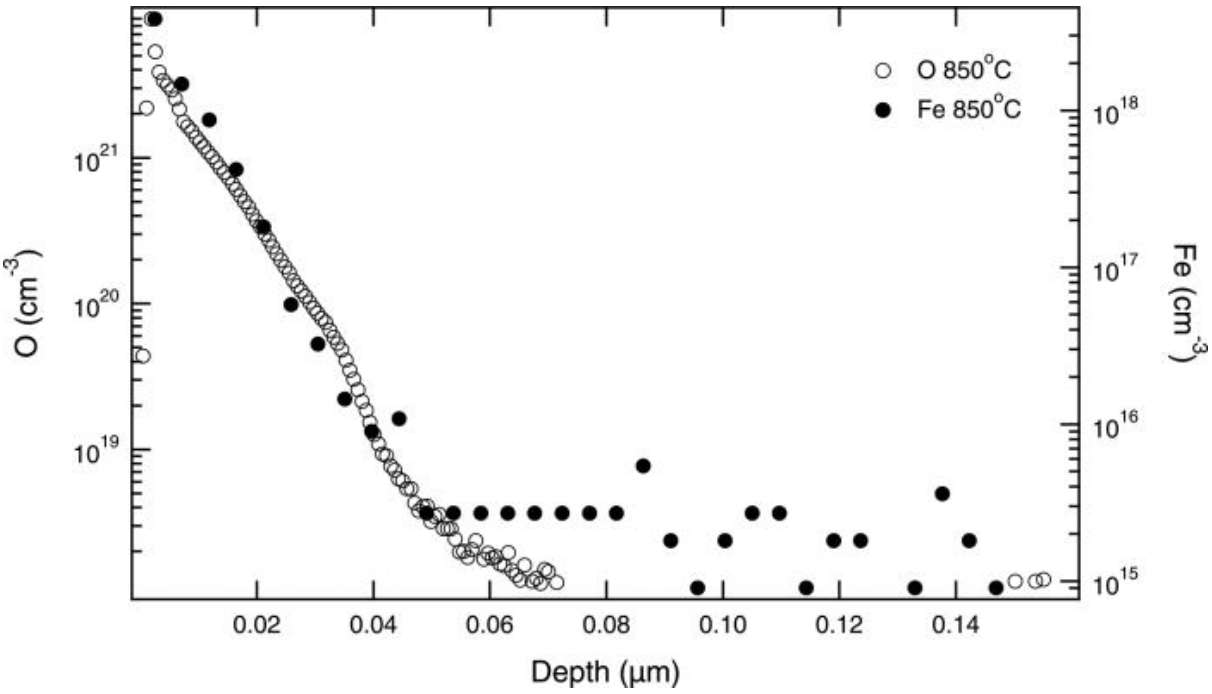


Figure 29. Oxygen and iron concentrations versus depth, for samples given PDG processing as determined by SIMS measurements. The PSG was supplied by a spin on source and the wafer was annealed at 850^{0}C for 30minutes. From [85].

3.4.1.5 Gettering into the phosphorous rich glass

An alternative hypothesis involves the segregation of impurities to the phosphorous rich liquefied glass that is typically used as the dopant source. It has been suggested by Vahanissi et al, that either the glass, or the glass/silicon interface acts as a sink for impurities[75]. They stress that this mechanism works alongside segregation of impurities into the emitter layer and is not a stand-alone process. Their conclusions are based upon Secondary Ion Mass Spectrometry data (SIMS) [88] and bulk iron measurements. These suggest that the PDG process removes iron from the wafer as well as simply re-distributing it, as iron appears to be lost from the system. However, SIMS is not particularly reliable in the first few nm measured, where the iron concentrations are highest after PDG, so these results may not be entirely reliable. Vahanissi et al removed the PSG before carrying out a second higher temperature anneal which they assumed would drive the impurities away from the gettering sites and back into solution. The bulk iron concentration did not return to its original level, which they concluded was due to permanent removal of impurities through gettering to the, subsequently removed, glassy layer. However, this conclusion is unlikely to be correct as the high

temperature anneal was not hot enough for their assumptions to be valid. This anneal was carried out at 1000^{0}C, compared to PDG temperatures of 800^{0}C and 900^{0}C, therefore it is unlikely that metallic impurities would have been completely removed from the gettering centres.

3.4.1.6 Doping levels

In addition to gettering, PD produces the n-type emitter region needed for the cell to operate, see section 1.2.1. The doping profile in the emitter affects the cell efficiency in a number of ways, all of which must be balanced when choosing the optimal PD conditions.

The doping profile in the emitter strongly affects the efficiency of the resulting cell. If the total doping is too low, the emitter will have a large sheet resistance, detrimentally increasing the series resistance in the cell, see section 1.3.5 [89]. The cell efficiency is also reduced if the doping level is too high at the surface as this leads to increased recombination at the surfaces. Additionally, the phosphorous rich layer typically is very recombination active. This is primarily due to the very high concentrations of impurities (dopants) and also the formation of SiP precipitates. Only carriers generated in the emitter can recombine within it. Reducing the thickness of this layer will result in fewer carrier pairs being generated in the emitter, and so recombination will be reduced. It is thus beneficial to reduce the thickness of the emitter layer, although ideally its conductivity should not be compromised. These last two factors indicate that a thin, weakly doped emitter region is desirable. It can therefore be seen that there are a number of competing factors which must be accounted for when designing an ideal emitter. PDG is only one of these factors.

3.4.1.7 PDG optimisation and limitations

PDG is not fully understood at a mechanistic level, but must still be optimised concurrently with other, potentially competing, factors. In addition to the doping effects discussed above, the processing times and temperatures should be minimised where possible to reduce cell cost. Despite these challenges, numerous optimisation models have been developed to maximise the

efficacy of the PDG process [90][91]. These have shown that phosphorous diffusion gettering is capable of reducing the iron concentration in wafers by two orders of magnitude[92].

PDG efficacy is highly dependent on the starting material. When processing mc-Si wafers, grains with an initially high lifetime, and low concentration of crystallographic defects such as dislocations, respond well to PDG, while grains with lower lifetimes are not significantly improved [93]. The lower lifetime grains contain a higher concentration of crystallographic defects which trap impurities, preventing their gettering. This immobilisation is partially due to the segregation of impurities to the strain fields associated with dislocations and other defects. Low lifetime grains may also contain a higher concentration of precipitates which must be dissolved before gettering can be completed effectively. This dissolution can be slow, particularly when the gettering temperatures are too low to dissolve all of the impurities at the start of the process [94], see section 4.5.2. This is the case when carrying out PDG on low lifetime grains. Although raising the PDG temperature may reduce this problem it would result in non-ideal doping profiles. Therefore, PDG is unavoidably limited by the requirements of the emitter.

3.4.2 Aluminium Gettering

Impurities can be gettered from the silicon wafers into aluminium rear contact layers during contact firing. As discussed in section 1.2.2, electrical contact between the silicon and the metallic aluminium is formed through a high temperature annealing step carried out at 880-920 ^{o}C [95]. This forms a molten Al:Si phase. Impurities such as iron strongly segregate into this molten phase and away from the solid silicon phase [96]. As such the liquid phase is an effective gettering centre [69]. However, conventional aluminium gettering/ contact formation steps are very short ~10 seconds [95]. Thus there is insufficient time for effective gettering to occur due to the slow diffusion of impurities. Longer annealing times, and higher temperatures, are unlikely to be used. This is because the purpose of the aluminium firing is to rapidly form a contact with appropriate doping levels. Higher thermal budget anneals can degrade the contacts

[97], as well as being a more costly process. Therefore aluminium firing is not optimised for gettering in industrial settings and consequently only has a minimal effect.

3.4.3 Low temperature gettering

Some gettering processes involve the use of low temperature anneals for long periods of time. The low temperatures make impurity capture effective, and long times are needed to overcome the slow diffusion associated with these temperatures. This form of gettering must be carried out late in the cell processing to ensure that the impurities are not re-released after a higher temperature process.

3.4.3.1 Internal gettering

It is possible to improve wafer lifetime through the short range re-distribution of impurities into crystallographic defects, a process referred to as internal gettering. These crystallographic defects include dislocations, grain boundaries and impurity precipitates these are all potentially associated with dangling silicon bonds and strain fields. They are able to trap impurities in four ways[98]. Firstly, chemical bonds can form between the impurities and the dangling bonds. Secondly, the impurities can segregate to the strain fields, relaxing the strain associated with both the impurity and the dislocation. Thirdly, the precipitates can act as nucleation sites for precipitates, see chapter 4 for more details. Fourthly, the defects have near equilibrium concentrations of point defects which may attract impurities [98]. Therefore, impurities may re-distribute towards grain boundaries[99], dislocations or precipitates, see Figure 30. This impurity capture affects the recombination in two ways. Firstly, it reduces the number of recombination sites as the impurities agglomerate together and so no longer act as individual recombination centres. This reduces the recombination rate. However, impurity capture also increases the recombination activity of the extended defects. These have minimal activity when pure, but can become very effective recombination centres when contaminated see section 1.3.2.2 [32]. This effect does not increase linearly with the contamination level, so if the dislocations become contaminated it is desirable that they capture as many impurities as possible. This slightly increases their activity but removes the impurities from the bulk of the

wafer. It is therefore important the any internal gettering captures impurities effectively as an ineffective process will reduce the wafer lifetime.

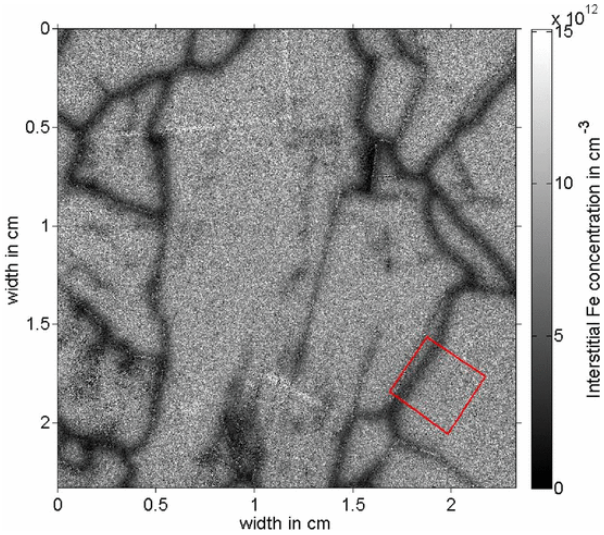


Figure 30. Internal gettering of iron towards the grain boundaries can be seen through the strong, clear reduction in the iron concentration at the grain boundaries. From [70] **using PL imaging.**

When impurities are captured by crystallographic defects, it is referred to as internal gettering. As impurity capture is thermodynamically enhanced at low temperatures, these are used during internal gettering at 300 ^{o}C-500 ^{o}C [100]. At these low temperatures impurity diffusion is slow so long annealing times, up to 15 hours [101], are required. When there is insufficient time for gettering impurities close to the internal defects will be gettered, but the ones located further away will be unable to reach the gettering centres fast enough. This is illustrated in Figure 31 which shows regions with high lifetimes adjacent to grain boundaries, an effective internal gettering centre, but lower lifetimes in the centre of the grains.

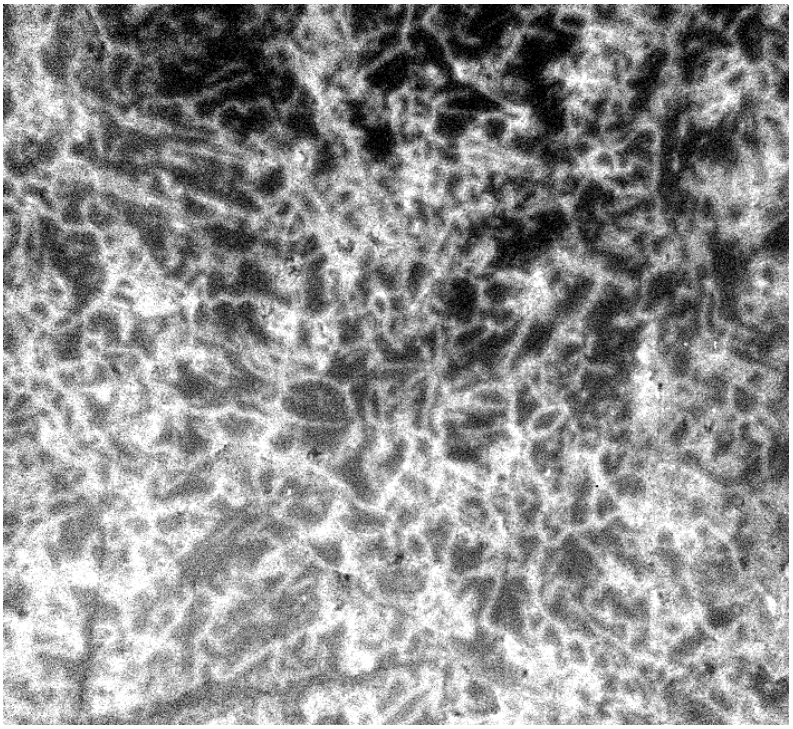


Figure 31. An un-calibrated PL image taken by REC solar, where lighter regions correspond to higher lifetimes. The wafer was from the bottom, highly contaminated region of an as-cast ingot. Internal gettering will have occurred upon the slow cooling of the ingot.

3.4.3.2 Combined phosphorous diffusion gettering and long low temperature annealing

Long low temperature annealing can also be used in combination with PDG to improve gettering to levels surpassing either technique in isolation. In this process, PDG is carried out as usual. However, the wafers are subsequently given a low temperature anneal to increase the fraction of impurities captured by the phosphorous rich layers. Annealing at 500^0C for 250 minutes can be seen to increase the resultant cell energy conversion efficiency by 0.8% absolute, which is a significant gain[102].

3.4.3.3 Low temperature gettering summary

Low temperature gettering can be a useful tool to improve wafer lifetimes. However, it cannot remove impurities from the wafer. Impurities will also unavoidably remain at highly deleterious locations such as dislocations. As such, low temperature gettering must be supplemented with additional gettering processes if very high quality solar cells are to be produced.

3.4.4 Porous silicon gettering

Another recently reported gettering technique uses a layer of porous silicon as a sacrificial gettering centre which is removed after gettering is complete. The layer of porous silicon can be

created through the use of an appropriate etching solution for example H_2O:HNO_3:HF solution in the ratio10:9:3[103]. Naturally, this porous layer has a high surface area with a large number of silicon dangling bonds present. The energy associated with impurities is reduced when bound to these dangling bonds. For example, Tsuo et all [104] report that the binding energy between copper and dangling bonds is 0.5eV higher than that between copper and a Cu_3Si precipitate. This means impurities can be gettered by the porous silicon, and are captured by the dangling bonds. The porous silicon can be removed after gettering leaving behind an upgraded wafer. Porous silicon has received most attention for its potential in improving substrate quality for the epitaxial growth of silicon on metallurgical grade silicon[105]. The porous silicon captures mobile impurities preventing their diffusion into the growing silicon layer[106], Figure 32 shows this schematically.

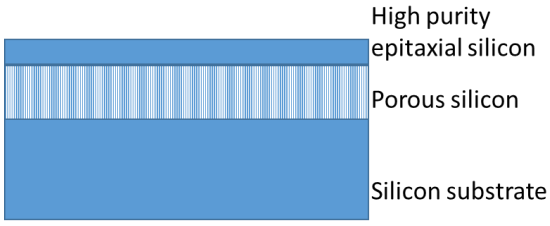


Figure 32. Sacrificial porous silicon layer preventing diffusion of impurities from the silicon substrate into the growing epitaxial layer.

3.4.5 Gas phase gettering

In gas phase gettering impurities are extracted from the wafers through a chemical reaction with an external gaseous atmosphere. The reactive gases in these atmospheres are typically chlorine based, including both molecular chlorine and hydrogen chloride. These reactions are often very favourable (2.27 eV reaction energy for a reaction between iron and molecular chlorine at 1000^{o}C) and so gettering may be effective. The products of these reactions are volatile and so are removed in the gas stream preventing the saturation of the gettering centre. However, the gettering agents can also etch the silicon, so this type of gettering processes has typically also included a simultaneous oxidation process as this forms a protective silicon dioxide layer[107][108]. However, this oxide is a potent diffusion barrier and it therefore

reduces the flux of impurities from the bulk of the wafer into the gettering atmosphere. Gas phase gettering is an important focus for this work, and will be discussed in detail in chapter 5.

3.5 Summary

This chapter has discussed why gettering is an important industrial process for the production of solar cells. A range of different gettering techniques have been developed, and it is possible to use these techniques in series so the final material is better than would be possible using any of these gettering processes individually. This is a standard process for the solar industry where a wafer is first given a PDG process, followed by an aluminium gettering process during contact firing. A low temperature gettering anneal could trivially be incorporated as well. However, these current processes cannot be improved a great deal further as these gettering processes are limited by other factors such as the need to create optimal doping profiles in junction regions.

Even after gettering, impurities located at dislocations are still problematic. As discussed in section 1.4.2, the recombination activity of dislocations is very low unless they are contaminated. In mc-Si the dislocations remain contaminated, and highly recombination active. There is currently a significant amount of interest in generating mc-Si with lower dislocation densities, and thus lower recombination activities after gettering. This is achieved by decreasing the grain size[51], which is otherwise undesirable as reduced grain size can also be associated with a reduction in the achievable lifetime [109]. If the gettering processes could be improved further the dislocations may become unimportant. In turn this would allow ingots with large grains and high dislocation densities to be manufactured without affecting the final wafer lifetime. Impurities can also be seen to be problematic in mc-Si as approximately 15% of the ingot is conventionally discarded due to unacceptably high contamination levels.

It is important to understand, develop, or modify gettering processes such that the contamination levels can be reduced and they cease to be problematic. It would be beneficial if these gettering processes could be used in conjunction with current cell processing techniques.

This means any high temperature process must be carried out before PDG to prevent additional, undesirable, dopant diffusion. With this in mind, two gettering techniques have been studied in this work: saw damage gettering, which aims to upgrade low quality currently discarded mc-Si, chapter 4; and gas phase gettering, which aims to improve the gettering of all mc-Si wafers, see chapter 5.

4 Saw Damage Gettering

As discussed in chapter 3, it would be beneficial if a new, low cost gettering process could be developed. In this chapter a new gettering technique which can remove impurities from the wafer, Saw Damage Gettering (SDG), will be discussed. This technique utilises the dislocation rich, saw damage (SD) introduced during ingot wafering, as an impurity sink to facilitate the permanent removal of impurities. This technique has been briefly hypothesised [110], but it is believed that this work is the first in-depth experimental study.

SDG completely removes some of the impurities from a wafer rather than simply moving them to less deleterious locations or configurations. This is referred to as external gettering for the remainder of this work.

4.1 Introduction

As has been discussed in section 1.4.2, wafers from the top and bottom mc-Si red zones remain too contaminated to be used for solar cells even after conventional gettering processes. They are therefore discarded, wasting cast material. SDG is a low cost external gettering technique intended to upgrade these wafers such that they become suitable for solar cell production. SDG is designed to take place immediately after the ingot is sawn into wafers, and should thus be easily integrated into current solar cell processes. It is also possible that this process could be utilised to enable UMG-Si to be used commercially. As discussed in section 1.4.1, this material is currently too impure to be used in commercial solar applications, however SDG may be able to upgrade these low cost wafers such that they can be viably utilised.

4.1.1 Saw damage gettering principles

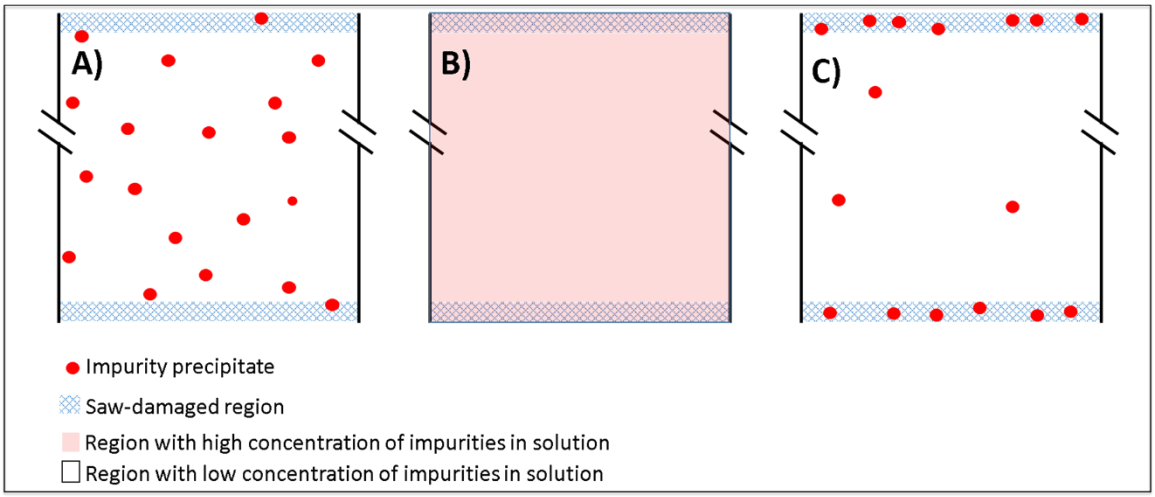


Figure 33. The idealised SDG process, A) is the as-sawn wafer, B) is the wafer during the high temperature SDG-anneal with impurities dissolved, and C) is the wafer after the completed SDG process.

SDG occurs when an impurity supersaturation in the bulk of the wafer is relieved through the nucleation and growth of precipitates within the SD regions at the wafer surfaces. These growing precipitates capture impurities from the bulk of the wafer, gettering them. These impurity rich regions are then removed during wafer surface texturing. SDG consists of two thermal stages. Firstly, a high temperature anneal, hereafter referred to as a SDG-anneal. This high temperature process results in an increase in the impurity solubility, so that precipitates formed during ingot cooling may be dissolved. This increases the concentration of mobile impurities and decreases the precipitate density within the wafer, as depicted between A) and B) in Figure 33. This shows the ideal case where all as cast precipitates are fully dissolved during the annealing process

In the second thermal process, wafers are carefully cooled to promote precipitation within the SD regions. During cooling, the impurity solubility will decrease and at some point the concentration of impurities in solution will exceed the solubility, thus becoming supersaturated. This supersaturation will increase upon further cooling. Impurity supersaturations are, by definition, energetically unfavourable, so the system can relax by forming impurity rich, precipitate, phases. There is an energy barrier to precipitate nucleation which means it is slow at moderate supersaturations [111]. This energy barrier is reduced when nucleation occurs at

crystallographic defects, such as grain boundaries and dislocations [111]. Precipitates will therefore preferentially form at these defective sites. The SD is a region with a high density of dislocations and so contains many potential nucleation sites relative to the bulk of the wafer. Therefore a high fraction of all nucleation events will occur within the small SD region. As they grow, these precipitates will rapidly reduce the local impurity supersaturation. However, in the bulk of the wafer nucleation events are less frequent so there are fewer precipitates. The supersaturation thus relaxes more slowly in this region. This results in a concentration gradient from the bulk of the wafer to the SD at the surfaces. Impurities diffuse down this gradient towards the SD resulting in macroscopic impurity diffusion to the SD. The impurities are then removed during the subsequent etching process which removes the SD and textures the surface. The resulting wafer thus contains fewer impurities than before the SDG process. It is important that the impurity flux is to the surface is maximised during SDG.

As SDG promotes the growth of precipitates to getter impurities, the thermal cooling profile must be appropriate. Precipitates can nucleate and grow at any crystallographic defects, either in the SD or the wafer bulk. The precipitates then compete to capture supersaturated impurities, and thus to grow. There is a relatively small concentration of crystallographic defects in the wafer bulk, so nucleation is likely to be slow. However, some of the precipitates formed during ingot casting may remain after the SDG-anneal. These will be able to grow on cooling after the SDG-anneal, capturing impurities and reducing bulk supersaturation without requiring a nucleation event. This reduces the impurity gradient between the bulk and the surfaces reducing the flux of impurities to the SD and the SDG efficacy. This can be avoided if the SDG-anneal completely dissolves the precipitates. In this situation, precipitate growth in the bulk can only occur after a nucleation event, although it should be noted that impurities may still be captured and precipitates nucleated by crystallographic defects such as dislocations and grain boundaries located within the bulk of the wafer. It is also important to control the cooling rate to maximise total impurity flux to the SD. While this could be improved by increasing the cooling time this would increase the time required to process the wafers. Therefore, a model to

optimise the cooling profile, to maximise gettering while minimising process time, was developed. This is discussed in section 4.3.1.

4.1.2 Appropriate experimental controls

The SDG process is designed to reduce the total impurity concentration within the bulk of wafers. As discussed in section 2.4.1, minority carrier lifetime measurements were used to characterise the impurity concentrations as these measurements are sensitive to very low impurity concentrations, (10^{10} cm^{-3}) [44].

However, there is a complication when using lifetime measurements to understand impurity profiles; the lifetime is sensitive to both impurity concentration and location, thus the re-distribution of impurities can falsely indicate that they have been removed or introduced into the wafer. Both conventional wafer processing and SDG consist of an anneal followed by a cooling process which is rapid compared to the cooling process directly after casting mc-Si ingots. During the anneal precipitates which formed during ingot casting will at least partially dissolve. A number of these impurities will be gettered. However, some fraction will remain in solution prior to wafer cooling. When, during the cooling process, the impurities become supersaturated, precipitates may form. Once the wafer has fully cooled any impurities which remain in solution are trapped and act as point defects. The fraction of impurities located in precipitates is likely to be increased when the wafers are cooled slowly, as there is more time available for diffusion to these sites, conversely the fraction of impurities in solution is likely to be reduced in wafers cooled slowly. Consequently, any processing undertaken after casting is likely to decrease the number of impurities located at precipitates, and may thus increase the number of impurities in solution, even if some gettering has occurred. As impurities in solution are potentially more recombination active than those located in precipitates, see section 1.3.2, this means that any thermal processing may falsely indicate that a process was detrimental in that the measured lifetime will decrease due to movement of impurity atoms from within precipitates into solution. In SDG samples, this ambiguity can be mitigated through the use of a control which is a “sister wafer” to a SDG sample, see Figure 34, which has undergone the same

processing except the SD is removed prior to thermal processing so SDG cannot occur. The difference between the two wafers can thus be attributed to the SDG process alone.

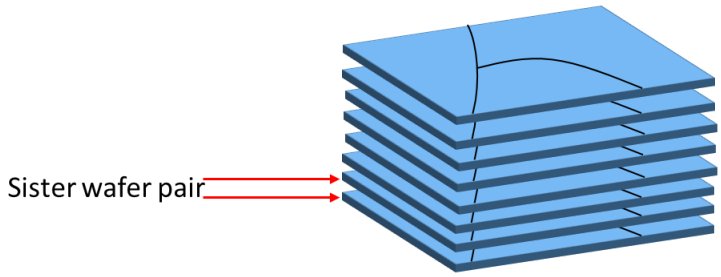


Figure 34. A schematic of a stack of wafers. Two sister wafers are highlighted.

4.2 Experimental method.

This section shows how the experimental processes discussed in chapter 2 are combined into the SDG process.

As discussed, sister wafer pairs were selected. The controls were preliminarily cleaned see section 2.1.2, then etched for 40 minutes in TMAH at 60 ^{o}C. This removed 25 microns of material [54] and hence the saw damage which is in a layer 10 µm thick at the surface of the wafers [54]. Both controls and SDG samples were then fully RCA cleaned. Concurrently, the quartz-ware, including the annealing tube and wafer spacers, were also cleaned see section 2.1.3. The wafers were then arranged into a stack in the furnace tube, such that they were separated by a quartz half-ring at two corners. They were then fully inserted into the annealing tube. This was then fully inserted into the furnace which was pre-heated to the SDG anneal temperature and given thermal processing as detailed below. After annealing, the SDG samples were dipped in HF and given a 40 minute, 60 ^{o}C TMAH etch to remove the saw damage and to ensure the same surface properties across sample and control wafers. All wafers were then given a further HF dip, before a 70 nm thick silicon nitride passivation layer was deposited on the surfaces at 350 ^{o}C. Lifetime measurements were then made using a Sinton WC-120 lifetime tester operating in QSSPC mode. The lifetime values were measured at an injection level of 10^{15} cm^{-3}. See Figure 35 for a schematic of this process. It should be noted that unless otherwise stated, all of the individual data points presented in the following graphs included information from six pairs of sister

wafers processed in at least two runs separated by at least a day, to reduce the impact of anomalous individual results. For all data, the average value is presented and the error bars are the standard deviations seen in the data for that point.

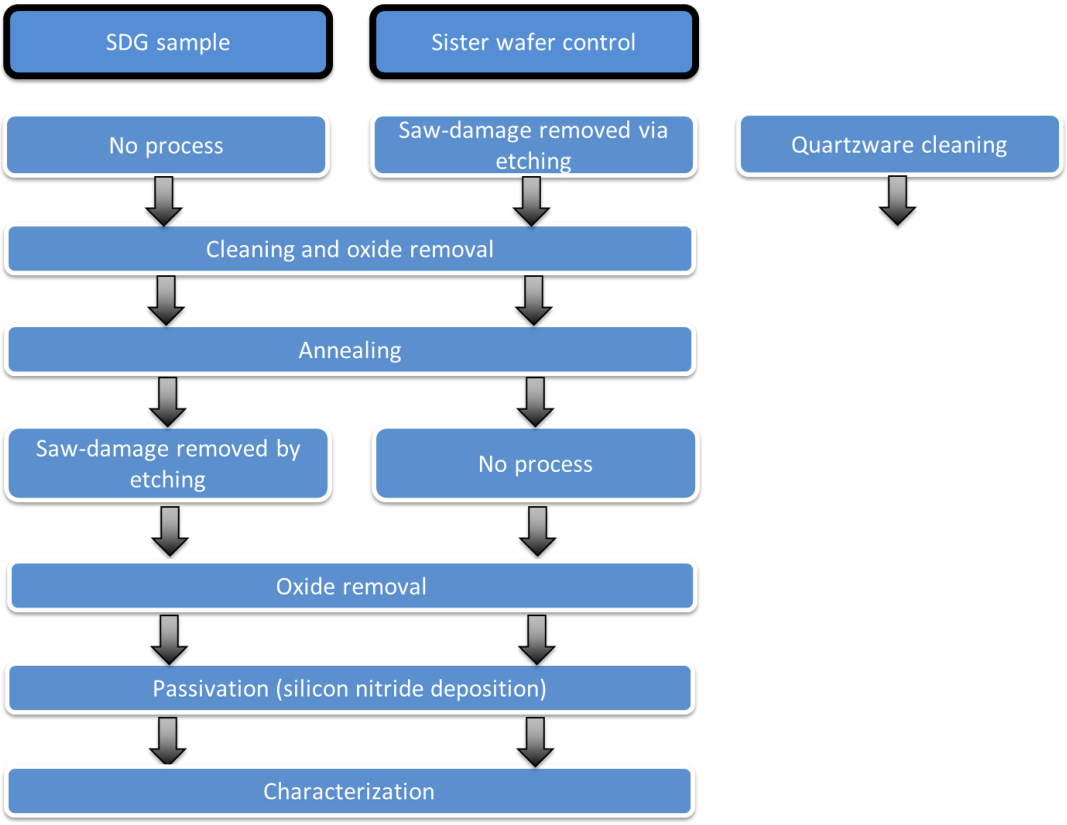


Figure 35. A schematic of the SDG process including controls.

A phosphorous rich emitter was formed on a number of SDG processed wafers, to enable phosphorous diffusion gettering (PDG) to occur. This was carried out on wafers already given SDG processing and their associated controls. Firstly the silicon nitride layers were removed and the samples were cleaned. A SOG layer was then deposited, and baked onto the surface see section 2.1.5. The wafers were then annealed at 950 ^{o}C for half an hour to drive in the phosphorous, followed by an 850 ^{o}C half hour anneal to increase PDG efficacy. Phosphorous diffusion is faster at the higher temperature which thus enables a phosphorous rich layer to develop, at the lower temperature PDG efficacy is increased. Thus this two phase annealing process is expected to increase gettering relative to a single phase cooling process [79], [91]. The samples were quenched to room temperature to trap any interstitial iron in solution were

its concentration could subsequently be determined using lifetime measurements, see section 2.4.1. Then the SOG was removed by an HF dip, and the phosphorous rich region removed using a TMAH etch at 60 °C for 10 minute which removed at least one µm of material from each side of the wafer. Finally, a silicon nitride layer was deposited and lifetime measurements made, see above for details. See Figure 36 below for a schematic.

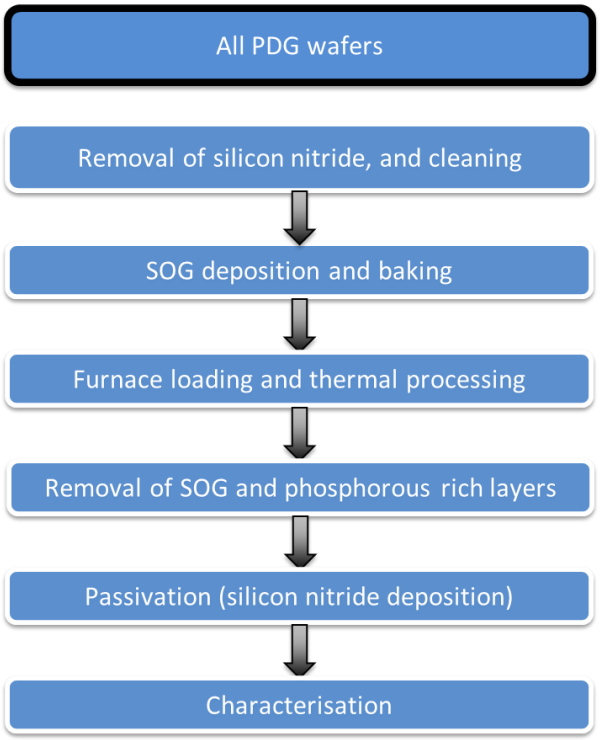


Figure 36. A schematic of the emitter formation and phosphorous diffusion gettering process.

4.3 Optimal cooling rates

The wafer cooling rate will strongly affect SDG efficacy. This cooling rate should be designed to maximise the total flux of impurities to the SD, in an industrially viable timescale. If the diffusion is assumed to be Fickian, the flux J is determined by

4.3.1
$$J = -\frac{dc}{dx} D_T$$

Where c is the concentration of impurities, x is distance, and D_T is the diffusion co-efficient under the conditions in question. The methodology for finding the appropriate cooling profile is discussed below, and was developed with the help of Dr Sebastian Bonilla and Toby Burton.

4.3.1 Modelling the effect of cooling profile on saw damage gettering effectiveness

Due to the high precipitation rates, the impurity concentration in the SD regions is assumed to be approximately equal to the solubility. However, there will be a supersaturation in the bulk unless the cooling rate is low enough for equilibrium conditions to develop. This means there will be a concentration gradient inducing flux towards the surfaces. As the concentration gradient results from the bulk supersaturation, it will be enhanced at higher cooling rates where the supersaturation is increased. By contrast, the diffusivity of impurities falls as the temperature is reduced, typically following an Arrhenius relationship of the form.

4.3.2 $$\boldsymbol{D_T = D_0 \exp\left(\frac{-E_a}{kT}\right)}$$

Where D_T is the diffusivity at temperature T, D_0 is a diffusivity correction factor, E_a is an activation energy, k and T have their usual meaning.

Assuming that the complete cooling profile must be complete within a finite time period, the optimal cooling rate must be a compromise between the two factors.

When diffusing, impurities have a characteristic diffusion length L which is the average distance that they will travel during the diffusion time, although the diffusion length will vary for different impurities. A thermal profile was developed which ensured that, while cooling, the diffusion length at any given temperature is independent of temperature. This can only be true for a single impurity which in this work was iron. This profile means that as the temperature and diffusivity falls, the cooling rate decreases, a full derivation can be found in [112].

4.3.3 $$\boldsymbol{L = g\sqrt{D(T)t}}$$

Where g is a unit-less geometric constant.

This model has been used to create a cooling profile for a wafer starting at 980 °C, the highest temperature used in this work, see Figure 37. This cooling profile was used for all SDG processes unless otherwise specified. Samples SDG-annealed at lower temperatures began their cool from the appropriate part of this curve and thus the duration of the cooling process was shorter for lower starting temperatures. Once the wafers reached 500 °C the wafers were

moved into the cold zone of the furnace and removed as soon as they were cool enough to handle safely. Consequently the final part of this cooling process was much faster than would be expected if the above model was to be continued until room temperature was reached.

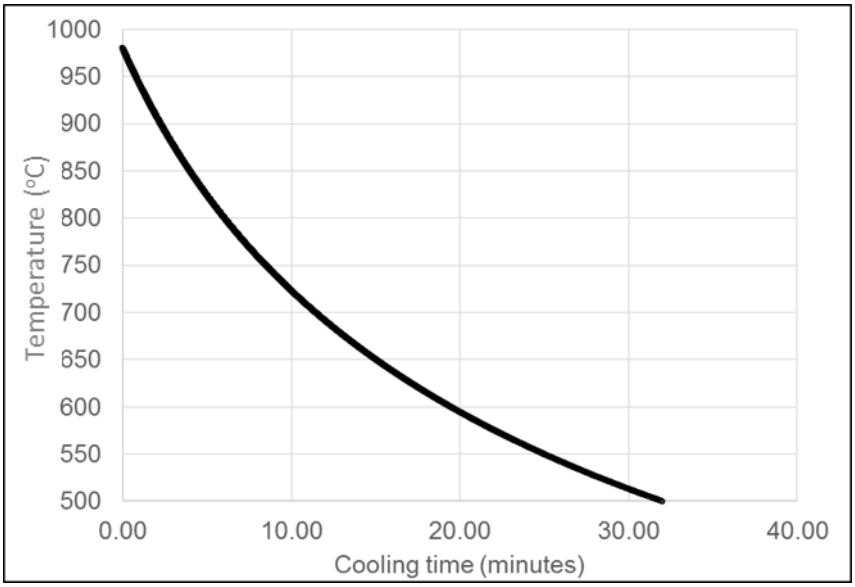


Figure 37. The cooling rate for a sample pre-annealed at 980^{0}C.

A Fickian model was then developed to find how the impurity profile in the wafer would change with time, assuming iron as the main impurity type. This model split the wafer into sections and modelled the impurity flux and concentrations in these sections as the wafer cooled. Only one half of the wafer thickness was modelled due to the samples' symmetry. The half wafer was then divided into thin sections, with initially uniform concentrations equal to the impurity solubility at the SDG annealing temperature. Precipitate nucleation is fast in the SD so the concentration of impurities adjacent to this region was assumed to be maintained at the solubility limit upon wafer cooling. The flux between regions was then determined using Fick's first law see equation4.3.1. In this, *dc* was the difference in concentration between two regions, and d*x* the distance between their two centre points. For each region, the flux in both directions was calculated, and the change in concentration over a small time interval found. The model then advanced to the next time interval, where the temperature was lowered as described above. A

similar model using a simple linear cool was also developed to highlight the benefits offered by the temperature dependent cooling profile.

The Fickian model developed above strongly indicated that a temperature dependent cool would enhance SDG efficacy. As seen in Figure 38 the modelled iron concentration is reduced by approximately a factor of two when using the temperature dependent cooling profile, relative to a linear cool lasting the same total time. It is possible to modify this model to optimise the cooling rate for different impurities.

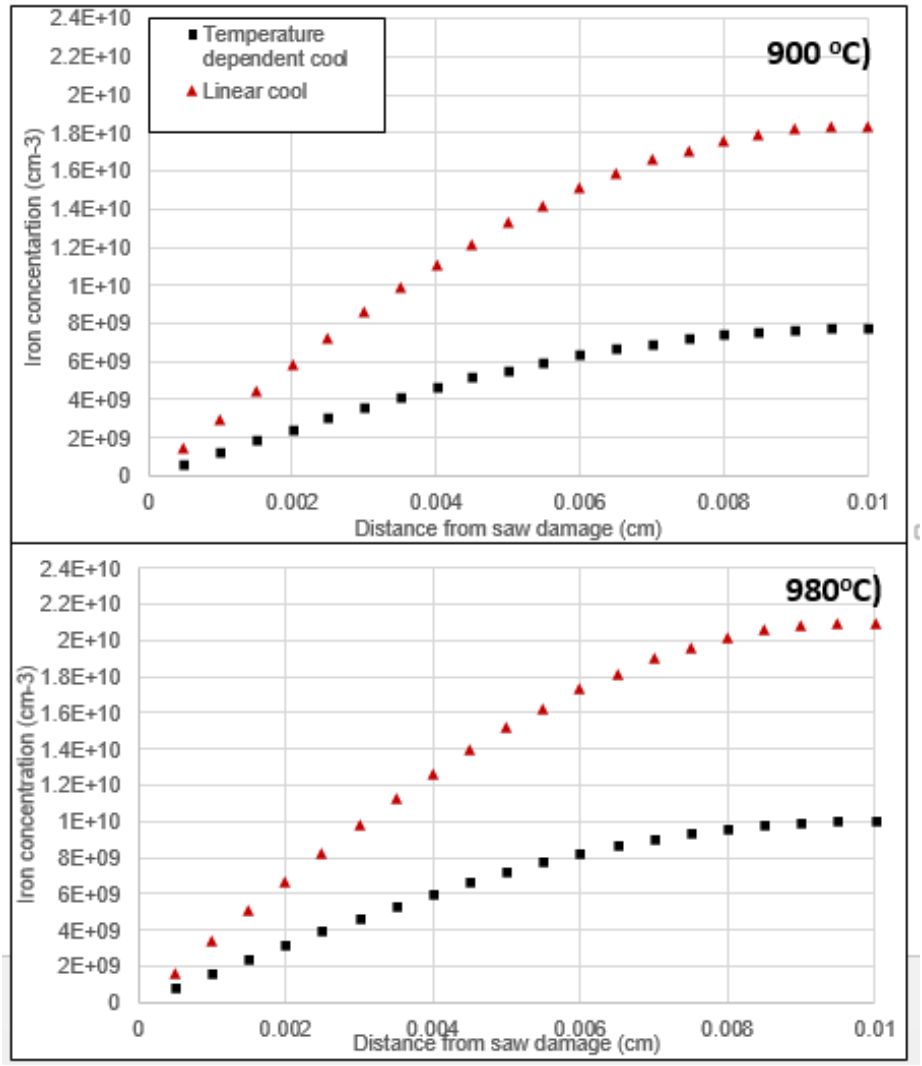


Figure 38. Results from modelling the diffusion of iron through silicon towards a perfect SDG gettering site. The difference between SDG samples given temperature dependent cooling and linear cooling can be seen. Above, is a sample cooled from 900 °C and below, is cooled from 980 °C. In this model the impurity concentration was determined by the solid solubility of iron at the initial temperature, 4.33 × 10^{13} and 2.64 × 10^{14} cm^{-3} respectively [113].

4.3.2 Experimental verification of cooling modelling

As the cooling profile would be used for the remainder of this work it was important to ensure that the temperature dependent cool developed above outperformed the linear cool. This validation was demonstrated by giving a set of SDG samples and controls either a temperature dependent cool, as detailed in Figure 38, or a linear cool designed to reach the finish temperature (of 500 ^{o}C) in the same time. After processing, the lifetimes were compared, and as shown in Table 4, the temperature dependent cool significantly outperformed the linear cool. This difference is particularly marked after a 900 ^{o}C SDG anneal where the lifetime after the temperature dependent cool was 9.3 µs, and that of the linearly cooled sample only 3.9 µs.

	Linear cool		**Temperature dependent cool**	
Annealing temperature [^{o}C]	**Sample lifetime [µs]**	**Control lifetime [µs]**	**Sample lifetime [µs]**	**Control lifetime [µs]**
900	3.9	2.1	9.3	1.2
850	10.1	4.4	9.9	2.4

Table 4 The difference between processing samples with a temperature dependent cool, and a linear cool. All samples were given a SDG-anneal lasting 20 minutes. Only one sample was processed per data point in this section.

In addition to lifetime measurements, interstitial iron concentrations were also measured, as detailed in Table 5. It can be seen that SDG reduced the concentrations of interstitial iron in the bulk of the wafers, as the concentrations are at least a factor a six lower in samples given SDG processing relative to their controls. In addition, the temperature dependent cools resulted in more extensive iron gettering. This is particularly pronounced when cooling from 900 ^{o}C where the fraction of interstitial iron in the SDG sample is 25 times lower than in the control, this compares to a factor of 6 difference after a linear cool. When cooling from 850 ^{o}C the difference between the two cooling rates was much less pronounced. This may be partially because the furnace can only cool relatively slowly, ~10 ^{o}C s^{-1}, at lower temperatures <650 ^{o}C. This means at lower temperatures the "linear" cooling profile cannot be followed by the furnace and the actual

cooling profile more closely matches the temperature dependent cool. This similarity can be seen in the final gettering results. This effect is likely to be more pronounced when cooling from lower temperatures where the deviation occurs over a larger fraction of the cooling profile.

	Linear cool	**Temperature dependent cool**
Annealing temperature (°C)	**Fraction of interstitial iron removed by SDG processing**	
900	0.83	0.96
850	0.86	0.88

Table 5. How the iron concentration is affected by different cooling profiles under the same conditions as in Figure 38. The fraction of iron removed is the concentration in the control divided by the concentration in the gettered sample. It should be noted that only the interstitial iron concentration can be measured.

4.4 Results

This section contains the majority of the results from SDG and PDG experiments. The implications and explanations of these results are discussed later.

4.4.1 Importance of saw damage gettering-anneal conditions

A range of SDG-annealing temperatures and times have been tested. For each thermal budget investigated, six pairs of sister wafers have been processed to reduce the impact of the inter-sample variation assosiated with mc-Si. All of these samples were subjected to the cooling profile shown in Figure 37. The shape of the cooling profile, but not the total cooling time was the same for all of the SDG annealing temperatures.

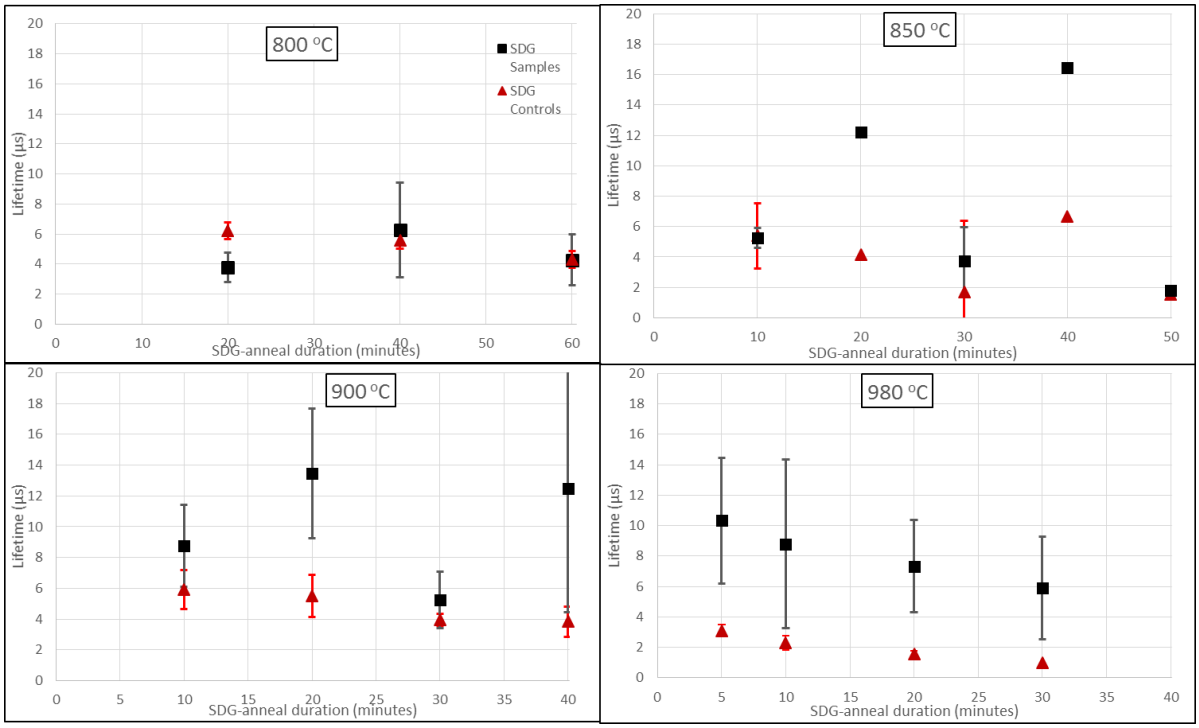


Figure 39. The lifetimes of wafers from the bottom red zone of an ingot after SDG thermal processing. The temperatures shown are the temperatures of the SDG-anneal, and the times are the duration of the SDG-anneal. The SDG sample wafers have been annealed with the SD present, and the control wafers had their SD removed prior to annealing. All wafers followed the cooling profile highlighted in Figure 37, starting their cooling profile at the relevant temperature, such that SDG samples SDG annealed at lower temperatures were cooled for less time.

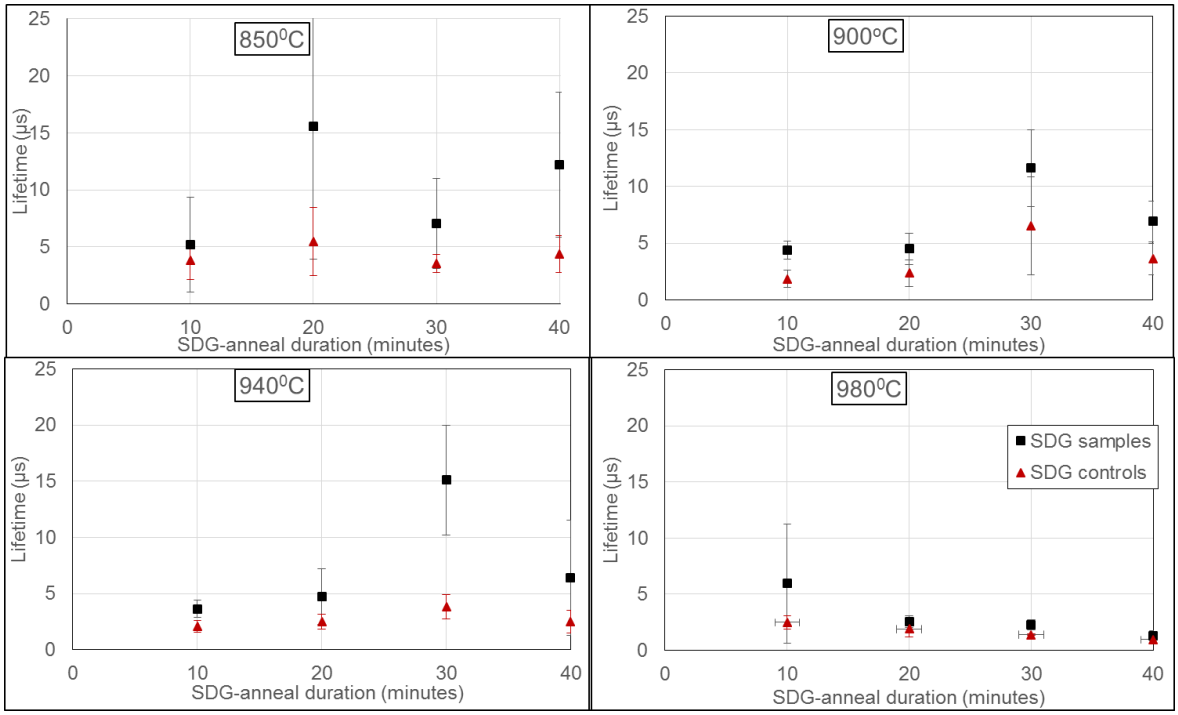


Figure 40. The lifetimes of wafers from the top red zone of an ingot after SDG thermal processing. The temperatures shown are the temperatures of the SDG-anneal, and the times are the duration of the SDG-anneal. The SDG sample wafers have been annealed with the SD present, and the control wafers had their SD removed prior to annealing. All wafers followed the cooling profile highlighted in Figure 37. They intercepted this curve at a temperature appropriate to the SDG annealing conditions.

Perhaps the most important observation which can be made from Figure 39 and Figure 40 is that SDG does improve the wafers. SDG samples outperform their controls in a wide range of cases. The relative improvement provided by SDG is significantly more pronounced when used on material from the bottom red zone of the ingot. The difference between SDG samples and their controls is more statistically significant when using bottom red zone material, and the lifetime difference between samples and controls is more likely to be larger than the inter-sample lifetime variation. This suggests that SDG processing has a larger impact on the wafer lifetime when using material from the bottom red zone.

Figure 39 and Figure 40 also indicate that the lifetimes after SDG are reduced if the thermal budget of the SDG-anneal is too high. This can be seen as SDG samples processed at 980 ^{o}C have lower lifetimes than those SDG-annealed at lower temperatures. The best lifetimes achieved after 980 ^{o}C SDG-annealing are 6 μs and 10.2 μs from the top and bottom red zones respectively. This compares to bests of 15.8 μs and 16.2 μs respectively, when processing at 850 ^{o}C. In addition, in both figures, the lifetime of wafers processed at 980 ^{o}C are reduced as the SDG-annealing times are increased. This trend is seen in SDG samples given full SDG processing and also, to a lesser extent, in their control wafers. There are a number of potential explanations for this effect, these will be discussed in section 4.5.3.

It can also be seen that SDG is ineffective if the thermal budget of the SDG-anneal is too low. This can be seen in Figure 39 where all of the SDG samples SDG-annealed at 800 ^{o}C showed no gettering response. In these wafers, the controls were indistinguishable from the SDG samples. In addition, the SDG samples SDG-annealed at 850 ^{o}C for ten minutes also showed minimal gettering while longer SDG-anneal durations at this temperature were significantly more beneficial.

4.4.2 Impact of starting wafer characteristics on saw damage gettering

As seen above, the SDG response is affected by the wafers' origins. Therefore, it was important to analyse how the gettering response varied when using wafers from different locations within

the ingot. In this section five stacks of sister wafers from the bottom red zone are analysed. One wafer from each stack was analysed in a PL system by REC solar. This enabled impurity and defect clusters to be located prior to SDG processing.

PL images can be used to identify regions with high defect densities, (region 1, Figure 41), and regions with high contamination levels (region 2 Figure 41). Connections between the presence of these imperfections and the wafer lifetime after SDG could then be made. Wafers A and B contain regions with very high impurity concentrations and thus low lifetimes. These wafers were grown with their right edge in contact with the crucible, so these edges were heavily contaminated by the crucible, as seen in the images. However, these impurity rich regions seem to only weakly affect the lifetime after SDG. This can be seen by comparing stacks B) and D) which are similar apart from the presence of the large highly impure region in B). Despite this region, the final lifetime of stack B) is still 96% of that of stack D). By contrast, defect rich regions appear to be highly detrimental to the SDG process. These regions are prevalent in stack A) and this has a post SDG lifetime which is only 53% of that in stack B which is otherwise similar.

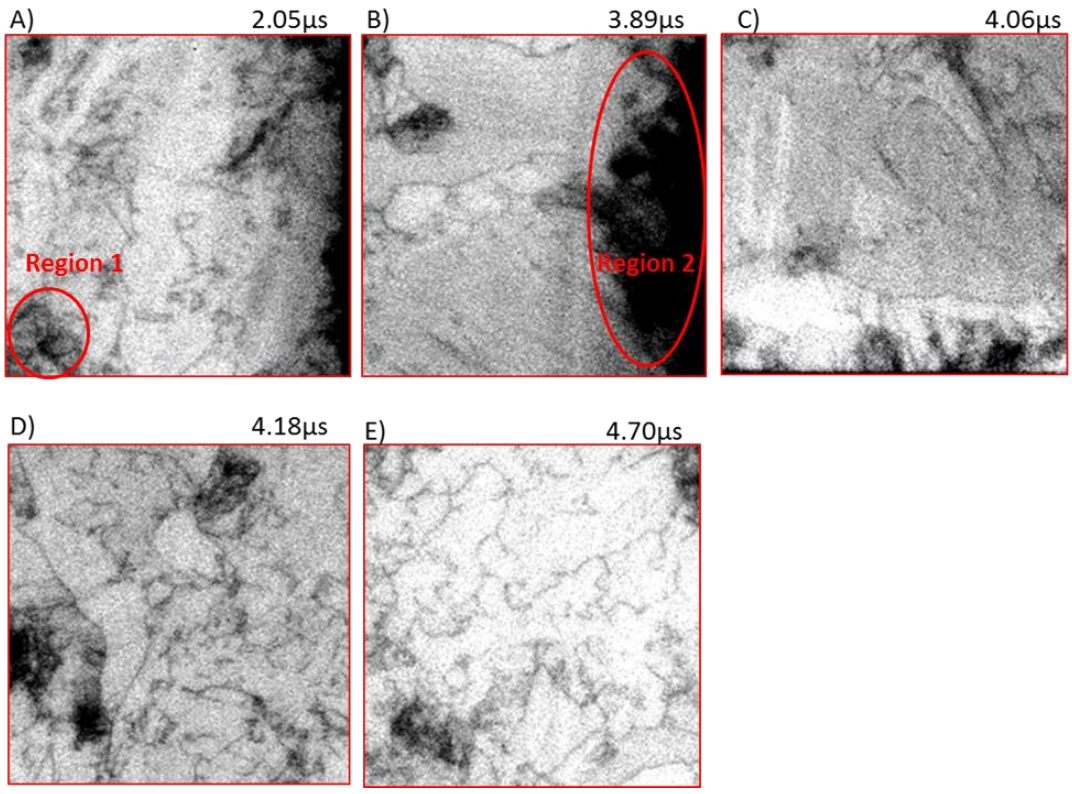


Figure 41. The PL images from wafer stacks, and the mean lifetimes observed in wafers given SDG processing from these stacks. Dark contrast in the PL image equates to lower localised lifetimes. A) and B) have been cut from the edge of the ingot, and their right side was in contact with the crucible during cooling. All the wafers are from the bottom red zone and were SDG-annealed at 850 °C for thirty minutes. These images were taken by REC solar, and supplied with the wafers.

4.4.3 Dual saw damage gettering and phosphorous diffusion gettering processing

If it is to be industrially beneficial, SDG must have a stable effect which is still observed after full cell processing. In this work, a stable effect is defined as one which is detected after SDG, and which is still observed after a second gettering process. The effects of SDG may be lost if significant numbers of precipitates remain in the bulk of the wafer at the conclusion of the process. These would not significantly affect the lifetime immediately after SDG, and so may not be detected by lifetime measurements. However, they could release impurities when the wafer is re-heated. This would reduce the quality of the wafers after a second thermal process such as PDG. This can be tested for by giving the wafers a second gettering process, in this work PDG. The results of this are presented in Figure 42 and Figure 43 below.

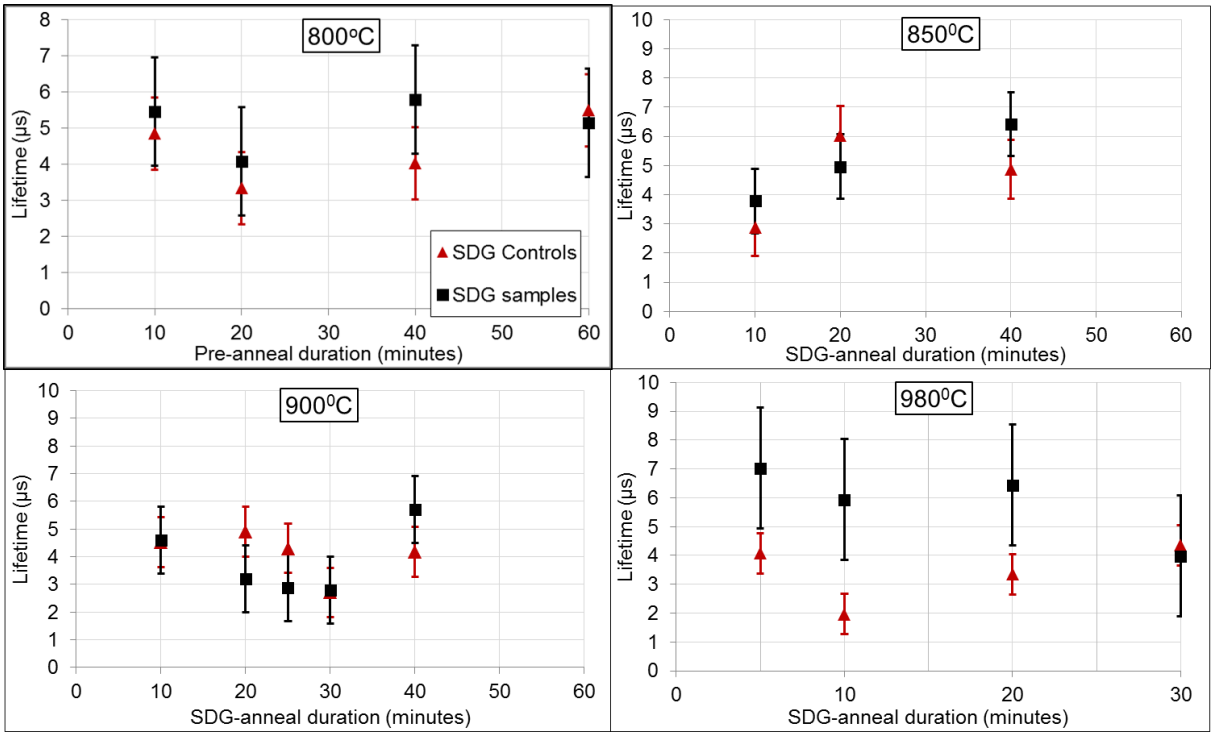


Figure 42. The lifetimes of wafers from the bottom red zone of an ingot given SDG and then PDG processing. The times and temperatures refer to the SDG SDG-anneal conditions. All of the SDG samples were given the same PDG process.

Comparing Figure 42 and Figure 39 shows that there are a number of SDG process conditions which improve the wafer lifetimes immediately after SDG but which have no lasting lifetime effect after a second gettering process, PDG. This is the case for wafers given SDG-anneals at 850 °C. As discussed, these initially respond well to SDG but after PDG there is no observable difference between SDG samples and controls. Figure 42 shows that the lifetime benefits of SDG are only stable for wafers which were SDG-annealed at temperatures of 980 °C. In these samples, the benefits deteriorate slightly after longer SDG-anneals.

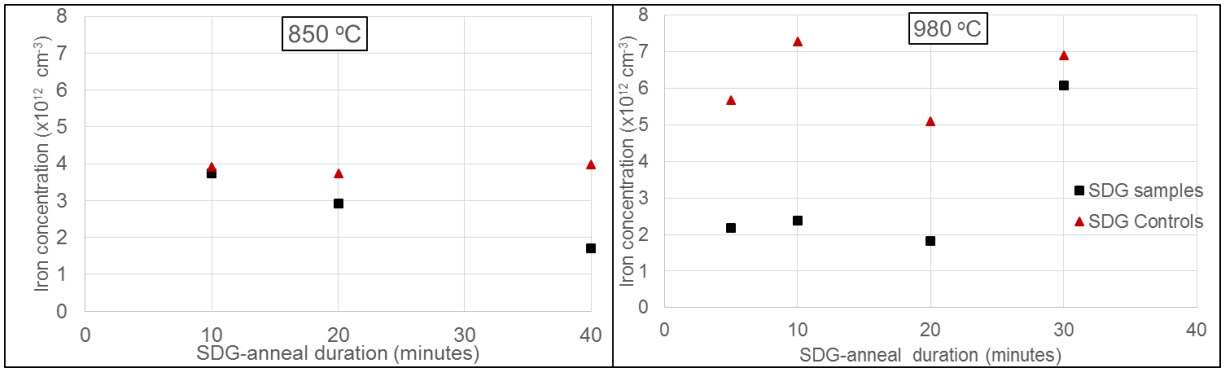


Figure 43. The concentration of interstitial iron remaining after both SDG and PDG processing. The times and temperatures are those used in the SDG SDG-anneal.

Figure 43 shows that the SDG process can result in a stable reduction in the interstitial iron concentration of the wafers. As both SDG samples and controls have had the same thermal processing it can be inferred that this reduction in interstitial iron concentration will be associated with a reduction in the total iron concentration (including iron bound to crystallographic defects and precipitates). SDG samples processed at 980 °C for ten minutes show approximately 68% reduction in interstitial iron concentrations relative to their control wafers which were not given SDG processing. However, no benefit to either lifetime or interstitial iron concentration is seen in the SDG samples SDG-annealed at 980 °C for thirty minutes. It is not clear if this is due to accidental contamination of the wafers, or if this is because the SDG process was less effective. The latter is considered more probable as SDG has already been seen to be less effective after high thermal budget processing, see Figure 39.

Figure 43 also shows that SDG-annealing wafers at 850 °C can reduce the iron concentration within the wafer, and that this effect is not subsequently lost when the wafer is given further thermal processing (PDG anneal). It should be noted that this stable iron concentration reduction is not associated with an increase in the wafer lifetime. The reduction in interstitial iron concentrations appears more pronounced in wafers annealed for longer times. These eventually reach interstitial iron concentrations comparable to those seen in SDG samples annealed at 980 °C. Additionally, no effect is seen after a SDG-anneal which only lasted ten

minutes. This agrees with Figure 39 and Figure 40 which show no improvement in lifetime due to SDG after such low thermal budget annealing.

4.5 Discussion

In this section the results described above will be discussed. This discussion covers how these results can be used to understand the SDG process better, and also covers some of the wider implications of these results.

4.5.1 Importance of starting wafer properties

It has been shown that the efficacy of the SDG process is affected by the starting wafers used. In particular, wafers which contain high concentrations of dislocations and other crystallographic defects appear to respond less effectively to SDG processing. There are two phenomena which could cause this effect. Firstly, the impurities may be strongly bound to these defects. Consequently, fewer impurities enter solution when these defects are numerous. As only impurities in solution can be gettered, impurity trapping would reduce SDG efficacy.

SDG efficacy could also be reduced by the presence of defects if they promote precipitate nucleation in the bulk of the wafer. Crystallographic defects can act as nucleation sites, and when defects are numerous in the bulk of the wafer, nucleation in this region will also be increased. All precipitates compete to capture impurities but only precipitates in the SD facilitate SDG. Precipitates in the bulk of the wafer reduce the number of mobile impurities which can be gettered by the SD precipitates. Thus the increased bulk nucleation may reduce the efficacy of the SDG process.

4.5.2 Low thermal budget processing

It has been seen that SDG requires some minimum thermal budget to be exceeded in order for it to be effective. This is the case if either a temporary, or stable SDG effect is to be seen, although the minimum thermal budget is different in these two cases. The hypothesised reasons for this are as follows:

During the SDG-anneal, precipitates in the bulk of the wafer are dissolved, releasing impurities which can then be gettered. When the thermal budget is low, the precipitates are less completely dissolved which has two direct effects. Firstly the fraction of impurities in solution after SDG-annealing is reduced, with more remaining within the precipitates. As only impurities in solution can be gettered, this reduced dissolution means less complete gettering is possible, see Figure 44, and more impurities are likely to remain in the wafer after the SDG process.

Secondly, a higher fraction of the precipitates will not fully dissolve, during the SDG-anneal, when the annealing process has a low thermal budget. These precipitates may be dissolved slowly for a number of reasons; the impurities may only diffuse slowly at the annealing temperature, the kinetics of impurity release may be slow, or the solution may become saturated before the precipitate has completely dissolved. If precipitates remain in the wafer after the SDG-anneal they can compete with precipitates that nucleate in the SD to capture impurities during cooling. As discussed, this reduces gettering to the SD and also means precipitates remain in the wafer after SDG. The presence of these residual precipitates are important for two reasons. Firstly they may be recombination active sites, reducing the lifetime of the wafer immediately after SDG. It is anticipated that this may only be a minor effect as the number of these precipitates would be small compared to the number of impurities in solution. Therefore the number of recombination events at these sites are also likely to be low. The second effect of these remaining precipitates is that they are a source of impurities which can be released into the wafer during further thermal processes such as PDG.

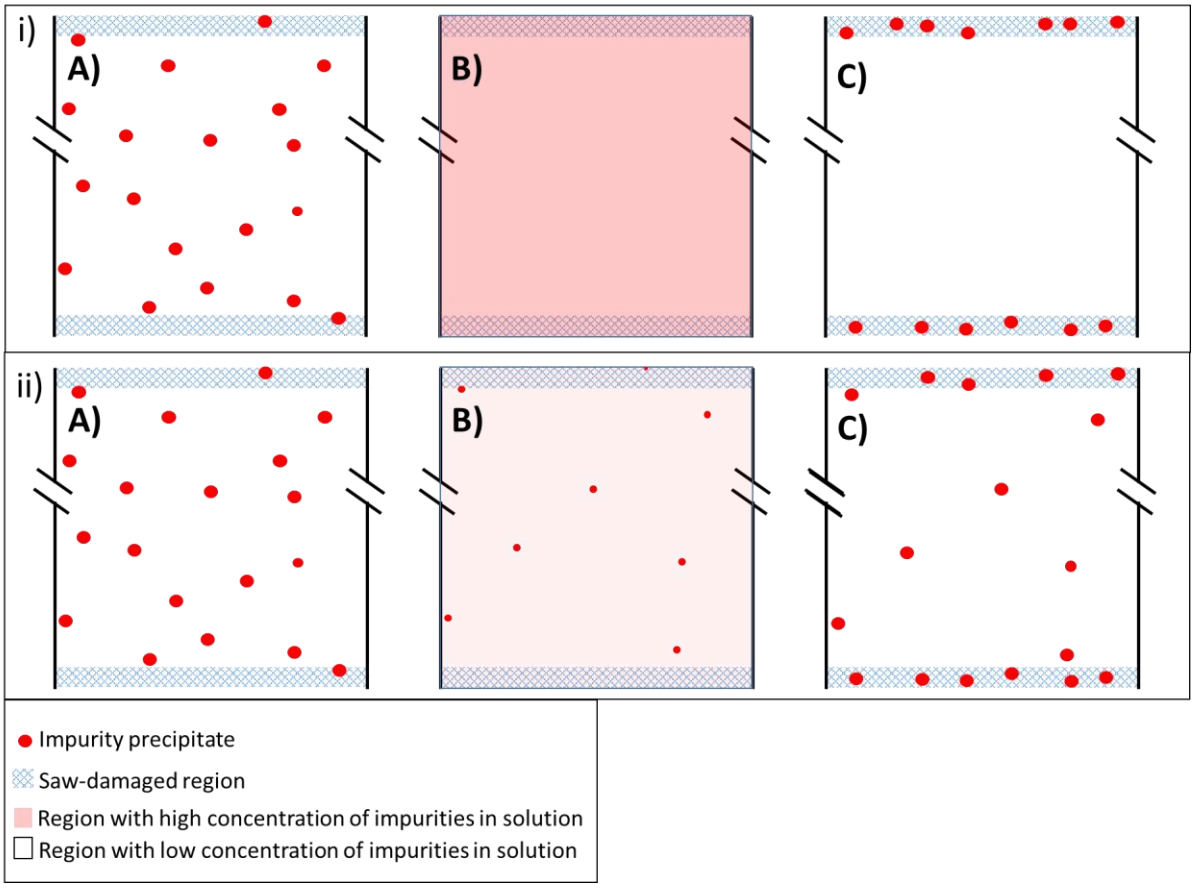


Figure 44. i). A schematic of the ideal SDG process, all precipitates are removed during the SDG-anneal and all precipitates form in the SD region. ii) is a schematic of the process when the SDG-anneal has too low a thermal budget. Precipitates remain after the SDG-anneal and the concentration of mobile impurities is consequently reduced. After processing precipitates remain in the bulk of the wafer. These can release impurities during further anneals, including during the PDG process. A), B) and C) are the wafer before processing, during the SDG-anneal, and after SDG respectively.

SDG may have a temporary effect if impurities are removed from solution, increasing the wafer lifetime, while a large fraction of impurities remain trapped within precipitates, where they remain a potential source of contamination, and can contaminate the wafer during any subsequent thermal process. Therefore, it is very important to ensure that the SDG-anneal causes comprehensive precipitate dissolution. This also explains why the SDG-anneals must have a higher thermal budget if a second gettering process is performed, see Figure 42 and Figure 43. It should also be noted that different types of precipitates will be removed under different conditions as solubility and diffusivity vary for different impurity types. For example, iron appears to be removed more easily than some other impurities; as suggested by the effective iron gettering seen in SDG samples even after further PDG processing, while minimal

lifetime improvement is seen in the same wafers, which implies that some other impurity has been less effectively gettered or accidentally added to the samples. In this work the SDG process was designed to maximise gettering of iron, but a more appropriate thermal process could be chosen to maximise gettering of other, potentially more important impurities. In addition, further optimisation of the SDG and PDG processing, including improving cleanroom cleanliness, may improve the results of the SDG process further.

4.5.3 High thermal budget saw damage gettering processing

Excessive SDG-annealing can be seen to reduce the lifetimes of wafers after SDG processing. There are two hypotheses which may explain this:

As discussed, high temperature annealing enables more complete precipitate dissolution. While this is required for SDG, it can also be detrimental. This is because some of the released impurities may not be fully gettered by the SD on cooling. This is not problematic if the impurities are subsequently gettered during PDG. However, slow diffusing impurities may be unable to diffuse to the wafer surfaces during the wafer processing. Instead they would become trapped in a supersaturated solution, where they could have a large impact of the wafer lifetime. This deleterious effect would be worse when more of these slow diffusing species are released from precipitates, and thus will be worse for wafers given higher thermal budget anneals. The total distance an impurity can diffuse during cooling can be estimated by finding the diffusion lengths for all times steps during the cooling profile for the impurity in question as follows:

4.5.1 $$\boldsymbol{L = \sqrt{\sum_{i=1}^{n} D(T)_i \times t_i}}$$

Where i is the cooling step number.

This characteristic diffusion length can be very low, for example it is only 2.83×10^{-9} cm for titanium when cooling from 980 ^{o}C.

The alternative mechanism is that the SD regions becomes less effective impurity sinks after high temperature annealing. Dislocations are high energy structures and as such it is energetically favourable if their total length is reduced. This can be achieved when two

dislocations with opposite Burger's vectors interact. When this happens, they annihilate each other leaving a more perfect crystal [114]. Dislocation annihilation is enhanced when the concentration of dislocations is increased, and thus the spacing between dislocations is reduced, and when the temperature of the material is increased. If dislocations are annihilated they will be unable to nucleate precipitates or capture impurities and the SD will getter less effectively for each dislocation pair destroyed. It is hypothesised that this dislocation annihilation occurs during the high temperature SDG-anneals and that this makes the SD less effective as a gettering centre.

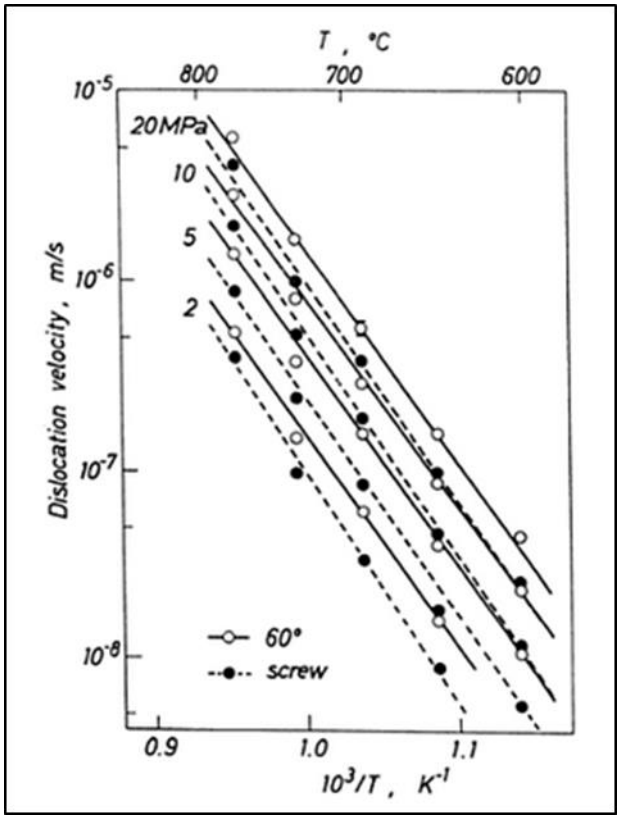


Figure 45. Dislocation velocity as a function of temperature and stress for high purity silicon. From [115]

It is possible that dislocation annihilation may occur at the higher temperatures used in this work. It has been seen that dislocations located within the bulk of silicon wafers can annihilate at temperatures exceeding 1170 ^{o}C [116]. While these temperatures are much higher than those used in this work, the dislocation density, and thus the forces between dislocations are much higher in the SD than in the bulk of a wafer. Dislocation densities of ~10^{4}-10^{6} cm^{-2} are common

in a dislocation rich mc-Si grain, versus 10^{9}-10^{11} cm^{-2} in the densest regions of the SD, calculated from [117]. In addition, it has been shown that dislocation cross slip, and thus annihilation is possible at ~990 ^{o}C[118] and dislocation annihilation at the annealing temperatures used in this work is thus probable. This would reduce the gettering capability of the SD region.

4.5.4 Industrial relevance

Discussions with Semih Senkader, an independent consultant based in the Norwegian PV industry who was previously employed by REC, have suggested that currently this process is not economically viable with solar grade silicon at its current, historically low, price.

SDG may be more usefully applied to UMG-Si, as this material is more heavily contaminated. Currently this contamination limits its industrial utilisation, and SDG may enable UMG-Si to overcome this obstacle. It is thus suggested that this would be a useful area for further work.

4.6 Conclusions and further work

It has been shown that SDG is a potentially beneficial technique which may enable impure wafers to be upgraded such that they can be re-introduced into cell processing lines. The efficacy of this process has been shown to be highly dependent on the thermal processing of the wafers. The optimal annealing temperature must be chosen correctly to maximise the stable effect of SDG processing. As SDG is designed to enhance the properties of industrially processed solar cells, the effects must be compatible with subsequent cell manufacturing processes. The most important of these steps, in the context of this work, is the emitter formation step (PDG process). This high temperature process can dissolve precipitates and thus is sensitive to the absolute concentration of impurities remaining in the wafer after SDG. Thus, to accurately evaluate the efficacy of SDG, it should be followed by a PDG process.. It is harder to design a successful SDG process when using the latter criterion, but this is more industrially relevant so must be considered. It has been seen that different impurities respond differently to a given SDG process. Some impurities such as iron may have been gettered effectively, whilst the wafer lifetime remains limited by other, slower diffusing, impurities.

It has also been shown that SDG is less effective when the underlying wafer has a high density of dislocations. This means that the fraction of wafers which can be recovered by using the SDG process will be higher from the bottom red zone than the top red zone as the former has a lower concentration of dislocations, see section1.4.2.

A number of additional experiments may be useful to further understand this process, and also to increase its industrial importance:

Firstly, it would be useful to analyse the concentrations of impurities within the SD, and to compare that to the concentrations within the bulk of the wafer. The absolute concentrations are important, so it is likely that a destructive technique such as inductively coupled plasma mass spectrometry (ICP-MS) [119] would be used as this is capable of measuring absolute impurity concentrations as low as tens of ppt [120].This would enable the fraction of impurities that were gettered to be measured, and the process adjusted to remove the most important impurities.

It could also be beneficial to adjust the cooling profile to optimise the gettering of an impurity with a different temperature dependence. This may be useful as the current cooling rate is designed to getter iron. It has been shown that iron does getter effectively, but it is not the lifetime limiting impurity in the wafers after a second gettering process.

It is also important to test if SDG remains a useful technique when applied to the most recent type of mc-Si. This material has smaller grains and fewer dislocations. It has been shown that crystallographic defects inhibit SDG but it is unclear which will have a more pronounced effect on SDG, the increased grain boundary length, or the reduced dislocation density.

It is also important to find if SDG can remove enough impurities from UMG-Si such that the resultant cell efficiencies are economically useful. It is possible that this will depend on the source of material as they will contain different concentrations of different impurity types, and SDG works more effectively on some impurities than it does on others.

5 Gas Phase Gettering

This chapter describes an investigation into the gettering of impurities into a gaseous medium. It will include a short literature review detailing previous studies of this technique, followed by a theoretical study of the limitations of gas phase gettering (GPG). This will include thermodynamic and kinetic calculations using two alternative gaseous gettering agents. Finally, a sample of results of GPG using chlorine as the gettering agent will be presented.

5.1 Introduction

In GPG, impurities react with the gaseous atmosphere to form volatile molecules. These are then drawn into the gas stream where they are permanently removed as shown in Figure 46. This form of gettering is therefore irreversible unlike those previously discussed in chapter 3. As the gettered impurities are removed from the system entirely, an equilibrium state between impurity gettering and release cannot be reached, therefore gettering can continue without saturation of the gettering centres. GPG has been trialled by the integrated circuit industry, where it is used during thermal oxidations. The gettering agents used include chlorine, trichloroethylene and hydrogen chloride [121], [122]. This form of GPG, combined with oxidations, reduces contamination of the wafers from external sources but does not actively remove impurities from the bulk of the wafer since the surface oxide very rapidly forms an effective diffusion barrier to bulk impurities. Hydrogen chloride (HCl) has been used during an oxidation free GPG process, designed to upgrade low quality silicon for solar applications [123][73]. Hample et al, exposed upgraded metallurgical silicon to a 2% HCl atmosphere at temperatures between 650 ^{o}C and 1300 ^{o}C for ten minutes. They found that the gettering of nickel was most effective at 650 ^{o}C, where the concentration was reduced by a factor of 7.8. However, it is not clear if these results can be transferred to gettering when using less heavily contaminated substrates. This may be challenging as it is probable that the removal of impurities from precipitates will be easier than from defected regions which trap impurities strongly. This will be particularly important when the reaction between the impurity and the

gettering agent is only weakly thermodynamically favourable. When this is the case, the energy required to remove the impurities from the traps will make the overall process resulting in the GPG of impurities less thermodynamically favourable. If this process ceases to be thermodynamically favourable it will not proceed, and GPG will be stopped.

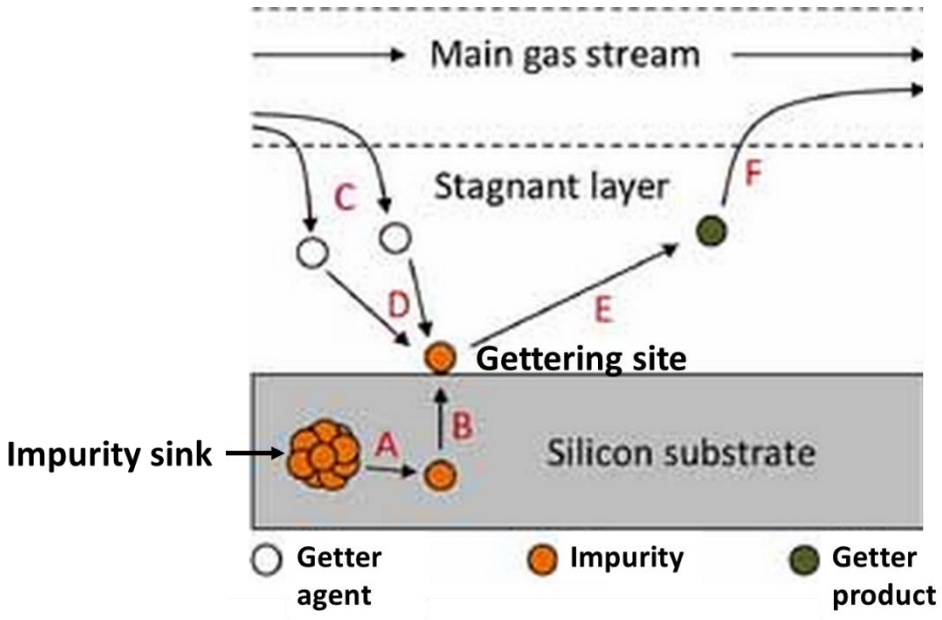


Figure 46. The processes which must be completed for GPG to proceed. A) Impurities are released from previous sinks, B) they diffuse to the surface of the wafer, C) the reactive gas diffuses and collides with the impurities, D) a reaction occurs, E) the impurity product is removed into the gas stream, and finally, F) the impurity is removed with the waste gases, leaving an upgraded wafer. Figure is modified from [73]

Figure 46 shows the processes which must occur for impurities to be gettered by the GPG process. Any of these could limit the net gettering rate. In all gettering techniques, the impurities must be released from any prior sinks (process A), and must then diffuse to the gettering site (process B), which in the case of GPG is the wafer surface. The gaseous gettering agent must also collide with the wafer surfaces, and react with the impurities, processes C) and D). The products of these reactions must then enter the gas stream, where they are removed from the process chamber with the other waste gases, processes E) and F).

The stages described in Figure 46 will be discussed in sections 5.3 to 5.5. In this work each potential factor limiting GPG will be treated independently so that the factors which may limit GPG efficacy can be assessed. This theoretical approach will cover the gettering of a number of

different impurities using either hydrogen chloride (HCl) or chlorine (Cl_2) as gettering agents. It will be shown that when oxygen is present during GPG, and when HCl rather than Cl_2 is used as the gettering agent, the process efficacy will be limited. As will be demonstrated below, it is anticipated that GPG efficacy will be maximised by using a chlorine in an inert atmosphere, consequently, this atmosphere will be used for the experimental section of this work. It is believed that GPG using an inert gas based atmosphere, containing Cl_2 has not been attempted prior to this work.

5.2 Surface etching during GPG

One potential disadvantage of GPG is the possibility of surface etching by the gettering agent. These agents must strongly bind to the metallic impurities so they can be removed. However, these highly reactive gettering agents may also react with the silicon, etching it. Etching has previously been observed when silicon was exposed to Cl_2, with irregular etch pits formed when the concentration of Cl_2 exceeded 0.6% [124]. Topographical features such as these would be highly detrimental to the integrated circuit (IC) industry as the active regions of these devices are located at the surface of the substrates, and so are highly vulnerable to any defects in these regions. Therefore, the IC industry has avoided direct exposure of bare silicon wafers to chlorine. However, etching of the silicon is less problematic for solar applications. This is because the as-sawn silicon contains a ~ 10 μm thick saw damaged region which must be removed before the final cell can be produced. Consequently if the GPG process removes some or all of this layer, but not too much of the underlying undamaged silicon, it is not expected to be problematic. This etching may even be beneficial if the uneven surface generated reduces the reflectivity of the silicon, increasing the absorption of light.

It has been shown that exposing wafers to gettering agents such as chlorine during an oxidation process is beneficial for the IC industry. The growing oxides prevent etching enabling GPG's use without risking the generation of topographical features. Simultaneously, the gettering agents react with contaminates found on the wafer surfaces. This prevents accidental contamination of

the wafers by any extrinsic sources during the high temperature oxidation, and results in a higher quality oxide being generated [121] [125] [122]. However, impurities must diffuse through the growing oxide before any as-cast impurities can be gettered.

5.3 Diffusion limited gettering

Impurities must diffuse from within the bulk of wafers to the solid/gas interface to enable GPG. If the silicon is coated in a layer, such as an oxide, the impurities must diffuse through both the wafer and this layer before they can be gettered. The flux of impurities diffusing through either the silicon, or the coating layers, can therefore impose an upper limit upon GPG efficacy.

5.3.1 Oxides as diffusion barriers

As discussed in section 5.2, thermal oxides are a barrier which prevent gettering agents etching the silicon. However, these barrier layers can also adversely affect the GPG of bulk impurities as diffusion through these layers can be slow. The diffusion co-efficient of many metals is very low within thermally oxidised silicon. For example, the diffusion coefficient for iron in SiO_2 is $\approx 4 \times 10^{-14}$ cm^2s^{-1} at 1000 ^oC, which contrasts with a diffusion co-efficient of $\approx 3 \times 10^{-6}$ cm^2s^{-1} in silicon at the same temperature. As shown in 5.3.1 to 5.3.3, this means that the flux of impurities through thin oxide layers is very low even at high temperatures. This flux can therefore limit GPG efficacy when an oxide is present on the silicon surfaces.

From Fick's first law of diffusion:

5.3.1 $$J = D\frac{dc}{dx}$$

Where J is the flux, D is the impurity diffusivity in the oxide, c is the impurity concentration and x is distance through the oxide.

If the oxide is assumed to be only 1 nm thick, and the concentration of iron at the gas/oxide interface is assumed to be zero, the steady state impurity flux at 1000 ^oC becomes:

5.3.2 $$J = 4 \times 10^{-14} \times \frac{[Fe_{Si}]}{10^{-7}} = 4 \times 10^{-7} \times [Fe_{Si}] cm^{-3} s^{-1}$$

Where [Fe_{Si}] is the concentration of iron in the silicon. The change in iron concentration in the wafer can be calculated by dividing the net flux by half the wafer thickness, as there are two interfaces where this gettering can occur. Using this flux and a wafer thickness of 200 μm gives a reduction in iron concentration of:

5.3.3 $$\frac{4 \times 10^{-7} \times [Fe_{Si}]}{10^{-2}} = 4 \times 10^{-5} \times [Fe_{Si}] cm^{-3} s^{-1}$$

According to this result, reducing the iron concentration in the silicon to 3% of its original concentration would take in excess of 24 hours, even assuming that there were no other rate limiting factors. This rate is too slow to be industrially applicable, particularly if higher purities are required. This therefore suggests that dual oxidation and GPG is inappropriate as a technique for gettering bulk impurities, such as those present in mc-Si or UMG-Si. The rest of this work will therefore focus on GPG where the silicon is directly exposed to the gettering agent.

5.3.2 Bulk diffusion limited GPG

GPG requires the macroscopic diffusion of impurities from the bulk of the wafer to its surfaces, and as such the process efficacy may become limited by bulk diffusion. Diffusion is highly dependent on the gettering temperature and the type of impurity, for example the diffusivity of titanium changes from 2.3×10^{-11} $cm^2 s^{-1}$ at 1000 °C [126] to 1.47×10^{-10} $cm^2 s^{-1}$ at 1200 °C. Figure 47. shows the relationship between diffusivity in silicon, and temperature for a range of transition metals. The data used to generate this figure is from [9], [127], [19]–[21]. It is possible to calculate how diffusivity will limit gaseous gettering if it is assumed to be the primary rate limiting factor. This requires solving Fick's second law assuming that diffusivity is not concentration dependent, which is valid for most metals in silicon:

5.3.4 $$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2}$$

Where *t* is diffusion time and *x* is the distance away from one of the wafer surfaces

Fick's second law can be solved if appropriate starting conditions are chosen. In this case, the initial impurity profile is assumed to be uniform. In addition, the surface impurity concentration is assumed to be zero. Hence, the initial impurity profile is a square wave which can be modelled as a Fourier series. This wave can be modelled as a square wave in contact with virtual wafers, which have initial impurity concentrations of the same magnitude, but opposite sign, to the concentration initially present in the actual wafer. This means the impurity concentration at the edges remains zero at all times. If the wafer is taken to be *d* thick, with a starting concentration of C_0, its initial concentration profile can be modelled as;

5.3.5 $$C(x) = C_o \sum_{n=0}^{\infty} \frac{4}{(2n+1)\pi} \sin\{(2n+1)\frac{\pi x}{d}\}$$

Each term can then be treated individually when calculating how the concentration profile changes. This produces equation 5.3.6 which describes the time dependent concentration profile.

5.3.6 $$C(x,t) = C_o \sum_{n=0}^{\infty} \frac{4}{(2n+1)\pi} \sin\{(2n+1)\frac{\pi x}{d}\} \times \exp\{-(2n+1)^2 \frac{\pi^2 D}{d^2} t\}$$

The higher terms decay rapidly, which is seen in the sample as a rapid conversion of the profile into a sine wave. Consequently, the system can be modelled as a simple harmonic at longer timescales where:

5.3.7 $$t > \frac{d^2}{D}$$

When this is the case the system can be modelled as below equation 5.3.8 can then be integrated with respect to *x* between 0 and *d* to find the total impurity concentration remaining after time *t*.

5.3.8 $$C_{total}(t) = \frac{4}{\pi} \exp(-\frac{\pi^2 D}{L^2} t) \int_0^d \sin\left(\frac{\pi x}{d}\right) dx$$

So

5.3.9 $$C_{total}(t) = -\frac{4}{\pi} C_o \exp(-\frac{\pi^2 D}{d^2} t) \frac{d}{\pi} [\cos\left(\frac{\pi x}{d}\right)]_0^d$$

And

5.3.10 $$C_{total}(t) = \frac{8d}{\pi^2} C_o \exp(-\frac{\pi^2 D}{d^2} t)$$

Therefore, the fraction of impurities remaining after some gettering time *t* is:

5.3.11 $$C_{remaining} = \frac{8}{\pi^2} C_o \exp(-\frac{\pi^2 D}{d^2} t)$$

If the initial concentration is set to some arbitrary level such as 1, and diffusivity data is taken from the literature [126] [128] [127] [129], the fraction of impurities remaining after a gettering time *t* can be calculated. This is detailed in Figure 48.

Figure 48 shows that diffusion is unlikely to limit GPG for fast diffusing species such as nickel. Consequently, the limited nickel gettering observed by Hample et al [73] is not caused by slow impurity diffusion and GPG in this case must be limited by some other effect, see section 5.5.2. The gettering of vanadium may be partially limited by long range diffusion, as a 30 minute gettering process will leave 1% of the initial vanadium concentration in the wafer assuming that there are no other factors affecting the gettering process. As cobalt diffusion is highly temperature dependent with an activation energy of 2.8 eV [129] GPG will not be limited by bulk diffusion at temperatures exceeding 1000 ^{o}C but may be diffusion limited below 900 ^{o}C. Finally, titanium diffuses sufficiently slowly that GPG is likely to be ineffective as long as the silicon remains in a solid state. These results will be used later in this chapter to understand which conditions are likely to be most effective for GPG when using different reactants.

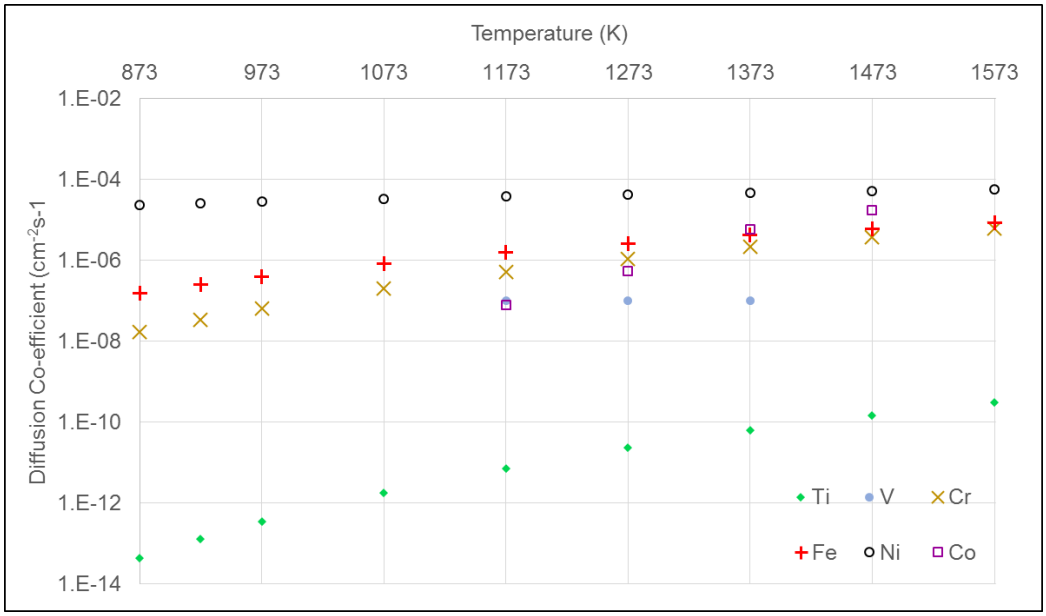


Figure 47. The relationship between diffusivity and temperature for a range of transition metals. Data from [9], [19]–[21]. Due to its dependence of doping level, data is not presented for copper, however, it is a very rapid diffuser at all doping levels [127].

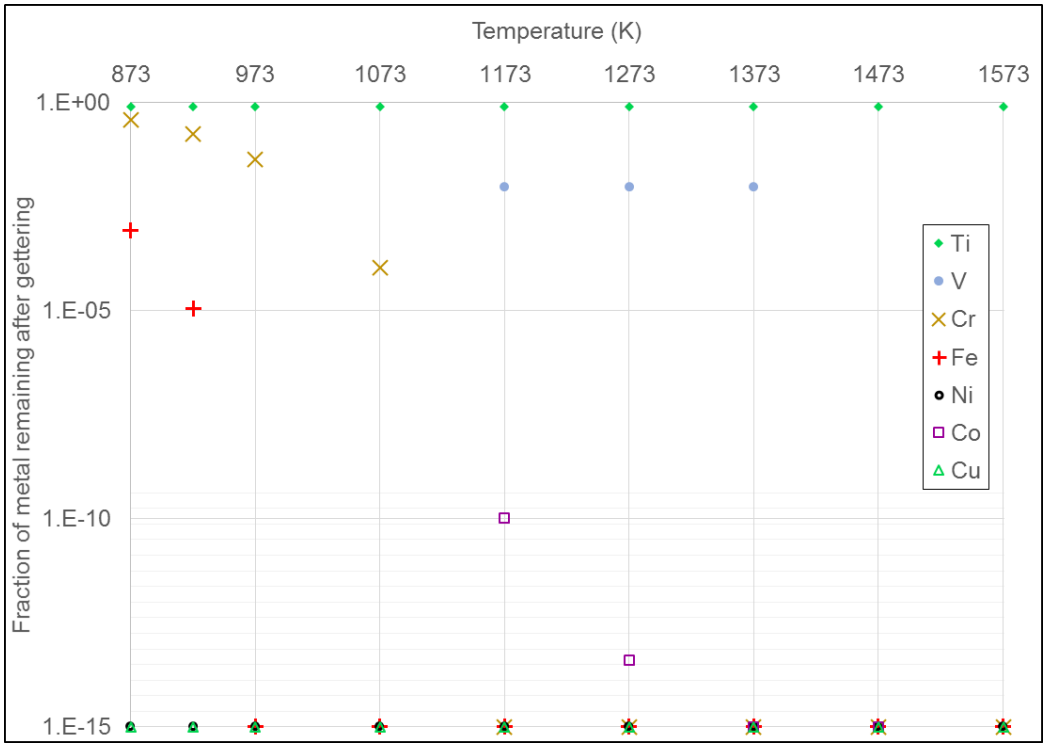


Figure 48. The fraction of impurities remaining in a silicon wafer after a hypothetical gettering process where the surface is a perfect gettering site. The gettering process lasts for 30 minutes at the specified temperature, and the wafer is 200 µm thick. Diffusivity data from [126] [128] [129] [127]**. Values below 10^{-15} are changed to a fixed amount as the precise values are unimportant as the gettering of these metals will not be diffusion limited. Only an insignificant amount of titanium was removed for the temperature range considered..**

5.4 Gettering limited by gas supply

As previously shown in Figure 46, the gettering agent must reach the silicon surfaces before a reaction can occur. In this section the collision rate between the gettering agent and the silicon will be modelled to find if the supply of gas molecules to the silicon surface could limit the gettering rate. A number of assumptions are made to test if gas supply alone could be a significant factor limiting gettering. These assumption are that:

- The diffusion of impurity atoms to the wafer surface is infinitely fast.
- There are no energetically favourable sites for the location of impurities within the wafer.
- The above two assumptions mean that it is assumed that the distribution of impurities within the wafer is uniform at all times during the gettering process. It is unlikely that both of these will be valid in many systems as discussed in section 5.3.
- The gettering agent has the same probability of colliding with individual impurities located at the wafer surface as it does with individual silicon atoms.
- The reaction between impurity atoms and the gettering species is "perfect", meaning that each collision results in a gettering reaction. This assumption will not be valid when the reaction stoichiometry between the impurity and the gaseous gettering species is not one to one. This will also not be correct when there is a significant energy barrier which must be overcome before a reaction can occur, see section 5.5.1.
- Collisions between impurity atoms and gettering agents result in the formation of stable, intermediate products if one to one reaction stoichiometry is not observed. Additional collisions change the stoichiometry of these products until a stable gettering product is formed and released.
- Collisions between the intermediate states and gettering molecules are as likely as collisions between gettering molecules and any other surface atom.
- The above three assumptions mean that a small correction factor is the only addition required to make the below model valid for reactions where the stoichiometry is not one to one. These assumptions may not be valid, particularly when the reaction stoichiometry significantly deviates from one to one.
- The distribution of gettering agents within the gas is uniform, and a stagnant layer which becomes depleted if the gettering agent does not form next to the wafer.
- All other kinetic theory of gasses assumptions are held to be valid [130]:
    - There are a large number of gas molecules, which have a large spacing: size ratio
    - Molecules move randomly with a speed distribution which does not change

- The only interaction between species is elastic collisions
- Newton's laws of motion are obeyed.

As described by the kinetic theory of gases, the collision rate, *F*, between the silicon and the gas is:

5.4.1 $$\boldsymbol{F = \frac{n}{4}\sqrt{\frac{8kT}{\pi m}}}$$

Where

F = number of collisions per unit time and area
m = mass of particle = molecular mass / Avogadro constant
n = number density of gaseous molecules in question, as determined by:

5.4.2 $$\boldsymbol{n = \frac{P}{kT}}$$

Where

P =the partial pressure of the molecule in question

Only a fraction of these collisions are with impurity atoms, assumed to be Fe for the remainder of this analysis, it should be noted that the same methodology could be directly used for any other impurity. This fraction, {*Fe*}, is approximately the number density of impurity atoms divided by the number density of bulk silicon atoms, assuming that the impurities are homogeneously distributed within the wafer..

5.4.3 $$\boldsymbol{\{Fe\} = \frac{[Fe]}{[Si]} = \frac{[Fe]}{5\times10^{22}cm^{-3}}}$$

Where [*Fe*] is the concentration of impurities in the silicon in the wafer and [Si] is the concentration of atoms in silicon.

The number of gettering agent/impurity collisions is the product of number of collisions with the surface and the fraction of these which involve impurities:

5.4.4 $$\boldsymbol{F_{Fe} = \{Fe\} \times F}$$

If it is assumed that:

- the gaseous species is molecular chlorine, as will be used in this work (m=71/A_v)
- processing is done at atmospheric pressure, with a concentration of 2% Cl_2 so P=10^3 Pa
- the processing temperature is 1200K

Then the collision rate *F* is 2.98 × 10^{19} $cm^{-2}s^{-1}$, and the number of gas/impurity collisions is [Fe]x6.0 × $10^{-4}$$cms^{-1}$.

The total number of impurities to be gettered at each surface, is the impurity concentration multiplied by the half thickness of the wafer, as gettering occurs at both sides. The wafer can be taken to be approximately 200 μm thick, as is standard for a solar wafer. Therefore the number of impurities available to be gettered to each side is $[Fe_{initial}]$. 10^{-2} cm. The initial rate of change of impurity concentration (R_i) is therefore, $[Fe]$. 6.0×10^{-2} s^{-1}. However, this will decrease with time as the concentration of impurities remaining in the wafer falls. After some period of time t, the concentration of impurities remaining ($[Fe_t]$) can be found from equation *5.4.5*.

5.4.5 $$[Fe_t] = [Fe_0]exp(\frac{-t}{t_0})$$

t_0 can be found by re-arranging this equation and substituting in a very low value for t and calculating $[Fe_t]$ at this time. This then enables t_0 to be calculated; see equation 5.4.6.

5.4.6 $$t_0 = \frac{-dt}{ln(1-R_i dt)}$$

Therefore, $t_0 \approx 16.7$ s, this means the concentration of impurities at some time t is;

5.4.7 $$[Fe_t] = [Fe_0]exp(\frac{-t}{16.7})$$

If each of these collisions resulted in a gettering reaction the overall process would rapidly remove all impurities. For example after a gettering processes lasting one and ten minutes respectively, the impurity concentration would have fallen to 2.7×10^{-2} and 2.5×10^{-16} of its original value. This assumes that there are no other factors limiting gettering. Therefore, the supply of gas to the silicon surfaces is unlikely to be the primary factor limiting GPG if all of the assumptions made above are valid.

5.5 Reaction limited GPG

For GPG to be effective, the metal/gettering agent collisions have to result in reactions which form volatile compounds. These reactions can be prevented by either kinetic or thermodynamic limitations as discussed below:

5.5.1 Kinetic limitations

The gettering process may be limited by the chemical reaction between the impurities and the gettering agent. The rate of these reactions is typically highly temperature dependent with an Arrhenius relationship, see equation 5.5.1.

5.5.1 $$V = V_0 exp(\frac{-Ea}{kT})$$

Where V is the reaction rate, V_0 is a pre-factor, and E_a is the activation energy which must be overcome to enable the reaction to occur.

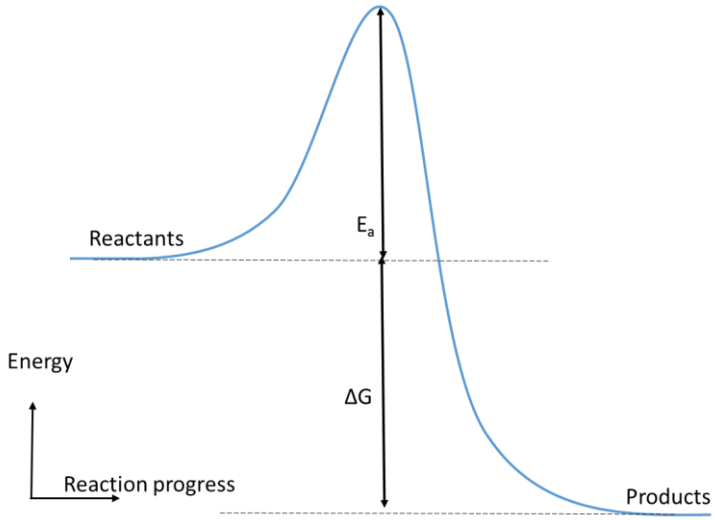


Figure 49. The reaction energy path of a typical reaction with the activation energy which must be overcome before the reaction can occur.

An activation energy exists as there is an intermediate state which the reacting species must enter before a reaction can occur. This intermediate state has a higher energy than that of either the products or the reactants. It may be associated with the breaking or straining of chemical bonds, prior to the relaxation of the system when the products are formed, see Figure 49. The existence of this activation energy has three significant implications. Firstly, it will ensure that not all impurity/ gettering agent collisions result in reactions, and hence it will slow the gettering process. Secondly, it means that these reactions should be significantly accelerated at higher temperatures where more thermal energy is present to overcome the activation energy. Thirdly, different gettering agents and impurities will have different activation energies and so different reaction rates.

5.5.2 Thermodynamic limitations

5.5.2.1 Reaction spontaneity

Although reaction kinetics are always enhanced at higher temperatures this is not always true of the reaction thermodynamics. Every product and reactant involved in a chemical process will have an associated enthalpy (H) and entropy (S), which combine to give a Gibbs energy, equation 5.5.2. The more negative this Gibbs energy, the more stable the species is.

5.5.2 $$\boldsymbol{G = H - TS}$$

When a reaction takes place the enthalpies and entropies of the reactants are replaced by those of the products, leading to a change in the Gibbs energy. If $\Delta G_{reaction}$ is negative the reaction should be spontaneous, and if $\Delta G_{reaction}$ is positive the reaction will not be spontaneous.

5.5.3 $$\boldsymbol{\Delta G_{reaction} = H_{products} - TS_{products} - (H_{reactants} - TS_{reactants})}$$

Alternatively,

5.5.4 $$\boldsymbol{\Delta G_{reaction} = G_{products} - G_{reactants}}$$

If the entropy and enthalpy of both the reactants and products are known, it is possible to calculate if the reaction will be spontaneous, and also to work out the energetic gain if it proceeds ($\Delta G_{reaction}$). It should however be noted that these calculations assume both reactants and products are in their standard states, ie pure solids and gases at 1 atm of pressure. It is possible to apply this methodology to gettering reactions using either pure metals or metal silicides as reactants, and also to use a range of different gettering agents as long as thermodynamic data can be obtained, see section 5.5.3.

5.5.2.2 Equilibrium position in non-spontaneous reactions

All chemical reactions are to some degree reversible, and the reaction energy calculated as above can be used to identify the relative concentrations of reactants and products when the reaction is in equilibrium. More negative Gibbs energies of reaction will be associated with an equilibrium position which has a higher fraction of reactants than products.

In the case of GPG, products which enter the gas stream are continuously removed, and gaseous reactants are replenished by the gas stream. This means that the system cannot reach its

equilibrium position, and instead will continue to form products to replace those which are extracted by the gas stream.

The above argument suggests that eventually all impurities will be extracted by the GPG process. However, this may occur over an unreasonably long timescale. This is because when reaction energy is highly positive, the equilibrium concentration of products will be very small. This concentration is the maximum concentration of impurities which are available to be extracted by the gas stream. As such, the gas extraction will only remove impurities at a very slow rate, and the gettering process will be very slow. By contrast, a highly negative reaction energy, will potentially result in high concentrations of impurity products forming and so the gettering will be promoted, assuming the reaction kinetics are favourable.

5.5.2.3 Gettering product removal

It is important that the products of the GPG reaction can be removed, and also that they do not prevent further reaction progress. This is trivially achieved if the products are fully gaseous at the reaction temperature, as these products will be removed by the gas stream. Condensed matter products can also be removed in the gas stream if they have a high vapour pressure at the process temperature. This means they will readily enter the gas and be removed.

If the products do not enter the gaseous phase they will deposit on the wafer surfaces. These can then be removed by a subsequent wet chemical processes. However, the presence of these products at the wafer surfaces could inhibit further GPG if they acted as a diffusion barrier to other impurities. These impurities would then by unable to diffuse such that they were exposed to the gaseous gettering agent, and so they will not be gettered. However, as is shown in the following, the impurity concentrations in mc-Si wafers are sufficiently low that at most only a fraction of a monolayer of coverage would be produced and so GPG would not be inhibited. Since there are $\sim 1.4 \times 10^{15}$ cm^{-2} atoms at the silicon surface. If the wafer is 200 μm thick, monolayer coverage of products will only form if the concentration of impurities removed from the bulk to the surfaces exceeds 1.4×10^{17} cm^{-3}. This concentration is higher than typical

impurity concentrations in mc-Si which are typically less than 5×10^{16} cm^{-3} for transition metal impurities [131]. Additionally, the impurities may cluster reducing the area coverage further. While, silicon tetrachloride may also form during this process, it is unlikely to form a passivating layer as it has a boiling point <100 ^{o}C [132] and so will not form a protective layer. Consequently it is not expected that the GPG process will be prevented by the formation of impurity products.

If the GPG process produces products which are not removed by the gas stream, they can be removed during further wet chemical processing, assuming that they are soluble.

5.5.2.4 Thermodynamic data

The majority of thermodynamic data used in this work was found within the databooks on the National Institute of Standards and Technology website (NIST) [132]. It should be noted that this only gives information at a small number of temperatures and so data must sometimes be interpolated, as shown in Figure 50. This was deemed to be justifiable due to the very accurate trends shown in the data. However, data extrapolation, is not always justifiable as the material may change state, leading to deviations in the energies associated with the material in question.

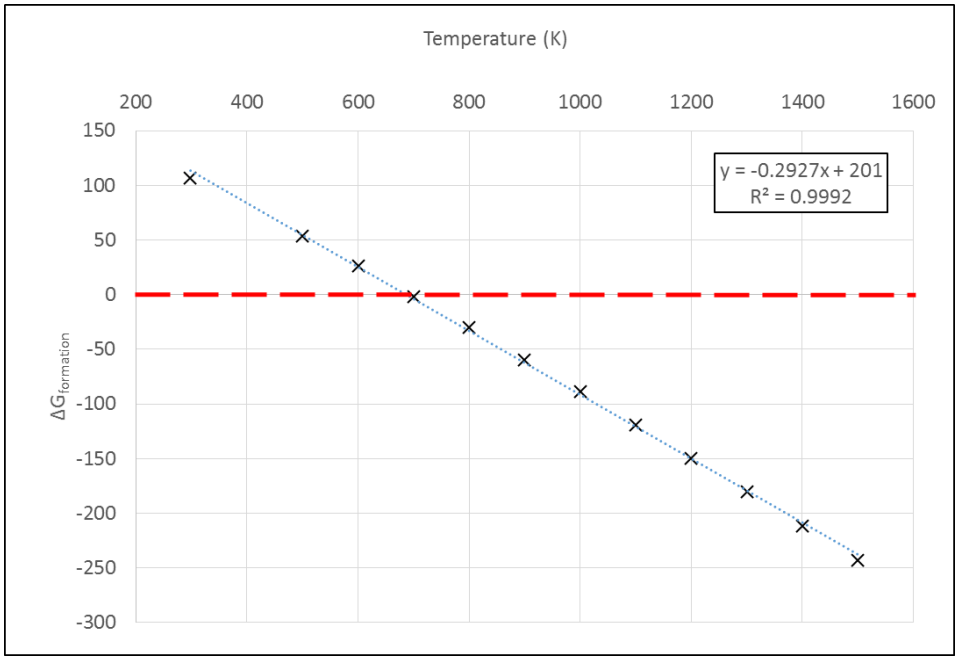


Figure 50. The Gibbs energy of formation of NiCl. The R^2 value shows there is good justification for data interpolation. From [132]

Some information is not available from these sources, in particular regarding the formation energies of metal silicides. In these instances it is typical for the only information available to be the enthalpy of formation at a specific temperature, and the heat capacity (C_p) at a range of temperatures. It is assumed that the entropy of formation is negligible as these are solid phases. The Gibbs energy is therefore simply the enthalpy. This can be calculated at a range of temperatures by summing the enthalpy of formation at a known temperature, and the energy required to heat this phase to the desired temperature, as determined by the heat capacity. Therefore:

5.5.5 $$\boldsymbol{G = H_{298} + \int_{298}^{T} H(T)\, dT = H_{298} + \int_{298}^{T} C_p(T) dT}$$

The heat capacity is often quoted in the form $C_p=\alpha+\beta T+\gamma T^{2}+\delta T^{-2}$

Therefore

5.5.6 $$\boldsymbol{G = H_{298} + \alpha(T - 298) + \frac{\beta}{2}\left(T^2 + 298^2\right) + \frac{\gamma}{3}\left(T^3 - 298^3\right) - \delta\left(T^{-1} - 298^{-1}\right)}$$

5.5.3 Gettering energetics

As discussed, it is possible to use thermodynamic data to calculate the spontaneity of a process at a range of different temperatures. Any reaction with a negative reaction energy will be spontaneous. The reaction energies for a series of reactions have been calculated and are shown in Figure 51and Figure 52.

Some of the transition metals evaluated may form multiple stable chlorides. For example iron can form both a dichloride and a trichloride. For simplicity, only the form which has the most negative reaction energy is shown, unless the relative stability changes depending on process temperature, where both reactions are plotted. The impurities can exist in either a metallic, or metal silicide phase, and the reaction energies associated with each of these potential reactants are plotted in Figure 51and Figure 52. If it is assumed that the more stable of these two phases is present, before GPG begins, then the GPG reaction must involve this more stable potential reactant. This may make the overall reaction energetics less favourable.

Knowing which reactants are initially present is very important for nickel gettering. When using HCl as the gettering agent, as done by Hample et al [133], it can be seen that a reaction between HCl and nickel silicide is possible at all temperatures, see Figure 51. However, at temperatures of 600K and above the silicide is no longer the most stable form, and the reaction between the metal and HCl must be considered. This reaction is spontaneous at low temperatures, but ceases to be so at ~820K. Research by Hample et al [73] suggests that HCl can be used to getter nickel at temperatures exceeding 650 ^{o}C (923K), even though the gettering reaction is not spontaneous.

This may happen because the reaction will have an equilibrium state which will have a small concentration of nickel chloride present. This chloride has a moderate vapour pressure at the temperatures in question (~100 Pa at 662 ^{o}C [134], [135]). The impurities which enter the gas stream can subsequently be removed, enabling the forward reaction to proceed, see section 5.5.2.2.

As this reaction is not spontaneous, it will only produce a low concentration of nickel chloride, and the reaction will consequently be slow. In addition, the reaction energetics will become increasingly unfavourable at higher temperature, as indicated by the positive slope in Figure 51. Therefore, the gettering equilibria will become less favourable, and the process will be slower at higher temperatures. This is in agreement with the data collected for nickel gettering using HCl [73].

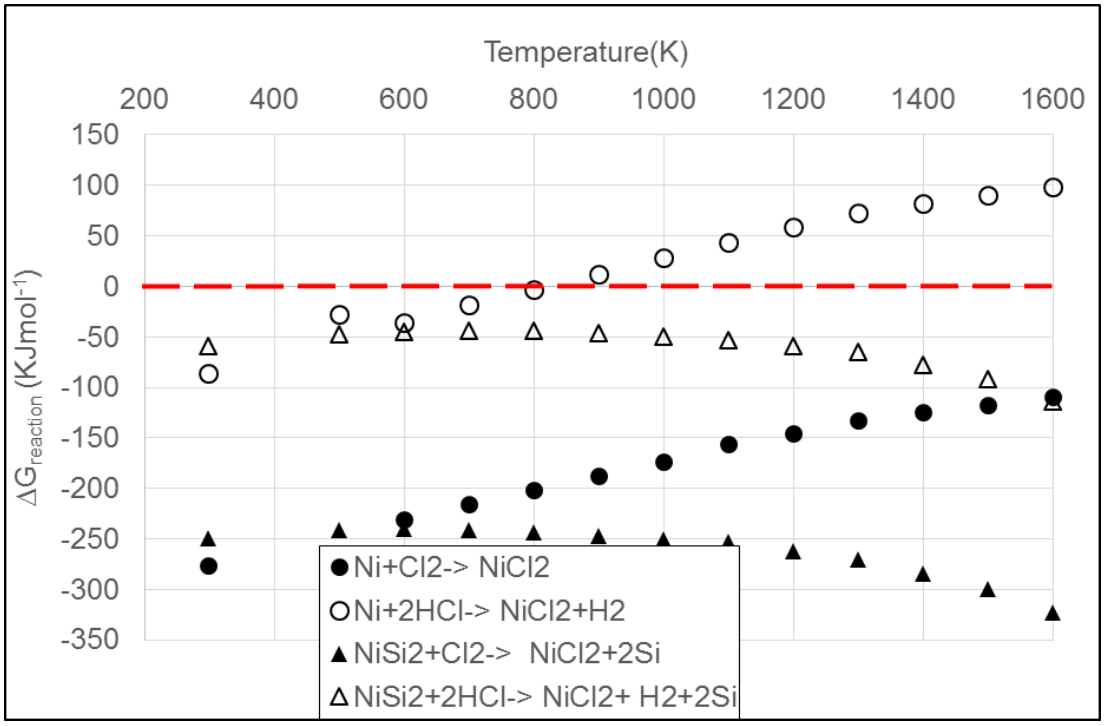


Figure 51. Thermodynamic data associated with the GPG reactions between nickel in various states and chlorine based molecules. The reactions with molecular chlorine can be seen to be the most energetically favourable reactions.

The GPG of nickel using molecular chlorine is expected to be very different to that using HCl. The reaction energetics are significantly more favourable when using chlorine (at 1000K, $\Delta G_{reaction}$ is -173 KJmol^{-1} between the most stable form of nickel and Cl_2, relative to a $\Delta G_{reaction}$ of +28 KJmol^{-1} when considering the reaction with HCl. In addition, the Cl_2 based reaction is predicted to be spontaneous over all of the temperatures considered in this work. It is therefore strongly expected that the gettering process will be significantly more effective when using Cl_2 as the gettering agent. It is believed that this is the first work to use chlorine in an inert atmosphere to getter impurities from solid silicon. As such, it is anticipated that this gettering process will be more effective than other gas phase gettering processes.

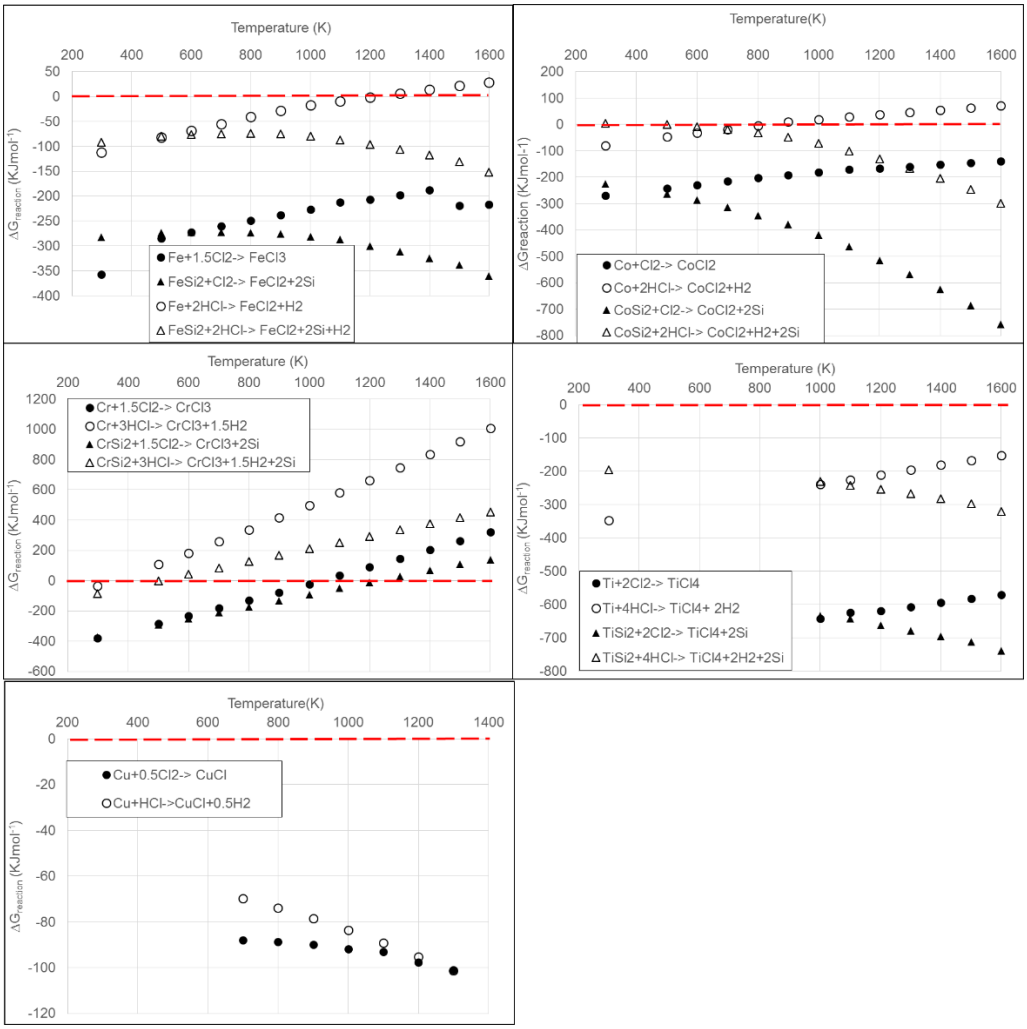


Figure 52. Thermodynamic data associated with the GPG reactions between different metals, both in their pure state and in silicides, and chlorine based molecules. The metals are iron (top left), cobalt (top right), chromium (middle left), titanium (middle right), and copper (bottom left). Energetic data on the silicides of copper could not be found so calculations involving this species could not be carried out.

The methodology used to understand GPG of nickel can be applied to other metals and broader conclusions can be drawn. One of the most important conclusions is the importance of choosing the correct gettering agent. Figure 51 and Figure 52 demonstrate that the energetics of the gettering process are strongly enhanced when using Cl_2 rather than HCl as the gettering agent. This is true when comparing all like for like reactions evaluated in this work. Additionally, the temperature at which the gettering process ceases to be spontaneous will be higher when using an atmosphere containing Cl_2, (for example no temperature threshold was observed for reactions involving iron and Cl_2 vs a threshold of ~1200 K between HCl and iron. Additionally, the maximum temperature for a spontaneous reaction with chromium was ~1030 K for Cl_2 vs ~370 K HCl).

The above results indicated that Cl_2 based gettering will be more effective than HCl gettering. As the reaction remains spontaneous at higher temperatures, when using Cl_2, effective gettering can still occur at these higher temperatures. This has three very important effects. Firstly, it will increase the diffusion rates of the impurities, which will improve their gettering rate, see section 5.3. Secondly, at these high temperatures fewer impurities will remain within precipitates. This means a higher fraction of the total impurity concentration can be gettered. As discussed in chapter 3, this is a very significant benefit, which may make GPG using Cl_2 more effective then HCl based GPG as well and many, if not all, conventional gettering processes. Thirdly, the higher temperatures possible when using Cl_2 may improve the reaction kinetics, enhancing the gettering rate. As a result of these factors Cl_2 will be used at the gettering agent for this work.

Figure 51 and Figure 52 also demonstrate that the reaction energetics, and the maximum temperature where the reaction is spontaneous is strongly affected by the impurity to be gettered. For example, the gettering of copper is always expected to be spontaneous, while the reaction with chromium ceases to be spontaneous at temperatures above 1000 K even when using Cl_2. It is expected that the optimal gettering temperature will be close to the spontaneous/ not spontaneous threshold temperature. This temperature will enhance all of the kinetic aspects

of the process without causing the process to be energetically unfavourable. This means that the optimal gettering temperature will vary depending on the impurity which is to be gettered. This information can be combined with diffusional information from section 5.3.2 to predict how effective the GPG process will be for each impurity type. Table 6shows the fraction of impurities remaining after a thirty minute gettering process, carried out at the threshold temperature where GPG becomes spontaneous. This assumes that at these temperatures, bulk diffusion is the only factor limiting gettering.

5.5.3.1 Gettering evaluation

	Maximum temperature for gettering spontaneity (T_{max}) (K), from Figure 51 and Figure 52		Fraction of metal remaining after diffusion limited GPG at T_{max} from Figure 48		Approximate vapour pressure of metal chloride at T_{max} (Pa) [135]	
Metal	HCl	Cl_2	HCl	Cl_2	HCl	Cl_2
Ni	820	1687	$<<10^{-20}$	$<<10^{-20}$	~10	$\sim10^5$
Fe	1210	1687	$<<10^{-20}$	$<<10^{-20}$	$\sim10^5$	gas
Co	370	1687	~ 0.2 (extrapolation)	$<<10^{-20}$	$<10^4$	gas
Cr	800	1030	~ 1	$<<10^{-20}$	Data unavailable	gas
Cu	1687	1687	$<<10^{-20}$	$<<10^{-20}$	$\sim10^5$	$\sim 10^5$
Ti	1687	1687	~ 1	~ 1	gas	gas

Table 6. A summary of the data regarding the potential effectiveness of GPG for different metals using different gettering agents. For each metal/ gettering agent combination a value T_{max} is stated, this is the lowest of the maximum temperature where the process is spontaneous, and the melting point of silicon. The fraction of metal remaining after a 30 minute gettering process at this temperature is also given. This assumes that the gettering reaction is perfect and so the concentration of impurities at the surface is zero. Finally, the vapour pressure above the metal chloride is given at the maximum temperature for a spontaneous gettering process.

Table 6 shows that GPG should be effective for the removal of nickel, iron, and copper when using either Cl_2 or HCl as the gettering agent. It also shows that cobalt will only be effectively

gettered when using a chlorine atmosphere, and finally, titanium is unlikely to be gettered effectively due to its very low diffusivity.

5.5.3.2 Etching reactions

Energetic arguments can be used to understand the etching of silicon by HCl and Cl_2. This is presented in Figure 53. This shows that while Cl_2 reacts more readily than HCl, both etching reactions are spontaneous at all temperatures of interest. There is some evidence from the literature that HCl only weakly etches silicon at temperatures <700 ^{0}C (973 K) [73]. However, Figure 53 indicates that the etching reaction is still highly spontaneous at these temperatures $\Delta G_{reaction}$ = 128 KJmol^{-1} at 1000 K. This etching limitation must therefore be kinetic, most likely due to the activation energy which must be overcome for a reaction. This is likely also to be the limitation for chlorine etching, meaning the etch rate cannot be estimated from thermodynamic data alone.

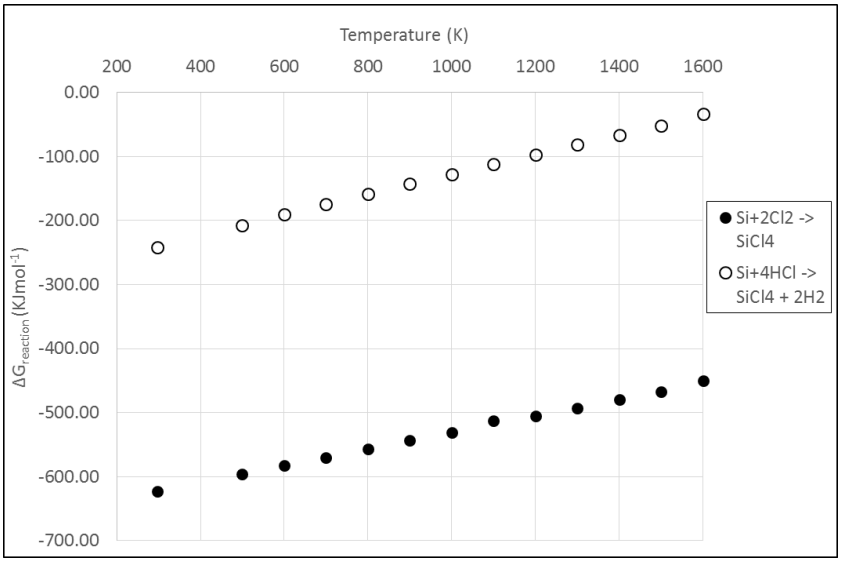


Figure 53. The reaction energies for gas phase silicon etching.

Fortunately, there is some experimental data regarding the etching of silicon by both hydrogen chloride and molecular chlorine. The latter was investigated by the IC industry, the results of this are shown in Table 7. The rate at which molecular chlorine etches silicon reproduced from [124]. This shows that the etch rate is strongly dependent upon the chlorine concentration, as evidenced by the etch rate increase from 0.23, to 1.3 μm min^{-1} when the concentration is

increased from 0.1 to 0.4% at 1173 K. The etch rate due to HCl is lower than for Cl_2 even when the concentration of the former is lower than the latter, for example Table 7 and Table 8 show that the etch rate due to HCl is 30% lower than Cl_2 when etching at 1373 K even though the concentration of the latter is 5 time higher. These etch rates are quite high but may not be prohibitive because mc-Si has a 10 μm thick saw damaged region which must be removed during cell manufacture so the loss of this material is unlikely to be deleterious. It should also be noted that the higher chlorine concentrations are also associated with a roughening of the silicon surface which may be beneficial if it improves the antireflective properties of the silicon.

Temperature (K)	Cl_2 concentration (%)	Etch rate (μm minute^{-1})
1373	0.2	1
1373	0.6	2.5
1313	0.2	0.87
1273	0.2	0.73
1248	0.2	0.69
1173	0.1	0.23
1173	0.2	0.53
1173	0.4	1.3

Table 7. The rate at which molecular chlorine etches silicon reproduced from [124]**.**

Temperature (K)	HCl concentration (%)	Etch rate (μm minute^{-1})
1350	5	3
1350	3	1.5
1350	2	0.6
1273	2	0.9
1373	1	0.7
1223	1	0.2
1073	1	0.02

Table 8. The rate at which HCL etches silicon [136][133]

5.6 Avoiding unintentional oxidation

As discussed in section 5.3.1, GPG is ineffective at removing bulk impurities if a silicon oxide layer forms during the gettering process, and as such the growth of this layer must be avoided. There are three ways to avoid the formation of an oxide which prevents GPG. Firstly, products of the oxidation process may have a structure which does not inhibit GPG. Secondly, the rate of the oxidation process could be slowed such that any oxide which grows remains too thin to prevent GPG, for example by reducing the concentration of oxygen to extremely low levels. Thirdly, a process which removes the oxide as fast as it grows could occur, such that no oxide can form on the samples.

If the oxidation products are volatile, they will not form a coherent layer which inhibits GPG. Unlike silicon dioxide, silicon monoxide is volatile (partial pressures of 0.29 Pa are observed at 1300 K [137]) and so if it is the oxidation product then a coherent layer will not form on the silicon, this is referred to as active oxidation. Silicon monoxide is formed when processing at high temperatures and low oxygen partial pressures [138]. This requires oxygen partial pressure of 1×10^{-3} Torr (6×10^{-6} atmospheres) and below, at 1273 K, which can be hard to achieve, see Figure 54. Most gas systems have a number of small leakages. These prevent the

oxygen concentrations falling low enough to enable active oxidation. It is possible to use higher quality fittings, and molecular sieves to limit the oxygen contamination levels such that active oxidation occurs, however these modifications were prohibitively costly for this work.

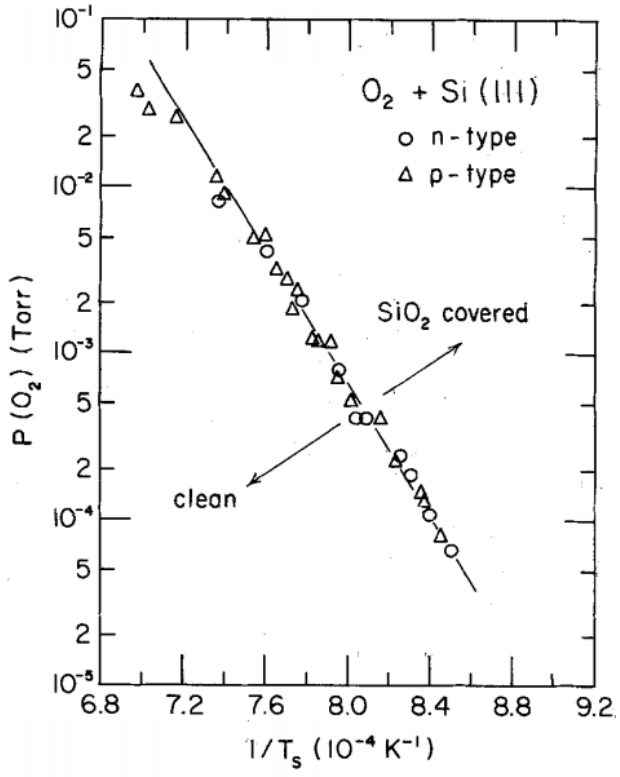


Figure 54. The boundary conditions separating active and passive oxidation of silicon. Below, and to the left of the dividing line SiO forms. This is not associated with layer formation so GPG may still occur. From [138]

If the formation of silicon dioxide layers cannot be avoided, lowering the oxygen concentration will reduce their thicknesses. As shown in Figure 55the growth rate of a silicon dioxide layer is proportional to the partial pressure of oxygen in the atmosphere [139]. In addition, the growth rate is highly dependent upon temperature [140], see Figure 55. Therefore, the thickness of the oxide may be kept to acceptable levels if lower temperatures are used and the concentration oxygen in the furnace is kept to sufficiently low levels.

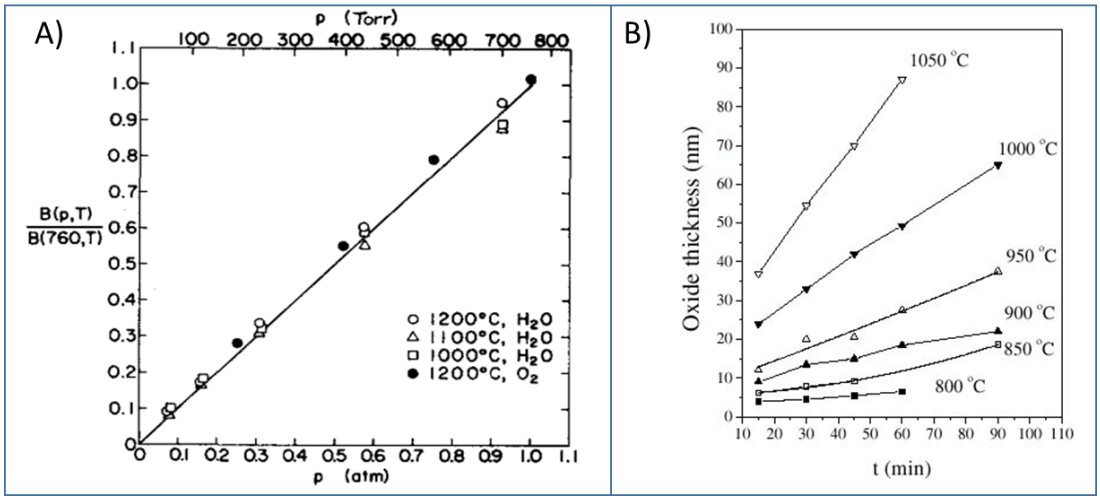


Figure 55. A). A plot of normalised silicon dioxide growth rate against the partial pressure of the oxidising species, from[139]**. B). A plot of the thickness of a growing oxide against growth time and temperature, from**[140]**, the atmosphere was 0.1MPa of dry oxygen.**

It is possible to prevent the growth of a stable oxide film by simultaneously etching it as fast as the oxide grows. Rijks et al [141] showed that a hydrogen based ambient is capable of slowly etching silicon dioxide layers. As such, a hydrogen ambient containing small concentrations of oxygen will not cause a complete silicon dioxide layer to form on silicon providing the oxygen partial pressure is low enough. While this would enable GPG to proceed without the formation of a silicon dioxide barrier layer, it would prevent Cl_2 GPG as the hydrogen would react with the chlorine to form HCl [132].

5.7 Chlorine gettering

The experimental procedure used to test chlorine gettering is as follows: Unless otherwise stated, the wafers were etched to remove at least 10 μm of saw damage prior to gettering, see section 2.1.4. They were then given full RCA cleans including a final HF dip to remove any oxides. Simultaneously the quartz furnace tubes were cleaned, and dried. The tubes were then attached to the gas lines and flushed with nitrogen for five minutes outside of the furnace. The samples were then loaded, and the tubes inserted into the cold zone of the furnace, sealed so the tubes were safe for chlorine usage, and purged with nitrogen again for five minutes to remove oxygen from the tubes before heating the wafers. The samples were then moved to the hot zone of the furnace such that they underwent very rapid heating, and 2.5 vol% chlorine in a nitrogen

atmosphere, was then passed through the tube for the desired time. After the gettering process the chlorine was turned off, and the tube purged for five minutes. The tube and samples were then removed from the furnace, where they cooled rapidly. A number of samples were then cleaned by a DI water dip for ten minutes, this process was only carried out samples from the bulk of the mc-Si wafer, and was not done for samples from the red zone of the ingot. This is because the need for this step was only ascertained partway through this work. All sample were then given an HF dip, this was required to provide a bare silicon wafer prior to further processing, see section 2.1.1 for more details. A silicon nitride layer was then deposited on both surfaces of the samples, see section 2.2.2, and then lifetime, and iron concentration measurements were made, see section 2.4.1.

It should be noted that four samples were used for each run and four sister wafer controls were given equivalent processing without any chlorine present. The flow of inert gas (nitrogen) used in this work was always 4000 sccm. This was the maximum flow rate, which was used to minimise the concentration of oxygen in the furnace even if there was a small leak. These flow rates meant that during the five minute purge cycles the gas inserted into the furnace was capable of filling the furnace 50 times, as such it was anticipated that the gaseous atmosphere would be completely exchanged in this time. The flow of Cl_2 was 100 sccm which gave a concentration of ~2.5 vol% during the GPG process.

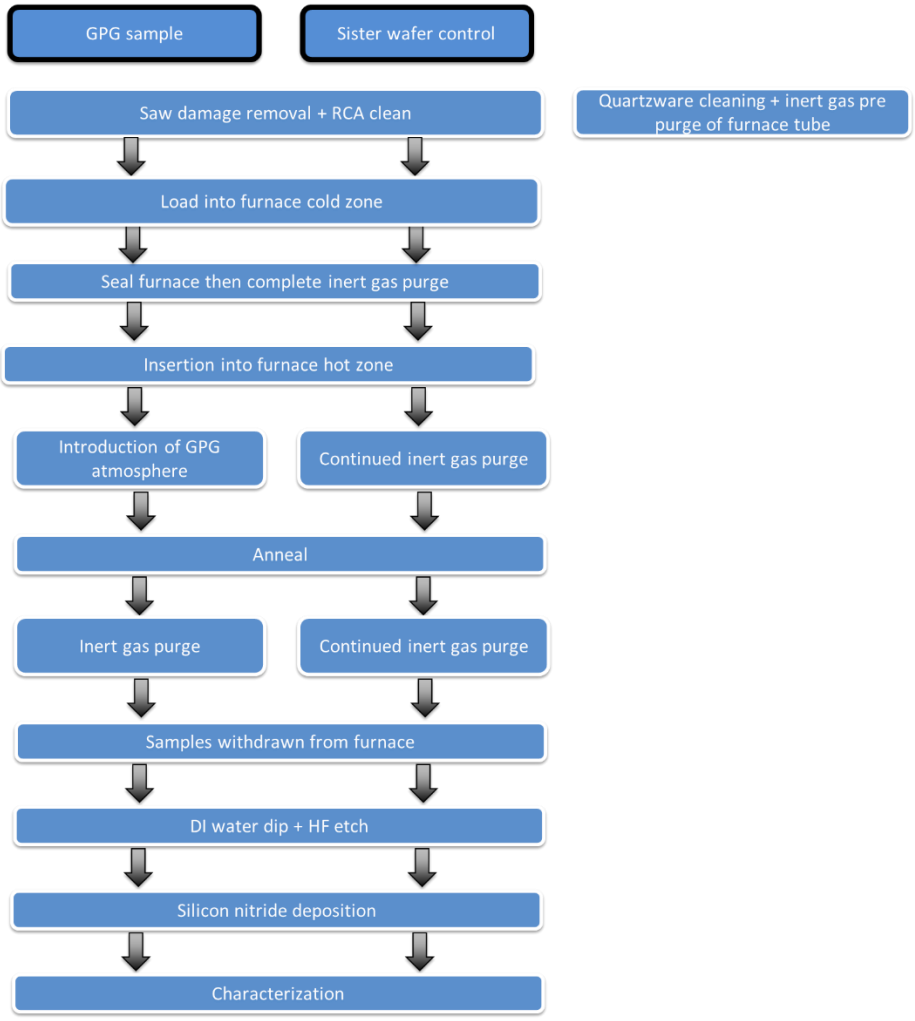


Figure 56. The processes required for GPG, this also shows the processes required for developing the controls for the GPG process.

Due to high temperatures and large cooling rates used in this work, it was necessary to use control samples which went through all of the same processing as the GPG samples other than the introduction of the Cl_2 during the annealing stage. It was then possible to evaluate the effectiveness of the GPG process by comparing the lifetimes, and interstitial iron concentrations, of the GPG samples, and their controls after the annealing process.

5.7.1 Gettering applied to red zone mc-Si

A series of sister wafers from the bottom red zone of a mc-Si ingot were also given Cl_2 based GPG. These all had their saw damage removed prior to the gettering process. Figure 57b) shows that chlorine gettering is capable of removing iron from the wafers at all of the temperatures tested in this work. This was particularly effective for the wafers processed at 1223 K, which

showed a final iron concentration of 1.2×10^{11} $cm^{-3,}$ a factor of twenty less than their control wafers. The interstitial iron concentration in the control samples increased with the annealing temperature, while the opposite is broadly true for the gettered samples. The latter is either due to increased precipitate dissolution at elevated temperatures, or contamination of the wafers by some external source. The decreased concentration in the gettered samples is therefore indicative that the gettering process is more complete at these higher temperatures.

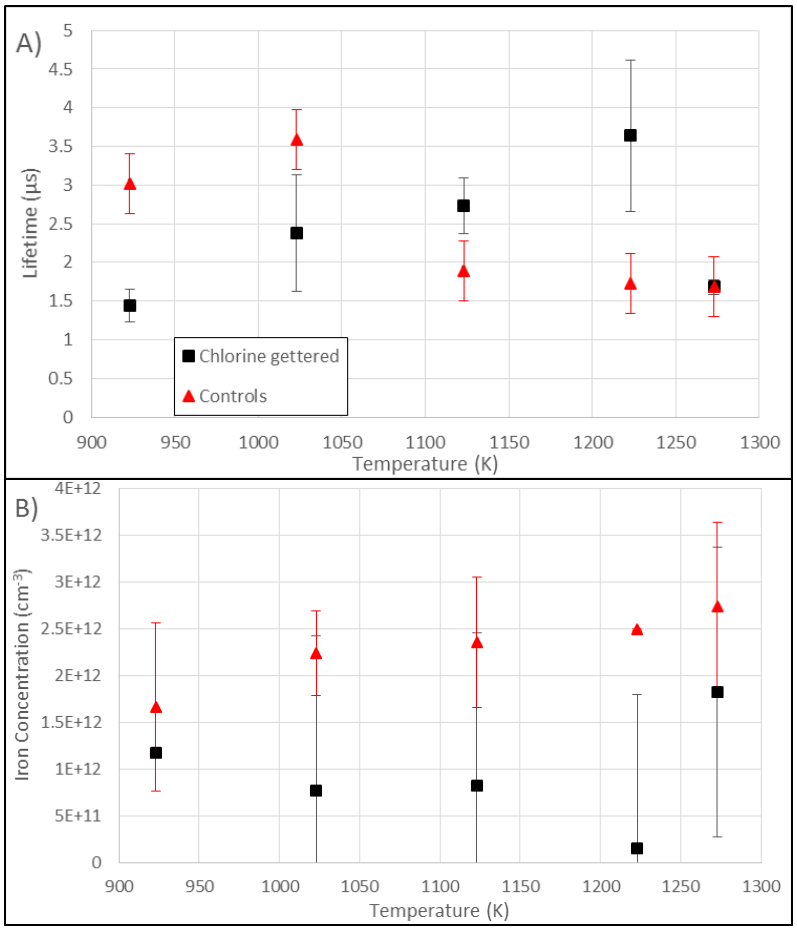


Figure 57. The lifetime and interstitial iron concentration response from processing a set of wafers from the bottom red zone of a mc-Si ingot. One set of sister wafers was given GPG in ~2.5 vol% Cl_2, and a control set were only given equivalent thermal processing without Cl_2 present. All samples were annealed for one hour. A). A plot of the lifetime as a function of the annealing temperature. B). A plot of interstitial iron concentration against annealing temperature.

How lifetime changes with the gettering conditions is more complicated. It can be seen that the lifetime of the gettered samples increases with gettering temperature, suggesting that the gettering process becomes more effective at these higher temperatures, in agreement with the iron concentration data. However, at low temperatures the lifetime of the gettered samples is

lower than in the control samples. This may be because there are two competing processes affecting the sample lifetime after GPG. GPG should result in the removal of impurities which will improve the lifetime of the samples. As discussed for iron concentrations, this effect will increase with GPG temperature. However, the GPG process may also degrade the wafer surfaces, which may decrease the observed lifetime as discussed below. If this effect is largely independent of temperature, then the net effect of the gettering temperature will be a fall in the lifetime at low temperatures where the surface damage is dominant effect. At higher temperatures, gettering may become a more important effect, and so there will be a net increase in the sample lifetime.

There are a number of possible ways that GPG may affect the surface of the samples such that the observed lifetime decreases. Firstly, it could introduce pitting into the samples, this could increase the samples' surface area which would slightly increase the surface recombination. The samples given GPG processing were seen to have developed a matt rather than mirror finish, unlike their control samples. This is attributed to the development of pits on the samples' surfaces. The lifetime of samples, with a high bulk lifetime, which are passivated with the silicon nitride layer are in excess of 100 μs, it is anticipated that this would not be drastically affected if pits were present. As the lifetimes of the samples are < 5 μs, it is believed that the surface recombination is not a major lifetime limitation in either GPG samples or their controls. As such, any pitting is not anticipated to affect the lifetime of the samples even after GPG.

However, the GPG process may still change the surfaces such that the measured sample lifetime is reduced, even though the actual lifetime is not affected, as detailed below. Samples given GPG processing look more orange after they have been coated in the silicon nitride layer compared to both conventional, and control samples, see Figure 58. It is anticipated that this change in colouration may be because gettering products have formed on the wafer surface during the GPG process. These products may then alter the silicon nitride deposition process.

The change in colouration is likely to reduce the amount of light absorbed by the silicon. This will mean that the rate of carrier generation within the silicon will be reduced in GPG processed samples relative to other mc-Si samples. However, the lifetime tester calculates the generation rate within sample based only on the illumination intensity. As such, the lifetime tester will overestimate the generation rate when the sample is more reflective than usual. As seen in equations 5.7.1 to 5.7.3, this means that the observed sample lifetime will be lower than the real sample lifetime. Consequently, if GPG affects the deposition of the silicon nitride layer, it will cause the lifetime tester to give a falsely low lifetime measure. This effect may falsely indicate that GPG is detrimental to the samples at low temperatures.

5.7.1 $$G_{en\,real} = \tau_{real} \times \Delta n$$

5.7.2 $$G_{en\,predicted} = \tau_{observed} \times \Delta n$$

Re-arranging and combining gives:

5.7.3 $$\tau_{observed} \frac{G_{en\,predicted}}{G_{en\,real}} = \tau_{real}$$

Where $G_{en\ predicted}$ is the generation rate that the lifetime tester expects within the silicon, $G_{en\ real}$ is the actual generation rate, τ_{real} is the actual lifetime in the samples and $\tau_{observed}$ is the lifetime that the lifetime tester will record.

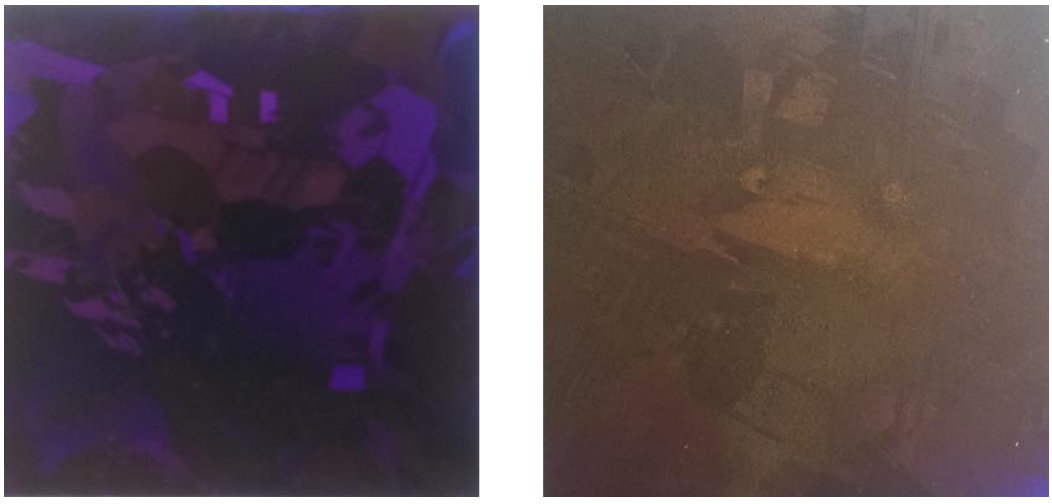


Figure 58. Photographs of mc-Si wafers after coating with silicon nitride layers. Left is a GPG control sample with a silicon nitride coating layer. This is the typical colouration of a mc-Si wafer with this coating layer. Right is a GPG sample which was not etched prior to the deposition of the nitride. It can be seen that the colouration is altered which indicates that the surface of the silicon has been altered by the GPG process. Both of these samples were annealed at 1273 K for an hour during GPG processing.

It was subsequently found that silicon nitride layers could be deposited as normal if the samples were dipped in DI water for at least five minutes before an HF dip and the nitride deposition. Unfortunately, it was not possible to repeat the above experiments with this modification, due to low sample availability.

5.7.2 Gettering bulk mc-Si

A second series of gettering experiments were carried out using silicon from the bulk of a mc-Si ingot, for each temperature/ etching condition, four sets of sister wafers were used, with one of the sister wafers being exposed to the Cl_2 atmosphere, and the other being used as a control. These samples were dipped in DI water after thermal processing to attempt to remove any GPG products which may have formed on the surfaces. This was required to ensure the silicon nitride deposited as expected.

As shown in Table 9, the presence of chlorine in the gettering atmosphere resulted in the wafers becoming upgraded. The lifetimes of the Cl_2 gettered samples significantly outperformed the control wafers in all cases, most notably when the wafers were annealed at 1323 K after the samples had their saw damage removed. Under these conditions, the lifetimes of the gettered samples are over five times higher than that of the controls.

Surface	Annealing temperature (K)	GPG in Cl_2 ambient Mean lifetime / standard deviation (μs)	GPG controls(no Cl_2 present during annealing) Mean lifetime / standard deviation (μs)
SD etched pre-GPG	1323	2.94/1.1	0.90/0.18
	1373	7.68/1.04	1.39/0.3
SD etched post-GPG	1323	4.93/1.74	1.22/0.24
	1373	2.67/0.81	0.69/0.24

Table 9 The lifetime of samples given GPG with a ~2.5 vol% chlorine atmosphere. One set of samples had the saw damage removed prior to GPG, and a second set had the saw damage removed after the gettering process. All GPG processes lasted one hour at the specified temperature.

It can also be seen from Table 10 that the gettering process significantly reduced the concentration of interstitial iron. In particular, the samples annealed at 1373 K with the SD removed showed particularly strong gettering responses as no iron could be measured in any of these samples, indicating that the concentrations were below 1×10^{10} cm^{-3}. By contrast an iron concentration of 9.1×10^{12} cm^{-3} was measured for the control samples at least nine hundred times higher than for the gettered samples. It should be noted that some sets of data show very high inter-wafer variability such as the samples processed at 1373 K with the saw damage present. These have larger standard deviations than the mean values. It is likely that the wafers that made this set had very different iron concentrations before annealing which reflect in the final iron concentrations. It can be seen that this is the case as two of the control wafers had no interstitial iron present, while the other two wafers had significant amounts, see Table 11.

Surface	Annealing temperature (K)	Cl gettering Mean iron concentration / standard deviation ($\times 10^{10}$ cm^{-3})	Control (no Cl_2 present) Mean iron concentration / standard deviation ($\times 10^{10}$ cm^{-3})
SD etched pre-GPG	1323	26/21	610/58
	1373	1/0	910/42
SD etched post-GPG	1323	210/68	660/46
	1373	250/430	8500/12000

Table 10. The iron concentrations of samples given GPG with a ~2.5 vol% chlorine atmosphere. One set of samples were gettered after the saw damage had been removed, and a second set had the saw damage present during gettering. All gettering processes lasted one hour at the specified temperature. Iron concentrations below $10^{10}cm^{-3}$ cannot be measured, so this is taken as the minimum iron concentration.

Despite the benefits seen from GPG the iron concentrations did not fall as much as predicted by the above theoretical calculations. Additionally, the lifetimes did not increase as much as would have been expected if the concentrations of other impurities had been reduced as much as predicted. It was suspected that this may have been due to the unintentional growth of a

diffusion barrier layer, assumed to be silicon dioxide, during the gettering process due to unintended oxygen contamination of the furnace tube. It could be inferred that a surface layer grew during GPG processing because after thermal processing, water became able to wet the samples. As discussed in section 2.1.1, this means that the surface layer was not bare silicon. Further evidence indicating that a barrier layer formed during GPG is provided in section 5.7.3. It is believed that this additional layer silicon dioxide as this layer forms very readily.

Interstitial iron concentration (cm^{-3})	8.31×10^{13}	1×10^{10}	2.59×10^{14}	1×10^{10}

Table 11 The iron concentration of the four control wafers annealed at 1323 K in an inert atmosphere with the saw damage present, it should be noted that the characterisation technique used cannot detect concentrations below 10^{10} cm^{-3}, this is thus given as minimum iron concentration. This data highlights the very high level of variability in the initial wafers. This is likely due to the variability in the as cast wafers.

5.7.3 Etch rates

As discussed, it was suspected that a silicon dioxide layer formed during the gettering process, limiting GPG effectiveness. This could be tested for by analysing the silicon etching rates. The etching of silicon by Cl_2 does not produce compounds which limit further reactions, for example by forming a barrier layer. Therefore, the etch rate should be independent of process time, and should broadly agree with literature results. If this is not seen to be the case, it can be inferred that a second, rate altering, process is occurring concurrently with the chlorine etching. To test if this was the case three sets of sister wafers were etched to remove their saw damage. They then had their oxides removed and were weighed. They then underwent a 1223 K anneal in 2vol% chlorine for various times. They were then given an HF dip and weighed again. Their mass lost was converted into an etch rate as plotted in Figure 59. From this it can be seen that the etch rate falls as process time increases. In addition it can be seen that the etch rate is significantly less than the value of 0.69 μm min^{-1} predicted by the literature when etching in only 0.2% Cl_2 [124]. In addition, water was seen to wet the samples after exposure to chlorine, but before the HF dip. These results strongly indicate that a thermal silicon dioxide barrier layer formed during annealing. This barrier caused the reduction in the etching rate and is also likely to have reduced gettering efficacy.

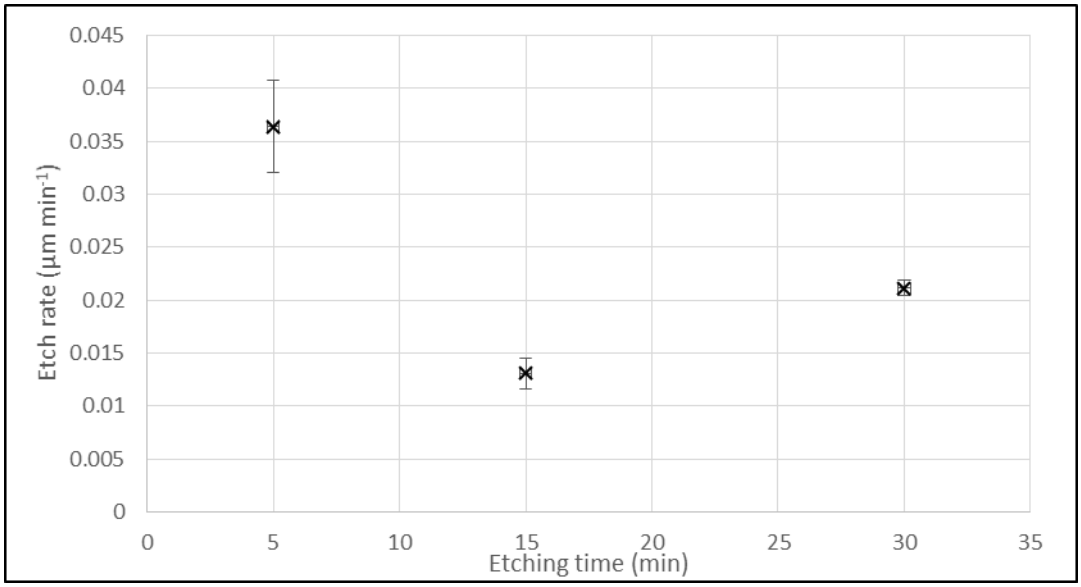


Figure 59. The etch rate of samples exposed to chlorine atmospheres at 1223 K for varying durations. It can clearly be seen that the etching rate is not independent of the process duration indicating that a protective barrier layer has formed. The errors are principally due to measurements of the sample mass. This has a relatively lessened effect on the etch rate when longer times are involved.

5.7.4 Chlorine gettering discussion

It has been seen that chlorine etching is capable of gettering impurities from a silicon wafer at all of the temperatures tested. This is in agreement with the theoretical calculations from section 5.5 which predict that chlorine should be an effective gettering centre at all temperatures. It has also be shown that the gettering process becomes less effective at lower temperatures. Again this is in agreement with theoretical calculations showing that impurity flux away from internal defects limits the low temperature gettering efficacy.

Chlorine gettering has not been seen to upgrade the wafers to high lifetimes in excess of 10 µs, and in most samples the iron concentrations were not reduced to undetectable levels. While this limited success was anticipated for slow diffusing impurities such as titanium, theoretical calculations suggested that the iron gettering in particular should have been more complete given the process times and temperatures. As discussed above, it is likely that a silicon dioxide film formed during gettering. As impurity diffusion through these films is very slow the growth of this film will impede the gettering process, dramatically reducing the effective time during which gettering can occur. This can only be avoided if the oxygen concentration can be reduced further. It is likely that the same process which inhibited GPG also limited the extent to which

the samples etched. This means it was not possible to use this work to test if the etch rates would be acceptable when carrying out GPG processing. The literature suggests that the 10 μm saw damage layer would take ~15 minutes to remove when using a 0.2 vol% Cl_2 atmosphere, but it is not clear if this would be enough time to remove impurities if diffusion barrier layers were not formed.

5.8 Conclusions and further work

It has been shown that gas phase gettering is a potentially valuable technique to remove metallic impurities from silicon wafers. It is capable of gettering impurities at very high temperatures where other impurity sinks such as crystallographic defects do not effectively capture impurities. This means GPG should be able to upgrade wafers to a higher quality than possible using any other technique. This may enable wafers with higher dislocation densities to be used without adversely affecting cell efficiencies. However, this is only the case when an appropriate gettering atmosphere and temperature is chosen. It has also been inferred that the inclusion of oxygen in this atmosphere severely impedes the gettering process. It has been inferred that the GPG atmospheres used in this work were contaminated with oxygen, and that this caused silicon dioxide layers to form. These layers reduced both the gettering efficacy and the rate at which the silicon was etched by the chlorine. There are a number of additional experiments which would be useful to carry out to understand GPG more effectively:

- GPG using a Cl_2 atmosphere with a lower oxygen concentration would be useful to achieve more effective gettering, and also to better understand the trade-off between gettering and etching.
- It would be useful to repeat the tests on RZ mc-Si material with the DI dip step included to see how the lifetime is affected by the GPG process.
- It would also be useful to test the gettering process on a trial systems with only single impurity type present. This would be useful to test the theoretical calculations.
- It might also be interesting to test the GPG process on lower quality material such as UMG-Si, as this may be of greater industrial significance.

6 Shielded Hydrogen Passivation

In this chapter surface coatings for silicon solar cells are reviewed. The benefits and current techniques for hydrogenating these films are also covered. This chapter then describes a new technique by which hydrogen can be incorporated into these films, namely shielded hydrogen passivation (SHP). A significant body of this work was dedicated to understanding, and preventing, damage caused by the plasma during SHP.

6.1 Introduction

In this section surface coatings are discussed, including the mechanisms by which they passivate the silicon. Hydrogenation of these films is also discussed. Finally, SHP is introduced, this includes an overview of the potentially damaging processes which may occur if inappropriate shielding is used.

6.1.1 Surfaces as recombination centres

As discussed in section 1.3.2, the surfaces of wafers are potentially highly active recombination sites. Silicon surfaces are associated with a high density of dangling bonds, as they are terminations of the crystalline matrix. These dangling bonds introduce energy levels within the band gap of the silicon [142], [143]. These energy levels increase minority carrier recombination, and are thus detrimental to the solar cell performance, see section 1.3.2. The surface recombination velocity is determined by recombination at surfaces. Its effect on practical samples is determined by:

6.1.1
$$\tau_s = \frac{d}{2S_{RV}} + \frac{1}{D_{mc}}\left(\frac{d}{\pi}\right)^2$$

Where τ_S equals the lifetime due to the surfaces, d is the thickness of the samples, S_{RV} is the surface recombination velocity and D_{mc} is the minority carrier diffusivity. This assumes that the surface recombination is the same at both surfaces. The surface limited lifetime can be calculated if the lifetime in the bulk of the wafer, and the total wafer lifetime is known:

6.1.2
$$\frac{1}{\tau_{srv}} = \frac{1}{\tau_{total}} - \frac{1}{\tau_{bulk}}$$

For this study the bulk lifetime was both high and approximately constant (~7ms as determined by the wafer suppliers), meaning the effective lifetime could be used to evaluate changes to the surface recombination, as it was the only lifetime limiting factor which changed.

6.1.2 Controlling surface recombination

It is possible to reduce surface recombination, through the application of a surface coating, typically a dielectric, which passivates the surface. There are two types of surface passivation, chemical and field effect. Both types can be applied simultaneously.

6.1.2.1 Chemical passivation

Chemical passivation reduces the recombination rate by reducing the density, and changing the nature, of the energy levels within the band gap. This is achieved through bond formation between the silicon and the coating layer. This removes dangling bonds so band gap energy levels are also removed. The nature of the energy levels may be changed if the dangling bond is replaced by a different bond, for example a strained silicon/ nitrogen bond when passivating with silicon nitride. The new defect levels typically are closer to the edges of the band gap and as such cause less recombination. The coating layer providing chemical passivation is usually a dielectric, and as such has a much wider band gap than silicon. Therefore energy must be supplied to enable minority carriers to enter the dielectric. This energy typically far exceeds kT at room temperature, so the density of minority carriers within the dielectric will be small. This means the net recombination rate within these regions will be low.

The passivating layer should minimise the number of dangling bonds remaining at the silicon surfaces [144]. These bonds are removed through bond formation between the crystalline silicon and the coating layer. However, some dangling bonds will remain as the surface layer will not have the same crystallography as the crystalline silicon. Therefore a fully coherent interface would significantly strain the interatomic bonds in both layers. This is energetically unfavourable so the bonds layer will still contain dangling bonds [145]. It may be possible to form further bonds at these sites through the use of monatomic hydrogen. This is a very small

species, which can form a single covalent bond, as such it can terminate dangling bonds in the silicon without introducing significant additional strain into the system.

6.1.2.2 Field Effect Passivation

If an electrical field can be induced such that one type of carrier is repelled from the silicon surface, the recombination rate can be reduced, this is called field effect passivation (FEP). FEP can be achieved through the application of an unbalanced charge at the silicon surfaces. This charge repels carriers of the same type. This can be visualised as the bending of the silicon band structure near the surfaces, Figure 60. If the coating has the same sign charge as the minority carriers it means the concentration of minority carriers adjacent to the defects associated with the surface is reduced. The recombination rate at any location is the product of its inverse lifetime and the minority carrier density. Thus reducing the number of minority carriers at the surfaces will reduce total recombination in these regions.

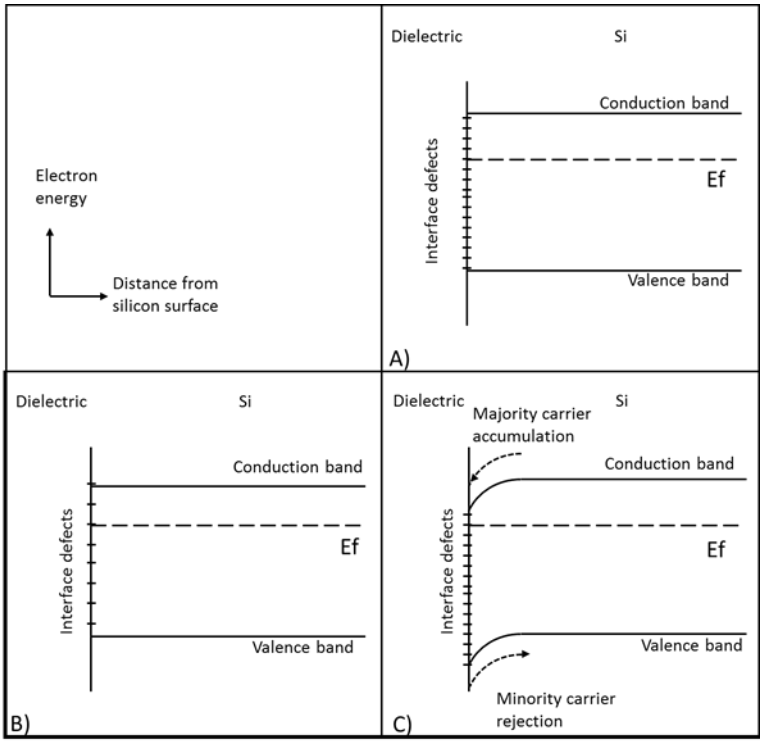


Figure 60. A schematic of the energy states at silicon surfaces, a) is a poorly passivated surface, b) has additional chemical passivation with an associated decrease in interface trap density., c) has field effect passivation applied.

FEP can also reduce the recombination rate if sufficient charge of the same type as the majority carriers is applied. This reduces the concentration of majority carriers at the surfaces until they become minority carriers (referred to as inversion), and their density is reduced until recombination falls. When inversion occurs it means there will be a region of material where the concentration of both types of carriers are equal. Therefore both can readily be supplied to defects and the total recombination in these regions will be high relative to the region's lifetime. Therefore inversion is generally undesirable.

When the charge associated with a surface is increased, the carrier re-distribution near the surfaces will also increase. This is reflected in the net recombination rate. When the charge density is small, the sample lifetime is strongly affected by small variations in the surface charge density. However, this dependence is weakened at high charge densities where the lifetime response saturates, see Figure 61. If too high a potential is held across the dielectric a breakdown current will pass, reducing the potential and damaging the dielectric. As such these potentials are not stable, this may limit the ultimate effectiveness of FEP [146].

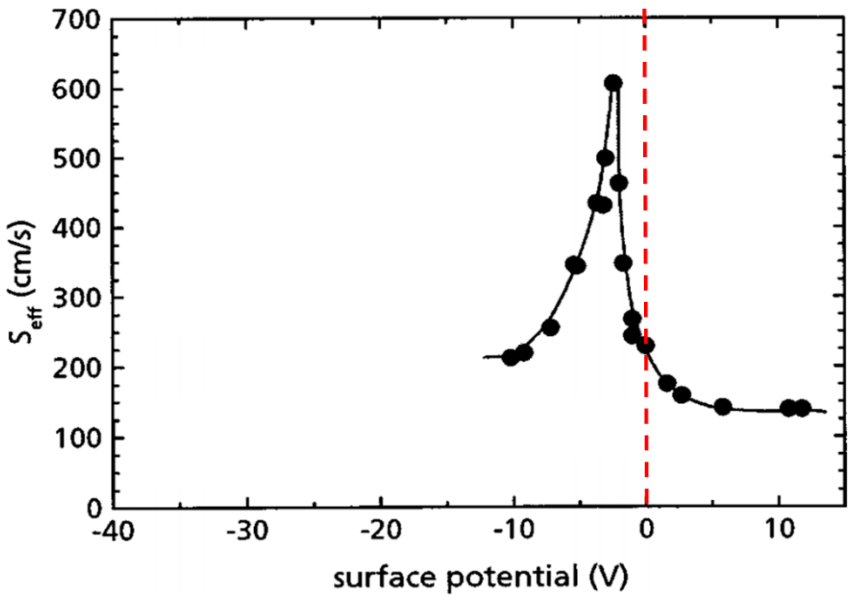


Figure 61. How the potential at the surface of the silicon affects the recombination rate at the surfaces. Lower S_{eff} values correspond to lower recombination rates. At low potentials it can be seen that recombination rate is highly dependent upon the potential, and therefore the charge density at the sample surface. This strong dependence is not seen when the charge density, or potential, has a large magnitude. Modified from [147].

FEP can be supplied extrinsically. This can be achieved by depositing charged species onto a dielectric layer. As long as these charged species are not neutralised or removed they will passivate the underlying silicon. It has been shown that this charge can be stabilised if deposited on a thermal silicon dioxide layer which is then coated to prevent water adsorption [56]. This is important as it suggests that charge is not lost through the silicon dioxide layer itself.

6.1.3 Current passivation layers

As discussed in section 6.1.2, it is important that any passivation layer has good FEP and chemical passivation. The former is typically achieved by either using a dielectric layer which is non-stoichiometric [148] or by applying extrinsic charge to the surfaces. Chemical passivation is typically achieved by depositing a layer onto the surface of the silicon. The most common of these are thermally grown silicon dioxide[149], aluminium oxide [150] [151], amorphous silicon, and plasma formed silicon nitride, sometimes in multilayer structures[152]. The properties of the latter two are improved as they contain high concentrations of hydrogen, which can passivate silicon bonds which would otherwise not be passivated.

6.1.4 Hydrogenation

The incorporation of hydrogen into solar cells has been shown to be beneficial in a number of ways, consequently hydrogenation techniques have been developed, and will be discussed below[145][153][154][155][156].

6.1.4.1 Benefits of hydrogen

Hydrogen has a number of unique properties which enable it to be used to improve solar cells. It is a very small atom which is capable of forming a single covalent bond. These properties mean that it can form bonds without needing to be incorporated into the structure of either the silicon or its coating layer. As such it can remove dangling silicon bonds without degrading the passivation provided by the coating layer. Hydrogen can also terminate dangling bonds within the bulk of a silicon wafer, passivating internal defects [157].

6.1.4.2 Extrinsic hydrogenation techniques

Although hydrogen may be incorporated during film deposition, a number of additional techniques exist to supply hydrogen extrinsically. In order for an extrinsic hydrogenation technique to be viable three conditions must be satisfied. Firstly, it must not cause damage to the pre-existing structure as this would negate the benefits offered. Secondly hydrogenation should be rapid to maximise throughput. Thirdly, the hydrogen supplied must be capable of passivating defects. In order for the latter to be satisfied it is believed that hydrogen must be present in a monatomic form. This is because monatomic hydrogen is significantly smaller than molecular hydrogen and as such its diffusivity is greatly enhanced [158][159]. As such it can readily diffuse to defected bonds enabling passivation. Additionally, as hydrogen passivates defects through bond formation, the energetics of passivation will be enhanced when the hydrogen/hydrogen bond present in the molecular form are broken by the hydrogenation process, see Figure 62.

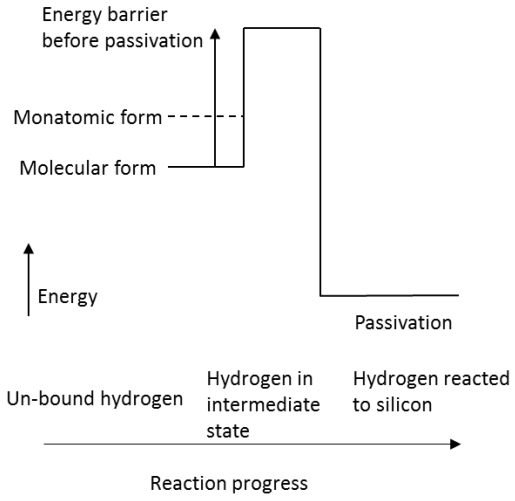


Figure 62. A simplified energy diagram for the reaction between hydrogen and silicon dangling bonds. On the left is the energy associated with the hydrogen, either molecules or free radicals, before the reaction. The middle shows the energy barrier to the reaction, and the right shows the energy associated with the hydrogen after the reaction is completed. In a Forming Gas Anneal hydrogen must be released from the molecular state before it can passivate defects, and as such must overcome an energy barrier. In a PECVD reactor, the reactor supplies the energy needed to form monatomic hydrogen by igniting the plasma. This should accelerate the passivation process. This figure also shows that the monatomic form is only metastable.

6.1.4.3 Forming gas anneals

Currently, the principal technique used for incorporating extrinsic hydrogen is through forming gas anneals (FGAs). In a FGA the hydrogen is supplied by an atmosphere which contains molecular hydrogen. The samples are then annealed at approximately 400 ^{o}C. At this moderate temperature it is unlikely that the pre-existing structures will be significantly modified and so FGA provides hydrogenation without causing any deleterious effects. Unfortunately, FGA is not a particularly rapid process (typically lasting over 30 minutes) because the formation of monatomic hydrogen is not specifically facilitated in this technique. As such the generation of monatomic hydrogen is likely to be rate limiting.

6.1.4.4 Remote PECVD hydrogenation

Extrinsic hydrogenation may also be achieved through the use of remote PECVD (rPECVD). In this technique samples are held at approximately 400 ^{o}C, and hydrogen is supplied by the gaseous atmosphere. The plasma provides energy to the gas such that monatomic hydrogen is generated, enhancing the passivation energetics and potentially resulting in more complete saturation of the defected bonds.

However, the plasma may simultaneously introduce damage into the samples. This is partially mitigated as the plasma is remotely generated so the sample/ plasma exposure is reduced, see Figure 63. This reduces, although does not fully eliminate, the damage induced by the plasma [160]. One issue associated with using a remote plasma is that the monatomic hydrogen generated by the plasma must travel approximately one meter before reaching the samples. Consequently, the monatomic hydrogen species may be partly annihilated during transit, reducing the number density of these species in direct contact with the samples. This reduces the achievable passivation rates, either reducing throughput or passivation efficacy.

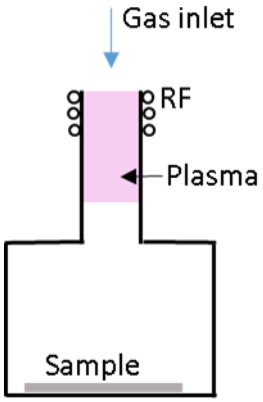


Figure 63. Shows a schematic of a remote PECVD from[160]**. The concentration of both damaging species and monatomic hydrogen decreases away from the plasma.**

6.1.4.5 Direct PECVD

The use of a direct PECVD reactor as a hydrogenation source has been attempted. A direct plasma source should significantly increase the concentration of monatomic hydrogen in contact with the samples, and so should increase the passivation rate. However, as the samples are also directly exposed to the plasma, the damage rates will be significantly increased. This explains the deleterious results exhibited by such direct techniques [161].

6.1.4.6 Shielded Hydrogen Passivation

In the present work an additional hydrogenation technique is introduced. This technique, called Shielded Hydrogen Passivation (SHP), uses a direct PECVD reactor to split ammonia, producing monatomic hydrogen, and a shield, which is permeable to monatomic hydrogen, to protect the sample from the plasma. The shield allows the plasma to be located very close to the samples (< 1cm), which should increase the local density of monatomic hydrogen whilst preventing extensive damage to the sample. In this technique it is very important to use the correct shield to prevent all potential damage mechanisms.

6.1.5 Plasma damage mechanisms

Plasmas can induce damage to any exposed materials. When a silicon substrate coated by a dielectric layer is exposed the damage may affect the underlying silicon, the bulk of the dielectric or the interface between the two. Damage to any of these parts of the system are anticipated to be detrimental to the overall performance of the solar cell. In the following

section the potential damage mechanisms are discussed. This will include a mechanistic description of each damage mechanism, as well as an explanation about how the solar cell may be affected by this type of damage. Particular emphasis will be given to a system consisting of a silicon layer coated in a thermal silicon dioxide layer.

Plasmas are comprised of a combination ions, free electrons, radicals, excited gaseous species and UV radiation, as well as less highly excited molecules. As the electrons are the most mobile charged species present, they rapidly move to the walls of the reactor where they are collected and so the plasmas generated within a reactor are typically charged[162]. Consequently an electrical field develops which can accelerate charged species towards that walls of the vessel.

6.1.5.1 UV radiation

The high energy densities associated with plasmas generate UV photons. It has been documented that this high energy radiation can induce either break or strain chemical bonds at silicon/ silicon dioxide layers such that recombination increases in these regions [163] [164] and it is probable that UV radiation will also damage other surface layers as well. This mechanism could be present whenever there is line of sight between the plasma and the samples.

6.1.5.2 Chemical reaction

The plasma generates highly reactive species including gaseous ions and neutral radicals [165] which may react with the surface layers. This may damage the dielectric structure and thus the passivation that it offers. However, this is quite unlikely as these species are unlikely to have enough energy to break the strong bonds (<6 eV [166]) within the silicon dioxide layer. Even if they could break these bonds it is unlikely that they would do so near the Si/SiO_2 interface as this would require their prior diffusion through 100 nm of oxide. This diffusion is expected to be slow for any species other than monatomic hydrogen due to the size of other species present in the reaction chamber. Monatomic hydrogen is not anticipated to be detrimental as it is expected to passivate rather than damage the interface.

6.1.5.3 Physical impingement

Physical impingement by ions can generate damage. As discussed in section 6.1.4.4, a field is generated between the electrodes and the plasma adjacent to them. These fields accelerate the positive ions towards the chamber walls, imparting kinetic energy. These ions will collide with the samples and may have enough energy to damage the dielectric layers.

6.1.5.4 Electrical breakdown

The plasma has a net charge, and this charge will be deposited onto the surfaces of any exposed materials. If these materials are not fully earthed this charge can build up. In the case of a dielectric/ silicon structure this charge build up will induce an electric field across the dielectric. If this field becomes too large it will result in electrical breakdown of the dielectric. This breakdown results in the passage of a high, localised, current through the oxide layer. This introduces damage into the silicon dioxide layer and the silicon/silicon dioxide interface. This effect has been observed by the integrated circuit industry[162], and could be caused by charged plasmas. There are a number of features which indicate that electrical breakdown is occurring in a given SHP system. One such feature will be that the damage induced by the plasma will be more notable when processing at lower temperatures, as discussed in section 6.5.6. In addition, this system requires an unbalanced charge to be deposited on the sample surfaces. It is possible to detect this charge, and thus to test if electrical breakdown is a damage mechanism which may be active in a given SHP system.

6.1.6 Beneficial effects of SHP

It is expected that SHP should improve the passivation of samples in a number of different ways. These are as follows:

6.1.6.1 Plasma induced FEP

As discussed, SHP may deposit unbalanced charge onto the surfaces of samples. This will cause FEP to occur and may improve the sample lifetime. This effect could be significant immediately after SHP. The as-received samples are initially free of charge, so their lifetime is strongly affected by any net charge application, see Figure 61. However, if the samples are subsequently,

optimally, extrinsically charged the effect of SHP induced FEP will be masked as optimum FEP will be supplied by the extrinsic charge.

6.1.6.2 Chemical passivation

It is anticipated that some hydrogen induced chemical passivation will be developed at the silicon/silicon dioxide interface. This effect will only be observable if minimal damage occurs during SHP processing. It should also be noted that this effect can be confused with SHP induced FEP. Both of these processes will result in increased wafer lifetimes after SHP processing. However, the two can be isolated by supplying extrinsic charge which ensures that the system has optimal FEP regardless of charge deposited during SHP. This enables any chemical passivation to be unambiguously identified.

6.1.6.3 Dielectric annealing

In this work, SHP processing occurs at moderately elevated temperatures. This may enable thermally activated processes to occur. It is not clear if this will have a net insignificant, beneficial or detrimental effect on the wafers' passivation.

Process active during SHP	Effect on lifetime post plasma, pre extrinsic FEP	Effect on lifetime post plasma, post extrinsic FEP
Chemical passivation	Slight benefit	Strongly beneficial
Un-optimised FEP	Strongly beneficial	None
Dielectric annealing	Unknown	Unknown
Electrical breakdown	Slightly negative	Negative
Physical impingement	Slightly negative	Negative
UV radiation bombardment	Slightly negative	Negative
Chemical degradation	Slightly negative	Negative

Table 12. The impact of different potentially active processes upon the lifetime of samples both before and after extrinsic charging.

6.1.7 Net effect of SHP processing

As discussed, SHP processing can have both beneficial and detrimental effects. This work aims to produce a process which reduces the latter to negligible levels, whilst enabling the former to

still have a significant passivating effect. This can be challenging as similar processes can promote both beneficial and detrimental effects. For example the deposition of unbalanced charge both causes detrimental electrical breakdown, as well as inducing beneficial FEP. Both of these processes are expected to have a significant impact on the final result of the samples. These conflicting effects can make interpreting the results challenging, as the two processes may mask the other's effect. A methodology to overcome these difficulties is discussed in section 6.2.7.

6.2 Experimental methods

In this work a PECVD reactor, see section 2.2.2, was used to split ammonia molecules, generating monatomic hydrogen which can subsequently passivate the samples. As discussed, this plasma can damage the samples, consequently in this work they were protected by a shield, see Figure 64. This section will discuss the different shields used, as well as the processing conditions, and processes required to ensure that the results can be evaluated correctly. The metallic shields were electrically connected to the plasma chamber, which was itself earthed. This meant that the shield always was earthed. The shield and chamber also formed a Faraday cage around the samples.

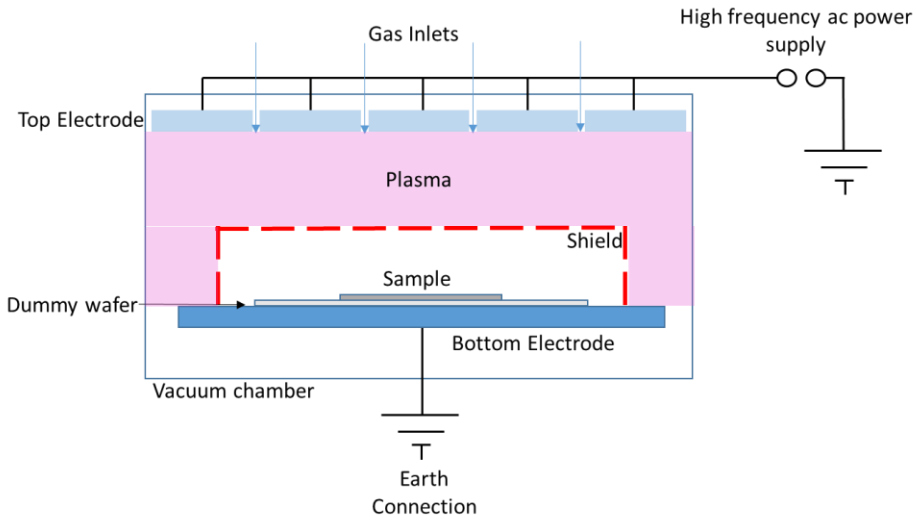


Figure 64. A schematic the SHP experimental set up, including the PECVD reactor, and the shield which protects the samples.

6.2.1 "Grid" shield

One shield was constructed from two sheets of aluminium with a square array of circular holes, the hole diameter was 4 mm and the spacing between hole centres was 8 mm. These two sheets were arranged such that the holes anti-aligned and there was minimal line of sight through the sheets. The sheets were then folded such that they could protect samples from above and the side, see Figure 65. The gap between the plates was large (~2mm) consequently reactive species could pass from the plasma to the samples without passing near the shield. This large gap means the probability of a charged species passing through the shield without colliding with it was high, see section 6.5.1. This shielding method will be referred to as a grid for the rest of this work.

6.2.2 "Mesh" shield

The second shield type was a fine wire mesh woven from 0.2 mm thick stainless steel wire with 0.4 mm holes. The mesh was coated in an aluminium layer >100 nm thick to prevent contamination of the PECVD chamber and to ensure the surface of the shield was conductive. The mesh was then bent into a three dimensional shape as above. Two meshes separated by a ~1mm gap were always used in series to provide additional shielding. The holes in the mesh are very small so any species from the plasma must pass near to the solid, earthed, part of the mesh before reaching the sample. This shield allowed line of sight between the plasma, and the shielded samples. This shield is hereafter referred to as a mesh. See Figure 65 for an image of this shield.

6.2.3 Dual Shielding

The mesh and grid shields were also combined, by stacking the two shields over each other. This created a new shield which was expected to have the benefits of both individual shields.

6.2.4 Pd shielding

A thin (<0.2 μm) palladium (Pd) leaf (supplied by Gold Leaf Supplies) was also used as a shield. However, due to its low mechanical strength it had to be supported by an aluminium structure. This structure was a partially hollowed cylinder, with holes drilled through the top surface. These holes aligned with a cap. The palladium sheet was placed between these two structures

which were then screwed together, see Figure 65. If gas could not pump out of this shield a pressure difference would be developed across the palladium film and could tear it. This was avoided by having a hole though the side of the cylinder which was then lightly stoppered with folded palladium leaf, which provided a torcherous path for damaging species passing from the PECVD chamber to the sample, while still allowing pressure equalisation between the two. Two aluminium support structures were developed. The first structure, which was used for all Pd shielded experiments unless otherwise stated, had holes occupying ~18% of the top surface. The second, more open structure had holes occupying ~80% of the top surface and was made only part way through this work.

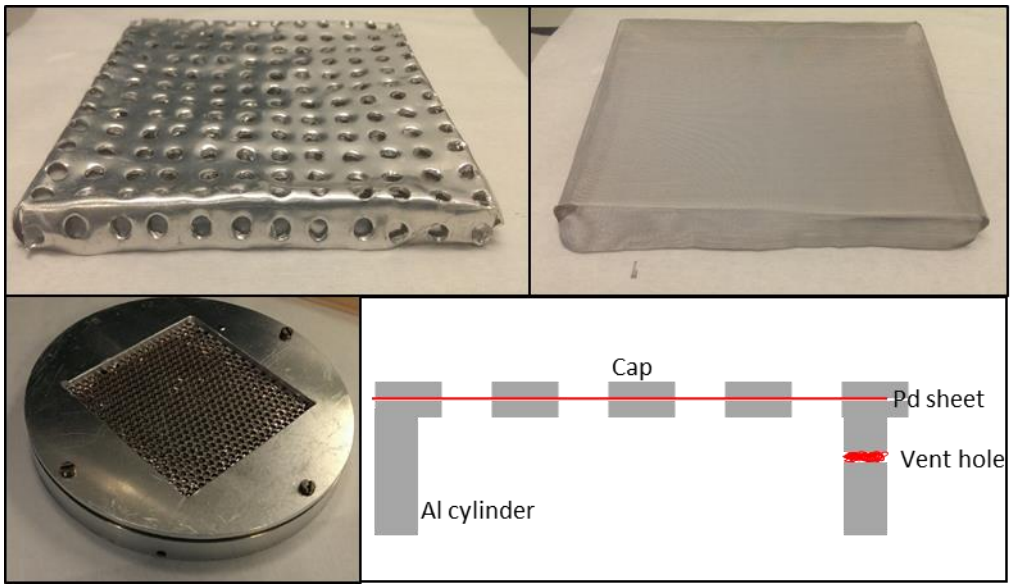


Figure 65. A). The "grid" shield. B). The "mesh" shield. C). The final palladium shield, which had the largest open area, palladium sheet can be seen between the aluminium supports. D). A schematic of the palladium shield with the vent hole shown.

6.2.5 Quartz Shielding

A quartz sheet was also used as a shield to test for a specific damage mechanism. It was important that this shield was as UV transparent as practical, so "UV transparent quartz" was used to minimise optical losses.

6.2.6 Process conditions

SHP is primarily a surface passivation technique, and as such can be most accurately evaluated when the lifetime of the as-received wafers are dominated by surface recombination rather than bulk recombination. This was achieved by using high quality 1Ωcm phosphorous doped FZ-Si

material, the sawing damage was chemically removed prior to processing. These wafers were thin, ~200 μm, and so surface recombination was particularly important. The as-received wafers had also been passivated through the growth of a 100 nm thick, thermal silicon dioxide layer grown on both surfaces in a hydrogen free environment. This oxidation was performed by Fraunhofer ISE. Unless otherwise discussed, the process conditions are those detailed in Table 13.

Ambient	Pressure (mTorr)	Process duration per side (minutes)	PECVD power (Watts)	Temperature
Ammonia	650	10	20	350

Table 13. The default conditions used for SHP processing. These are used unless otherwise specified.

6.2.7 Interpreting SHP results

SHP is designed to improve the chemical passivation of a silicon surface, while changes to FEP are, for this particular process, not considered to be beneficial. While FEP may not be detrimental for many applications, it may be problematic if the as received wafers had an optimised charge state prior to the SHP process. This should not be affected by the SHP process.

As discussed, the use of plasmas, and thus SHP, can result in charge deposition. This means SHP can change sample FEP. It is important to distinguish this from chemical passivation, as the latter is a better metric of the hydrogen passivation. A lifetime measurement made immediately after SHP will be unable to distinguish between the two passivation types. This means an SHP process which damages chemical passivation but induces FEP could appear beneficial, even though it does not fulfil the goals of the SHP process.

Applying extrinsic charge to the samples can remove the ambiguity which results from SHP being able to induce FEP and chemical passivation, see section 6.1.2.2. Immediately after the SHP process, the passivation consists of the SHP induced FEP, and the chemical passivation present after SHP processing. After corona charging, the chemical passivation remains the same, and FEP is at an optimal level which is independent of the SHP induced FEP, and approximately consistent across all samples. Consequently, the latter measurement provides a good way to

compare the chemical passivation of different samples. Comparing the former measurement against the latter, gives an indication about the amount of FEP induced by the plasma.

6.2.8 Processing without a plasma

It is important to verify if annealing samples in an ammonia atmosphere, with no plasma present, significantly influences them, as this must be considered when interpreting the results of the SHP process. A sample was processed using all of the conditions detailed above except no electrical power was supplied to the gas, so plasma was not produced. As seen from Figure 66, annealing in an ammonia based ambient had minimal impact on the sample lifetime. Therefore any changes that result from the SHP process can be attributed to the plasma.

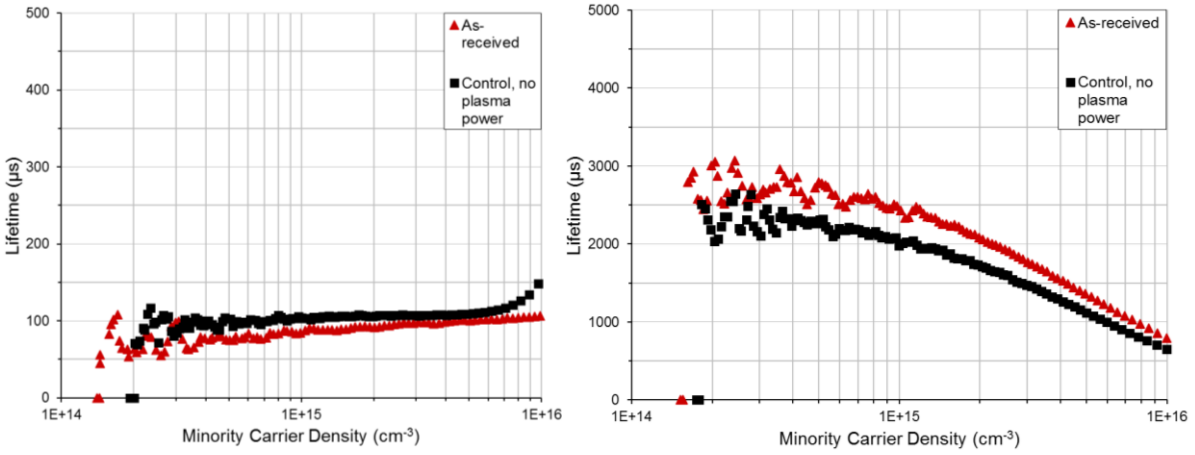


Figure 66. The effect of ammonia exposure in the absence of a plasma. A) Compares an un-processed sample against one exposed to ammonia gas at 350 °C for ten minutes per side. B) Compares the same samples also given optimal extrinsic FEP. From both it can be seen that the ammonia anneal has minimal effect on the samples if no plasma is present.

6.3 Direct PECVD

Direct contact between the PECVD plasma and the sample is the simplest set up that can be tested, although it is unlikely to improve chemical passivation. The literature suggests that direct exposure of samples to ammonia plasmas can be detrimental [161]. This is verified by processing samples via the SHP process without a shield present. As is shown in Figure 67, this results in significantly decreased chemical passivation compared to unprocessed samples, in agreement with the literature. This shows that any chemical passivation which may occur as a

result of hydrogenation, is being overwhelmed by the damage introduced by the plasma. All further work presented uses a shield to reduce this damage.

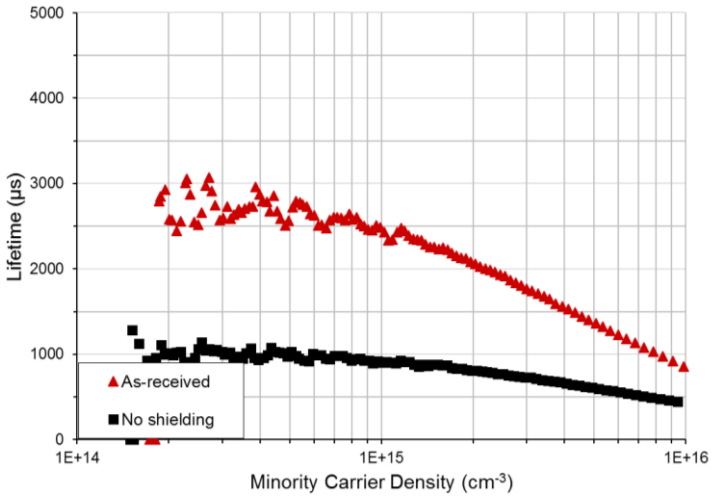


Figure 67. One sample was exposed to an ammonia plasma without any shielding while the other was not exposed to any thermal or plasma processing. Both samples were then given optimal corona charging. Their lifetimes as a function of minority carrier density are presented and show that the unshielded plasma is damaging chemical passivation.

6.4 Perforated Shielding

The first shields tested were made from perforated aluminium coated structures, where the active species had to pass through the holes in order to reach the samples. These shields included both the grid and mesh shields described above. These structures were earthed via the bottom of the reaction chamber and so they form a Faraday cage around the samples, therefore there are no electrical fields adjacent to the samples.

6.4.1 Collisions between the shield and charged particles

The charged particles generated by the plasma must pass through the shield before they can reach the samples. It is assumed that they will be neutralised if they collide with the shield during transit.

The distance that the charged particles must pass through the shields, > 1mm, is larger than the mean free path of the ions in the plasma, ~0.1mm, see section 6.5.3. Therefore the charged particles must undergo a random walk to pass through the shield, and in this time they could collide with the shield. From kinetic theory of gasses, the total number of these collisions varies linearly with the surface area of the shield.

Each mesh shield can be thought of as having a square unit cell as seen in Figure 68 with length and width 0.6 mm, the sum of the wire thickness, 0.2mm and the hole size, 0.4mm. This has a total area of 0.36 mm^2. Within this unit cell there are two wires with diameter 0.2mm and length 0.6mm. This has a total surface area of 0.75 mm^2. Therefore, for every 1 cm^2 of shielding, there is 2.1 cm^2 of wire.

The grid shield has a square unit cell with length and width 8 mm, and thus an area of 64 mm^2. This unit cell contains a circular hole with diameter 4mm, and a depth of 0.2 mm. Thus the area of grid material in this unit cell, including both sides of the grid and the circumference of the hole is 105 mm^2. Therefore, for every 1 cm^2 of shielding the grid has 1.6 cm^2 of material.

It can thus be seen that for the same sized shield, the mesh has a higher surface area. Therefore, more collisions will occur between charged species and the mesh rather than with the grid. This suggests that the mesh will be more effective at preventing the deposition of charge on the sample surface.

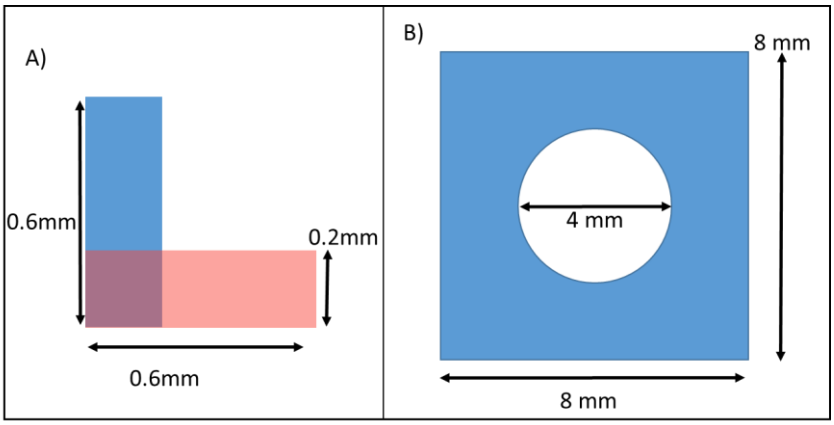


Figure 68 A). The unit cell of the mesh with the two overlaid wires of diameter 0.2mm. B). The unit cell of the grid which contains a circular hole 4 mm in diameter.

6.4.2 Perforated Shielding: Results

As can be seen in Figure 69 there is noticeable improvement when changing to using any shield relative to no shielding. In addition the two shields have slightly different results compared to each other. The grids show the highest increase in lifetime immediately after exposure to the plasma see Figure 69 (A). These lifetimes significantly exceed those of the non-shielded

samples, those shielded by the meshes and those shielded by both the grids and meshes. This lifetime improvement relative to as-received wafers means that the SHP has caused an improvement in chemical passivation, FEP or both, and that this effect is reduced by shielding with a mesh.

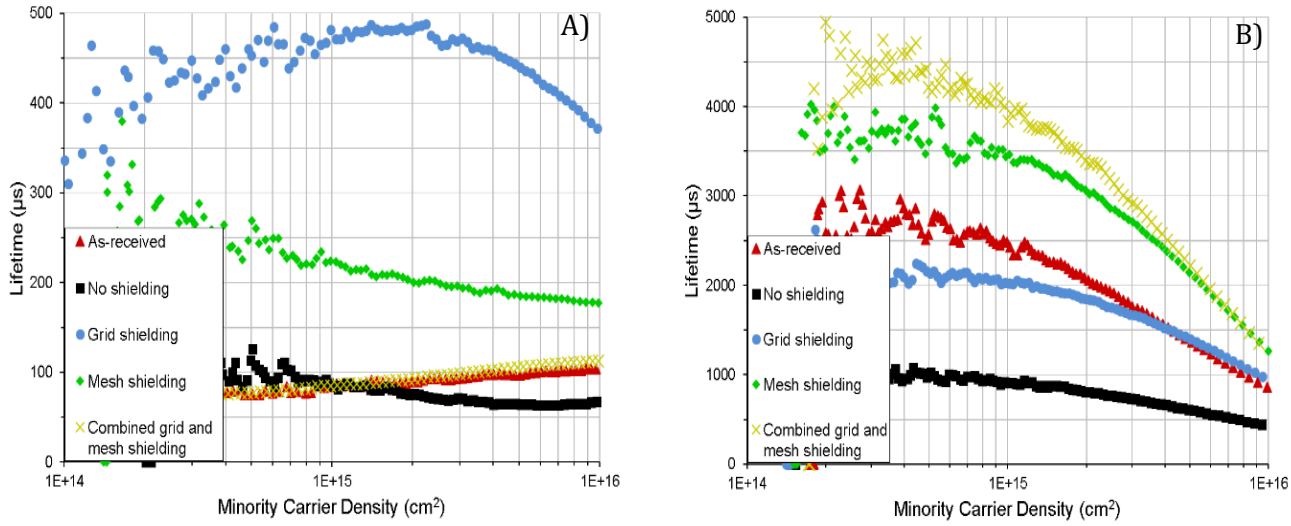


Figure 69. The effect of the SHP process with perforated shields in place. Results from all three shield types are shown as well as samples with no shielding and no processing for comparison. A). How the lifetime is affected by shield type without extrinsic charge supplied. B). How lifetime is affected by the shield type after both the SHP process as well as extrinsic, optimal, FEP. These show some ambiguity regarding the best shield type.

When extrinsic FEP is applied, shielding with the grids ceases to be the most effective method of increasing the final lifetime. Post corona data even shows that samples only shielded by the grids are damaged by SHP. This indicates that damage to the chemical passivation has occurred. It is believed that this was initially not seen in the pre-corona measurements as the effect was more than compensated by the unintentional, simultaneous, application of FEP during the SHP process.

In comparison, samples protected by meshes perform well after extrinsic FEP. The final lifetime increases significantly relative to both, grid protected and samples which did not receive SHP processing. The strong implication of this result is to suggest that SHP has conferred net chemical passivation to these samples. The benefits of SHP were further improved, through the use of both shield types simultaneously. Figure 69 shows that although the pre-corona lifetime

of doubly protected samples shows minimal change compared to unprocessed samples, the final lifetime increases to extremely high levels. It is believed that the best of these results corresponds to a record lifetime for comparable silicon with only a single dielectric coating layer.

It should be noted that one sample which was shielded by both the grids and the meshes simultaneously reached a final, post corona, lifetime of 4500 μs at an injection level of 10^{15} cm^{-3}. However, this result was achieved when using material which was oxidised at a different time to the material used for the rest of this work. It proved impossible to reproduce these lifetimes when using the material available for the bulk of this work. Due to the irreproducibility of this finding it is not presented in more detail.

6.4.3 Perforated Shielding: Discussion

The most important result obtained from the use of the perforated shield is that SHP can be used to increase the lifetime of samples, and this effect remains even after a subsequent application of optimal FEP. As the corona applies optimal FEP to the sample, the change in lifetime observed must be due to chemical passivation of the Si/SiO_2 interface. This improvement is not seen in control samples annealed without plasma so must be due to one of plasma induced species passivating the Si/SiO_2 interface. It is assumed that the species most likely provide this passivation is monatomic hydrogen, in either a charged or uncharged state. This is due to the highly reactive nature, small size and high diffusivity of these species. This assumption is further supported by hydrogen's use in other chemical passivation processes [152].

As hydrogen induced chemical passivation can be seen in the most comprehensively shielded samples, it is believed that it will occur in all other samples exposed to plasma when using perforated shields. However, net chemical passivation may not always occur, as the SHP process may simultaneously introduce damage, which reduces the chemical passivation originally provided by the SiO_2 layer, if this damage is significant the net passivation may be reduced. This

damage is generated by the high energy plasma as no damage is seen if the plasma is not present. In order to further improve SHP the nature of the damage causing processes must be understood and minimised.

The above results also provide information into the nature of the damage created by the plasma. As the lifetime of the grid shielded samples increases immediately after SHP, but does not improve as much as an as-received sample, it is possible to infer that grid protected SHP induces FEP, but reduces the chemical passivation of the wafers, Figure 69. The former means that charged species must be crossing the shield, and reaching the sample, while the latter means that damage mechanisms are still active when using grid shielded SHP. When using the mesh shielding, the post SHP lifetime improvements are minimal, however the samples respond well to extrinsic FEP. The former indicates that very few, if any, charged species are crossing the shield and reaching the samples, while the latter indicates that minimal damage has occurred. This suggests that protecting the samples from the charged species present in the plasma may reduce the damage caused by the plasma. However, as the samples given grid and mesh shielding outperform samples only shielded by the mesh it can be inferred that some damage mechanisms are still active when using the meshes alone. This is unlikely to be charged induced, as the mesh shielded samples appear to be exposed to few charged particles from the plasma. The nature to these damage mechanisms are explored further in the following section.

6.5 Understanding damage mechanisms

As suggested above, it is probable that there are at least two concurrent damage mechanisms, which are tested for in this section. In order to test for these damage mechanisms, a range of experiments not intended to induce optimal SHP were carried out. These tests are designed to evaluate if specific damage mechanisms are active.

As discussed in section 6.1.5, there are a number of potential damage mechanisms which may be active. Electrical breakdown, and physical impingement may occur when charged species from the plasma reach the samples. This charge supply may also result in the deposition of net

charge on the samples. It is likely that electrical breakdown will have a strong temperature dependence, as discussed in section 6.1.5.4. This is unlikely to be the case for physical impingement. UV induced damage should be possible whenever the samples are exposed to the radiation produced by the plasma. It is assumed that chemical attack induced damage in minimal. This is because this damage mechanism should not be prevented by the use of the shields tested above, but they enabled effective passivation, implying this mechanism was not problematic. Furthermore, it is considered unlikely that the species generated by the plasma would be able to break Si/O bonds near the Si/SiO_2 interface.

The following sections detail the work carried out to understand which damage mechanism(s) may be active during SHP. This uses some of the results discussed above, as well as dedicated experiments, and a series of calculations. Understanding these damage mechanisms fully will aid in the development of a better shield which fully protects the samples.

6.5.1 Understanding Damage Mechanisms: Charge Deposition

Both electrical breakdown and physical impingement damage mechanisms can only be active if the surface of the samples are exposed to charged particles. Therefore, demonstrating that the surfaces can become charged by SHP processing can reveal that these mechanisms may be active. As discussed below, there are two strong sets of evidence which suggest that SHP can result in the deposition of charged species at the sample surfaces:

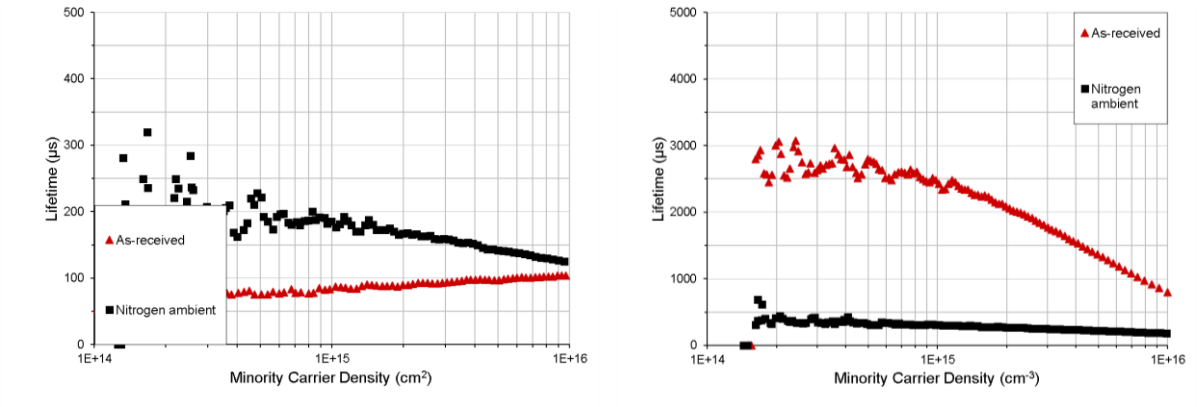


Figure 70. The effect of exposing a sample to a nitrogen based plasma using grid based shielding. Figure A suggests that some passivation initially occurs. As no hydrogen is present this cannot be chemical passivation

so it must be FEP. Figure B supports this as the lifetime gain from the nitrogen plasma is lost when FEP is optimised.

If charged species are reaching the sample from the plasma they will induce FEP, increasing the lifetime of the samples immediately after processing. This effect will occur even if the plasma does not contain hydrogen, and so chemical passivation will not be possible. Therefore, it is possible to unambiguously test if charge deposition occurs. This can be achieved by exposing the samples to nitrogen plasmas. As seen in Figure 70 (left), the lifetimes of samples only protected by the grid shield increases immediately after plasma processing, which can be directly attributed to charge deposition and FEP. In addition, it can seen in Figure 70 (right), that the lifetime of these samples is reduced, relative to samples not exposed to plasma after corona charging indicating that damage to the chemical passivation occurred.

Section 6.4 provides additional evidence that the plasmas can induce surface charging. This section showed that net chemical passivation is increased after shielding the samples with the meshes rather than the grids. This implies that one or more damage mechanisms are at least partially prevented by using the meshes rather than the grids to protect the samples. The primary advantage offered by the meshes is that they will reduce the number of charged particles reaching the samples. As this reduces the damage caused by the processing it can also be inferred that the charged particles can induce damage to the samples.

6.5.2 Understanding Damage Mechanisms: Electrical Breakdown

One of the damage mechanisms which could be caused by the deposition of charge is electrical breakdown. The conductivity of the dielectric layer on the sample is strongly temperature dependent [167]. Consequently, at higher temperatures and conductivities the same rate of supply of charge to the dielectric surface will result in a lower charge density and potential forming. This makes detrimental electrical breakdown less likely to occur. It is not believed that these lower temperatures will have any significant impact on the other damage mechanisms. As seen in Figure 71, low temperature SHP results in significant damage occurring. This implies that electrical breakdown can be an active and important damage mechanism.

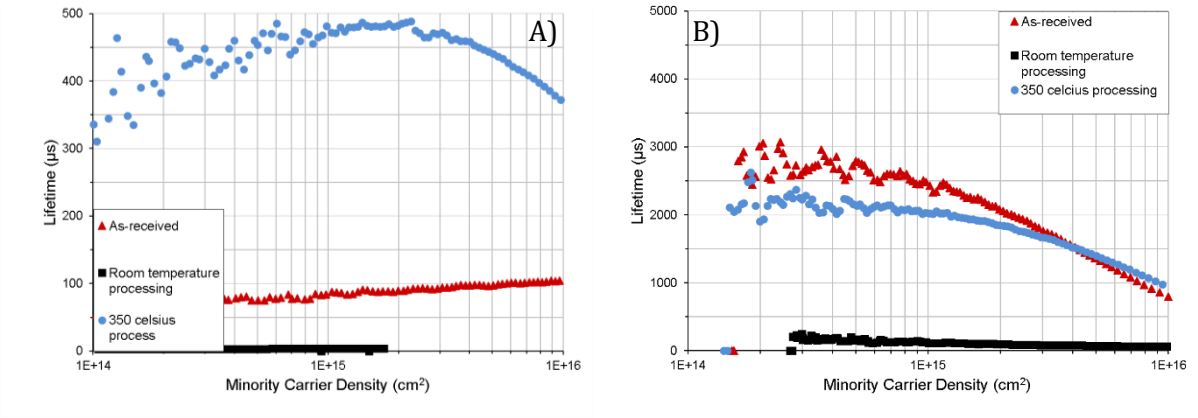


Figure 71. The impact of exposing samples to a plasma at room temperature, versus processing at 350 °C. A). The lifetimes immediately after SHP processing. B). The lifetime after both SHP and optimal corona charging. Both samples given SHP processing were processed for 10 minutes per side with a grid shield in place.

6.5.3 Understanding Damage Mechanisms: Physical Impingement

The other damage mechanism which may be caused by charged particles is physical impingement. Ions are accelerated by the field present between the bulk of the plasma and the earthed containment vessel. An earthed metallic shield which is also electrically connected to the plasma vessel, see Figure 64, forms a Faraday cage around the samples. There cannot be an electrical field within this region, although this region can have a net charge. This means that the charged particles which enter this region cannot subsequently be electrically accelerated. Therefore, any kinetic energy which they lose through collisions with other gaseous species cannot be replaced when the particles have entered the region contained by the shield. It is thus important to identify the mean free path of these species within the plasma.

From the kinetic theory of gasses, the mean free path of both molecules and ions within the plasma can be found by using 6.5.1. The mean free path will be longest for hydrogen ions, as they are the smallest ion in this system. It is assumed that they act as point masses as they are unshielded nuclei, and that the majority of the remainder of the atmosphere is ammonia (a valid assumption as this is the feed-gas, and the fraction of ionised species is small <<1% [165]). It is also assumed that there is no long range interaction between the hydrogen ions and the ammonia, again this is valid as the ammonia molecules are neutral. The temperature of the samples stage is assumed to be the temperature of the gas, and the set pressure of the reaction

chamber is also used. Finally, the assumptions made by the kinetic theory of gases are made including:

- The number of species is large, but the separation is still large relative to their size.
- The molecules move at random with an invariant distribution of speeds.
- All collisions are elastic.
- The molecules obey Newton's laws of motion[130].

6.5.1 $$l = \frac{kT}{\sqrt{2}\pi r^2 p}$$

6.5.1 details the mean free path within a pure gas, where l is the mean free path, r is the radius of the gaseous molecules (ammonia molecule (3.6 angstroms)) and p is the pressure of the system (650 mTorr, 87 Pa). As the hydrogen ions are considered to be negligibly small, the sum of the cross sections of the two colliding particles is reduced from πr^2 to $\pi r^2/2$ in the calculations above.

From this, a mean free path on the order of 10^{-4} m is calculated for the hydrogen ions. This means these species will typically scatter many times while crossing the $\sim 10^{-2}$ m between the shield and the sample. During each collision some kinetic energy can be transferred from the energetic ions to the ambient ammonia molecules. Therefore, when the scattered ions reach the samples they will have thermalized, and will have an energy of 3/2kT which ≈ 0.05 eV. This is very unlikely to damage the sample surface, so physical impingement is unlikely to be an important damage mechanism.

6.5.4 Understanding Damage Mechanisms: Chemical Reaction

In addition to producing charged particles, the SHP plasma will also produce free radicals. These radicals are likely to be $NH_{2\cdot}$ and $H\cdot$ as these will develop when ammonia decomposes, as detailed in 6.5.2. These are highly reactive chemical species which may react with, and alter the silicon/ dielectric interface. Before these species can have any effect they must reach the silicon/ dielectric interface. This means they must first diffuse through the whole dielectric

layer. As thermally grown silicon dioxide is an extremely effective diffusion barrier it is strongly anticipated that this process will be extremely slow, and so negligibly small number of NH_{2}· radicals are likely to reach the interface and as such do not damage the samples. As H· radicals are extremely small, they may still diffuse through the dielectric layer however it is expected that these species will be beneficial and are the reason for this work.

6.5.2 $$\boldsymbol{NH_3 + energy \rightleftharpoons NH_2 + H\cdot}$$

All of the shields trialled in section 6.4 had open structures. These would have been ineffective at preventing exposure of the samples to radicals generated by the plasma as the latter are neutral species so will not be attracted to the shields. However, as seen in Figure 69, these perforated shields protected the samples sufficiently well that SHP improved the chemical passivation of the samples. From this is can be inferred that free radicals generated by the plasma did not cause significant damage to the samples, and it is a damage mechanism which does not need to be focussed on for the remainder of this work.

6.5.5 Understanding Damage Mechanisms: UV Damage

It is possible that UV radiation will degrade samples even when they are protected from all charged, and chemically reactive species. This was tested by carrying out SHP using a 1 mm thick, UV transparent, quartz shield. This shield is an effective barrier to physical bombardment, and electrical effects. Therefore it is expected that UV radiation will be the only damage mechanism which can be active. The lifetime of samples shielded by the quartz decreased after SHP processing, before corona charge was applied, see Figure 72. The sample then improved moderately after corona charging, but still did not reach the levels reached by samples which had received no SHP processing. This shows that UV induced degradation is an active damage mechanism.

As the lifetime of the samples was reduced after the corona charging, relative to samples which were not SHP processed, it can be inferred that the SHP process damaged the samples' chemical

passivation, see Figure 72. This means a damage mechanism was still active. This can only be UV damage as all other potential damage mechanisms will have been prevented by the quartz shield. This shows that UV radiation damage is an important damage mechanisms which must be prevented if the SHP process is to produce the desired results.

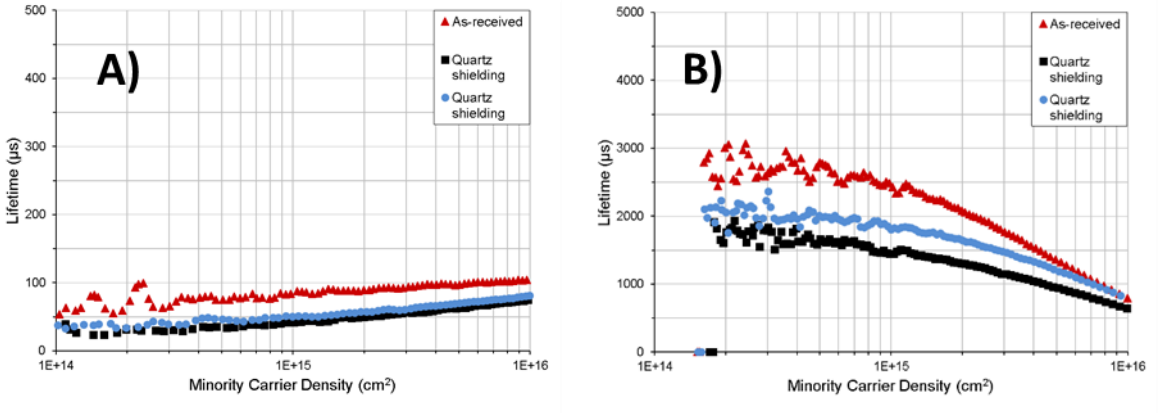


Figure 72. How SHP processing underneath a thick, quartz shield affects the lifetimes of wafers. With this shield in place only two SHP processes may be active, UV radiation damage and dielectric annealing, the latter of which has been shown to have no noticable effect. A). The lifetimes of samples immediately after SHP processing. B). The lifetimes with subsequent full corona passivation. Two separate samples processed for ten minutes under quartz shields are shown. It is clear that the quartz shielding is unable to fully protect the samples from all damage mechanisms.

6.5.6 Understanding Damage Mechanisms: Conclusions

In the previous section is has been seen that there are two damage mechanisms which can be highly important in SHP processing. These are electrical breakdown of the dielectric layer, and damage by UV radiation. This understanding will be used to develop a shield which should enable high quality SHP to be carried out. This will be covered in the remainder of this work.

6.6 Permeable Shielding

As the damage mechanisms active during SHP have been identified it is possible to design an improved shield. This shield must be impermeable to UV radiation, and must prevent charged species from reaching the samples. The shield must also be permeable to the active hydrogen species, which are assumed to be monatomic hydrogen due to the high diffusivity of this species relative to molecular hydrogen [158][159].

Within the SHP plasma there are two monatomic hydrogen species, radicals and ions. As SHP can be effective when using the meshes which prevent ions from reaching the samples (see

Figure 69). Thus it can be inferred that hydrogen radicals are capable of hydrogenating samples in the SHP process.

The shield used in the remainder of this work comprises of a layer which is permeable to the hydrogen species, whilst isolating the samples from any damaging species. This layer is also supported by a separate aluminium structure, see section 6.2.4. The permeable layer had to be:

- Stable under operation conditions including annealing at temperatures up to 400 ^{o}C, and plasma exposure.
- A barrier to UV radiation,
- Impermeable to charged species, suggesting that it should be conductive.
- Sufficiently permeable to hydrogen radicals such that the transport of these active species to the samples was not inhibited to such an extent that SHP could not proceed.

For SHP to be effective, hydrogen radicals must diffuse from outside the shield to the Si/SiO_2 interface. This requires the radicals to cross the permeable shield layer, the gas gap enclosed by the shield, and the SiO_2 layer. While, the net flux will increase when diffusion across any of these layers becomes faster, the most significant improvement will be seen when the most limiting barrier is made more transparent to the hydrogen. Impurity flux will only be acceptable if the diffusivity of hydrogen through the shield layer is high at the process temperatures (300 – 400^{o}C). Impurity flux can be increased by increasing the process temperature as this increases the diffusivity and solubility of hydrogen. If diffusion through the shield limits the flux of hydrogen reducing the thickness of this layer will also be beneficial.

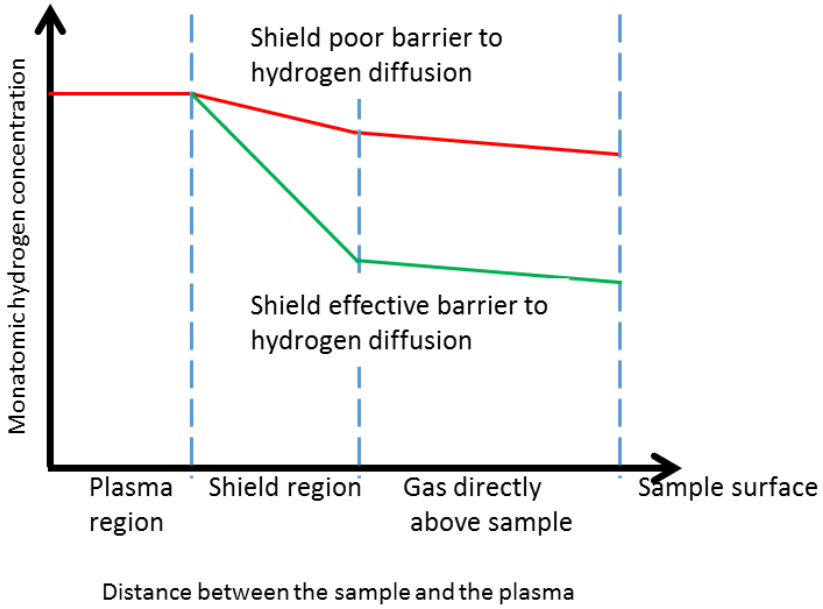


Figure 73. The impact of a shield which provides an effective diffusion barrier to hydrogen (green) compared to one which is an ineffective barrier (red).

99.9% pure palladium leaf was chosen as the permeable layer for the shield. It is a noble metal and did not react with the plasma, and was not noticeably altered by the thermal processing. Like all metals it is conductive and opaque, so is effective at preventing the active damage mechanisms. In addition, hydrogen diffuses rapidly through palladium [168] and the foil used was very thin, (0.2 um) so the flux of hydrogen through this film was anticipated to be high. However, as the palladium leaf is delicate it must be supported when used in the PECVD reactor. The design of this support structure can be found in section 6.2.4. A modification was made to this design part way through this work to maximise area where the palladium was the only barrier between the plasma and the samples see section 6.2.4 for more details.

6.6.1 Permeable Shielding: Proof of Principle

As demonstrated by Figure 74, SHP resulted in net chemical passivation when using the palladium shield. There are a couple of important conclusions which can be obtained from this result. Firstly, chemical passivation can be improved when using the palladium shield, as the SHP process produced wafers which out-performed the as-received wafers, even after both had been given extrinsic FEP. From this result it can be inferred that hydrogen based chemical passivation occurred, and so the hydrogen radicals must have diffused through the palladium

film. This confirmation that the palladium shield is sufficiently permeable to monatomic hydrogen is an important proof of principle for this shield.

The second important result is that minimal damage occurred to the samples when using this shield. This is suggested by the improvement in, post corona, sample lifetime. In addition, Table 14 shows that when the samples are protected by the palladium shield their kelvin probe backing potential did not change, which indicates that the charge on the dielectric did not change. As this test was carried out at room temperatures, the silicon dioxide layer was a very effective insulator, no charge leakage will have occurred. Therefore the lack of charging strongly indicates that the palladium shield protected the samples from charged species.

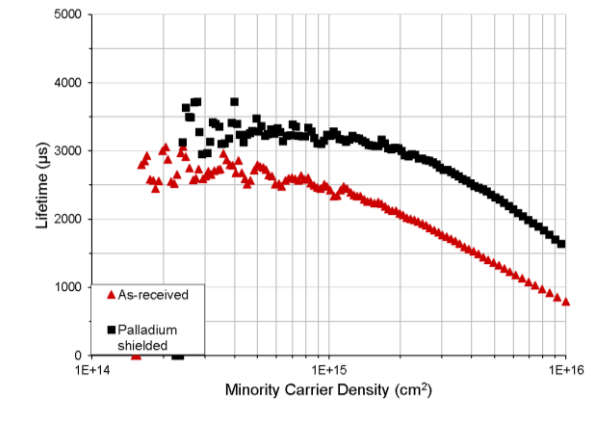


Figure 74. How SHP processing samples underneath a palladium shield affects their lifetimes after optimised FEP, compared to an unprocessed sample. The lifetime increases when using the palladium demonstrating that some passivating species can pass through the palladium leaf.

	As-received samples	SHP processed samples
Backing potential range (V)	0.3-1.0	0.4-1.0

Table 14. Kelvin probe backing potential on the samples before and after SHP processing using the palladium leaf shield, this indicates that the SHP processing deposited negligible charge on the surfaces of the samples. The samples were processed at 22 °C for ten minutes per side with a power of 50 W. This work was carried out by Shiyun Liu, with this author providing supervision.

6.7 Optimisation

Although the permeable shield appears to give good passivation results it is important that the process is optimised further. In this section, a number of process variables are optimised, the processing time, chamber temperature and the electrical power supplied to the plasma. In

addition a number of variations to the shield, including the use of a double thickness palladium layer, and using a more open support structure are described.

6.7.1 Optimisation: Experimental Reproducibility

Variation between samples given nominally equivalent processing is seen. In Figure 75 two samples are separately SHP processed at 400 °C for 30 minutes, it can be seen that they have different resulting lifetimes. It is not clear if this distinction is the result of minor variations in the way the samples are processed, or due to variations in the starting wafers.

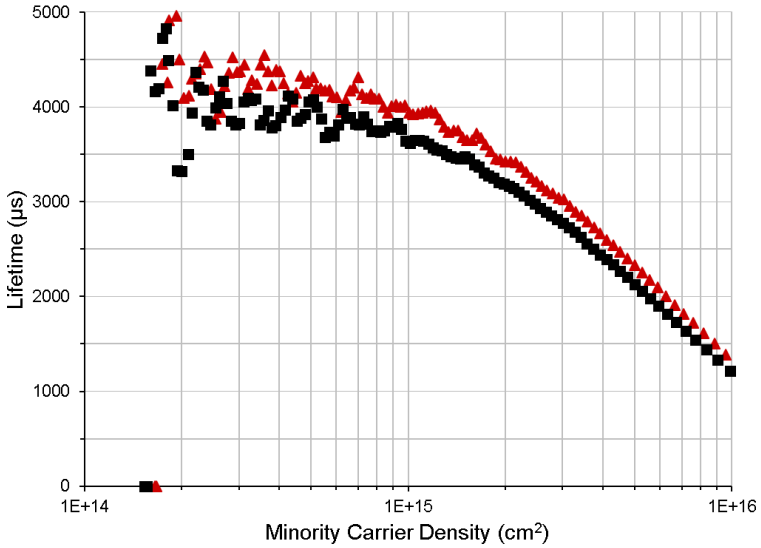


Figure 75. Two nominally identical samples processed under the same shield and with the same plasma conditions. Despite these similarities the two samples have different associated lifetimes.

It is considered likely that some variability in the final results will originate from the starting wafers used. Due to the expense of the samples, maximising material usage was important. Therefore samples with slight shape variations were used. While all of the samples were based upon a square, a number of samples had one corner slightly removed. This can be seen from Figure 76, which highlights the geometry of 3x3 cm samples cut from a 10.16 cm circle, the shape of the received wafers. It can be seen that some of the circumference of the original wafer is now included in the edge of the sample. This was not originally assumed to be important as the area of the edges is significantly smaller than the area associated with the main surfaces. However, it has been suggested that the cleaved surfaces are important when the lifetime of the wafers are increased to the levels achieved in this work, see section 6.7.6. Therefore the samples

cut to contain part of the wafers circumference may give slightly higher lifetimes as they will contain less of these damaging bare surface regions.

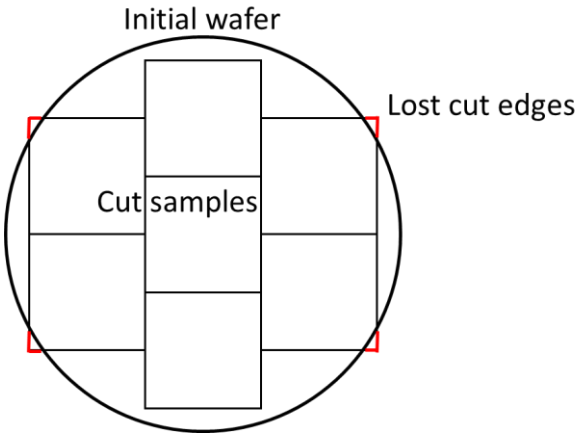


Figure 76. The pattern of samples cut from a 4" (10.16 cm) wafer. The edge wafers can be seen to be missing corners, instead having a section from the circumference of the wafer which has a thermally grown oxide present. The losing of edges therefore reduces the length of bare surfaces present in the edge samples. The missing bare surfaces are seen in red.

6.7.2 Optimisation: PECVD power

It is possible to change the power supplied to the plasma by the PECVD reactor. Increasing the power increases the energy of the plasma. High energy plasmas are likely to contain a higher concentration of energetic species, including ions, high energy photons and hydrogen radicals. As Figure 77 shows, increasing the power is beneficial for SHP. Passivation using only 20 W of power is outperformed by that achieved using 50 W, even when the processing time of the former is longer. This is explained as follows. When the power is increased, more hydrogen radicals are generated outside the shield, and so the flux of impurities through the shield is increased. Consequently, concentration of hydrogen radicals adjacent to the samples is also increased. This has two important effects. Firstly, it will increase the rate at which hydrogen is supplied to the defect sites, and so passivation will be faster. In addition, the increased concentration of hydrogen radicals will alter the equilibrium position of equation 6.7.1 such that more hydrogen is trapped and fewer defects remain un-passivated under equilibrium conditions.

6.7.1 $H^{\cdot} + T \rightleftharpoons TH$

Where $H^{\cdot}$ is a hydrogen radical, T is an un-passivated defect and TH is a hydrogen passivated defect.

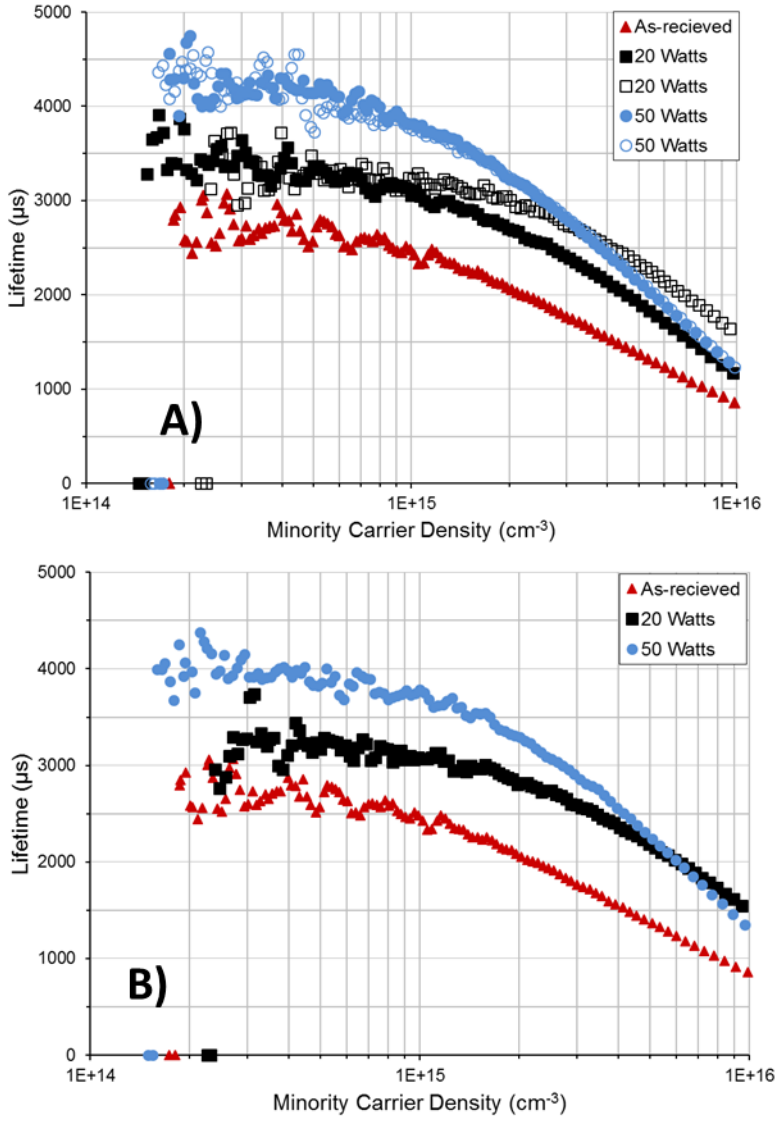


Figure 77. The effect of altering the power supplied to the plasma during SHP upon sample lifetime post FEP treatment. A). Processing at 350°C for ten minutes with two diferent power levels. B). Processing at 350°C for 30 minutes, again with two different power levels.

It was not possible to exceed the power used in Figure 77 due to equipment limitations. This may impose a limit upon the passivation that is possible. A plateau is expected because the maximum concentration gradient across the shield will be limited by the solubility of hydrogen in palladium. When this is reached, a de-coupling between the hydrogen concentration in the plasma, and the hydrogen concentration adjacent to the silicon will be observed.

An alternative hypothesis which might explain why higher powers are beneficial is as follows. When the power supplied to the plasma is increased, the plasma will supply more heat to its surroundings, potentially increasing their temperatures. This effect is likely to have limited impact on the process chamber, and thick aluminium sections of the shield. However, the palladium shield is very thin and so has a low heat capacity per unit area and so the increased heating may notably increase the temperature of the palladium film. As shown below, increasing the temperature of the film increases the flux of hydrogen through, and increases the passivation achieved. This may partially explain why increasing the plasma power increases passivation.

6.7.3 Optimisation: Process temperature

It is possible that increasing the process temperature will have both beneficial and detrimental effects. The major potential detrimental effect is that at higher temperatures the hydrogen will be less effectively trapped by the defect states at the silicon's surfaces. This would result in less complete chemical passivation at elevated temperatures, ie a shift in the equilibrium position of equation 6.7.1to the left. However, increasing the process temperature will also increase the solubility and diffusivity of impurities in both the palladium and the dielectric. This will increase the diffusive flux through these layers so SHP should be accelerated. As shown in Figure 78 and Figure 79, the net effect of higher temperature processing is to increase the passivation offered by SHP. This indicates that the increased flux of hydrogen radicals at this temperature, either through the palladium and/or the dielectric, is important for determining the passivation obtained by SHP.

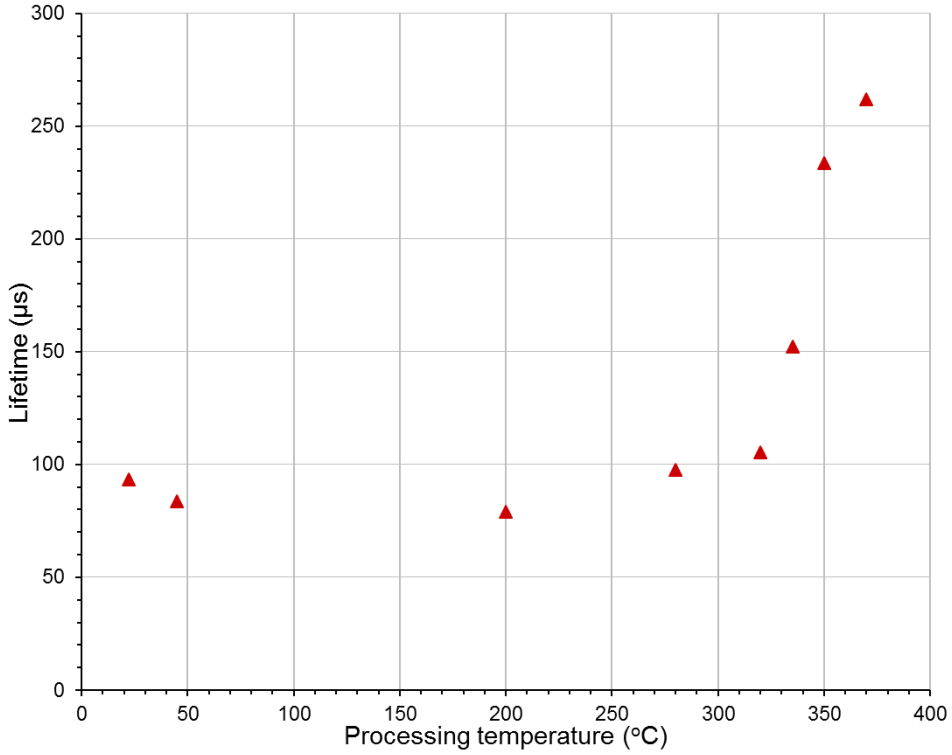


Figure 78. The lifetimes of samples after SHP processing at different process temperatures. All samples were processed using the higher free area shield, and were processed with powers of 50 W. The work was carried out by Shiyun Liu with this author's supervision.

6.7.4 Optimisation: Process time

As anticipated, the processing time has a significant impact upon the effectiveness of the SHP process. This relationship can be clearly seen in Figure 79. From these figures it can be seen that the samples which were only subjected to short SHP processing were passivated less effectively than those processed for longer times. This indicates that diffusion limits SHP efficacy in samples processed for short durations. However, passivation appears to plateau after the samples have been processed for long times. This implies that an equilibrium condition has been reached by this point, and so diffusion ceases to be an important factor determining the SHP efficacy.

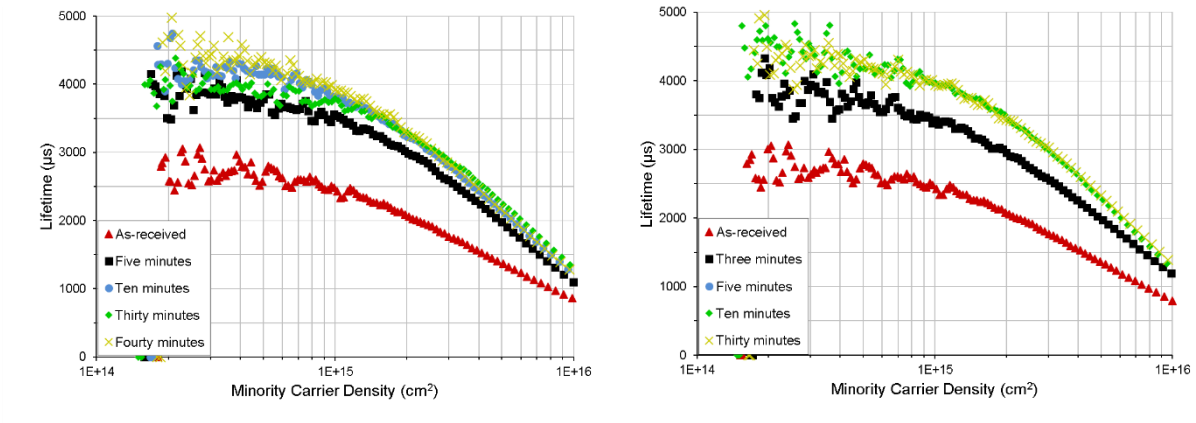


Figure 79. How the passivation extent is affected by SHP processing at different temperatures and durations. All samples were subsequently given optimal FEP. A). Samples processed at 350°C for different times. B). Sample processed at 400°C.

6.7.5 Optimisation: Shield design

A number of variations of the palladium shield were used to find the optimal shield design. Two different aluminium support structures were used, one of these had a higher hole coverage (80%) than the other (18%) and so was expected to have a higher average hydrogen flux. The more open structure only became available part way through this work. As can be seen in Table 15, the more open structure resulted in improved SHP. This is attributed to the increased impurity flux expected from this structure.

In addition, shielding using a single, and double thickness palladium sheet was carried out, to test if the use of a thicker layer of palladium adversely affected the passivation, this used the more open support structure. The use of a double layer would mean that even if one sheet was partially damaged during processing, the samples would still not become damaged as the second sheet would remain intact. This would be advantageous as it was hard to avoid introducing at least pinholes into the palladium sheets during handling. However, as seen in Table 15, using two palladium sheets significantly reduced SHP. This strongly indicates that the diffusion of hydrogen through the palladium film is a major factor limiting SHP rates. If diffusion through these layers was not a major factor limiting SHP speed, increasing the film thickness would have minimal impact.

	Single film, small coverage	Single film large coverage	Double film, large coverage
Pre-corona lifetime µs	157.3	233.7	120.0

Table 15. How the lifetime of samples after SHP but before corona charging is affected by the palladium shield design. Either one or two sheets of palladium where used in series. In addition two different aluminium support structures were used, these had hole coverage of 18% and 80%.

6.7.6 Optimisation: sample geometry

It is possible that the lifetime observed in these samples may be increased if their geometry is changed such that larger samples are used. In this work the samples are cut from a larger, oxidised wafer, and the samples are not annealed again after this point. Consequently the cut edges are unpassivated bare surfaces, which will have high local recombination rates. It has previously been assumed that these edges have minimal importance for two reasons. Firstly the total area provided by these surfaces is a small fraction of the total area of the samples (1.3 % for a 3x3 cm sample with a thickness of 200 µm). Secondly, these edges are located a long way away from most of the sample, and the coil used in the lifetime tester. This means even if the edge created a local "dead zone" region with low lifetimes, this would have minimal effect on the measured lifetime. However, the edges may become important when the sample lifetime is large, and the recombination rate at the passivated surfaces is very low. At these longer lifetimes the distance that minority carriers diffuse before their recombination is increased. Therefore carriers generated further away from these edges may recombine at the edges, increasing the importance of these regions, see Figure 80. This means higher lifetimes may be observed when using larger samples, where the dead regions are less important.

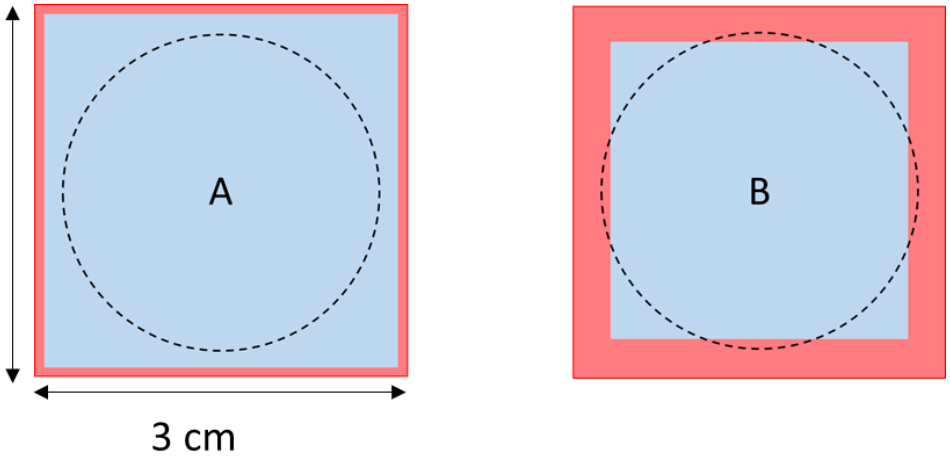


Figure 80. The effect of the "dead zones" created by the existence of cut edges. The blue regions have lifetimes only affected by the bulk and passivated surfaces, the red regions are affected by the un-passivated cut regions, and the dotted circle surrounds the area measured by the lifetime coil. A). A case where the bulk lifetime is low, or the sample is large. As such the measured area is unaffected by the cut edges. B). A case where the sample is only slightly larger than the coil sample area, in addition the bulk lifetime is high, so a large region is affected by the presence of the cut edges. This means the overall lifetime measured is affected by these edges.

6.8 Conclusions and further work

SHP has been introduced as a technique for the extrinsic hydrogenation of silicon/ dielectric systems. Monatomic hydrogen is produced within the plasma, this then crosses a shield before passivating the samples. The shield protects the samples against damage caused by the plasma. The damage mechanisms have been identified as electrical breakdown of the dielectric, and UV radiation. These were effectively prevented through the use of a thin film of palladium.

The palladium shield used is semipermeable to monatomic hydrogen. When using the shield, the chemical passivation of samples is increased, which is attributed to the monatomic hydrogen which has crossed the shield. However, it appears that the passivation rate is strongly affected by the diffusion of hydrogen across the palladium film. Increasing the process time, temperature, plasma power, decreasing the palladium thickness, using a more open shield structure all increase the net chemical passivation. Using a combination of these optimised conditions may enable maximum passivation to be obtained faster.

There are a number of potentially useful additional experiments which could be carried out with respect to SHP, these are as follows:

- It would be useful to try to develop a process which is designed to achieve maximum passivation in a reduced time. It is hypothesised that the use of a higher power plasma, combined with the more open shield structure should be beneficial, and may allow passivation to be achieved more rapidly than was possible in this work.
- A duel temperature SHP procedure could also be developed. This would have a high temperature process where passivation is rapid. During this process the majority of the interface traps would be passivated, however at these temperatures de-trapping can also occur, limiting the maximum passivation possible. Further passivation could then be achieved by cooling the sample to another temperature where diffusion is slower but where the energetics favours more complete trapping.
- It is also important to find the stability of the chemical passivation offered by SHP and to see if these effects can be made more stable through a modification of the processing. This is not a trivial factor to investigate, as extrinsic charge must be supplied to accurately evaluate the chemical passivation. This charge decays, and also can damage the samples if not applied carefully. Either of these effects would falsely indicate that the chemical passivation was lost.
- It is important to test the passivation achievable using SHP as opposed to FGA and rPECVD.
- It is also important to see if higher lifetimes can be achieved when larger wafers are used as these will not be as significantly influenced by the bare edges generated by cleaving the wafers to size.
- It is important to test if SHP can supply hydrogen to defects located within the bulk of a wafer. It is anticipated that this could be useful for reducing recombination by passivating crystallographic defects within a mc-Si wafer, as well as reducing the recombination activity of boron/oxygen complexes [157]. This would enable hydrogen free passivation systems to be used in these systems without affecting the properties of the bulk of the wafers.

7 Conclusions

In this work two techniques for gettering silicon solar cells, as well as one technique for hydrogenating silicon wafers without introducing damage have been introduced. All three of these techniques have slightly different objectives to many processes commonly used in industrial solar cell processing.

In industrial processing, gettering principally occurs as a by-product of another process such as the formation of electrical contacts. As such, none of these processes cannot be fully optimised for gettering, and must fit into the cell manufacturing process. By contrast, SDG, and GPG are stand-alone gettering processes which can therefore be optimised for gettering without affecting the rest of the cell manufacturing process.

The benefits offered by SDG processing are not considered likely to be of major importance for conventional solar cell production, as the costs associated with the additional processing are likely to overcome the benefits of reduced impurity concentrations prior to conventional processing. However, SDG has been seen to be able to confer stable improvements to the lifetimes of wafers from the discarded red zones of mc-Si wafers, and as such it is capable of enhancing these wafers such that they may no longer need to be discarded. Therefore, SDG is capable of increasing the useful yield of a cast ingot, reducing both the economic and energetic wastage associated with discarding otherwise viable cast silicon. Unfortunately, it is hard to ascertain what fraction of the wafer could be recovered and the costs associated with implementing SDG processing. As such the precise advantages of this process cannot be estimated reliably. In addition to reducing the wastage of mc-Si, the SDG process may help to enable the use of UMG-Si for industrial processing. If so, this could significantly reduce the costs associated with the raw silicon used for solar cell production.

Modelling of GPG using Cl_2 has indicated that it should be a very effective technique for gettering a wide range of transition metals. This is supported by experimental finding which show that

GPG significantly improves the lifetimes of mc-Si wafers, and also greatly reduces the concentration of iron in solution within the wafers. As these gains have been made without removing any material beyond the saw damage, this technique may already be useful for processing mc-Si based solar cells.

Despite the promising experimental findings obtained in this work, it is thought that the full potential of this technique has not yet been revealed. It has been inferred from surface wetting and etch rate experiments that a silicon dioxide layer formed near the start of the GPG thermal process. This will have reduced the efficacy of GPG. As such, it is to be expected that if unintentional oxidation of the surface could be avoided, GPG would be significantly more effective, although etching of the silicon would also be accelerated. It is not clear how reducing the oxidation rate would affect the net advantage of the GPG process, although it is thought that gettering could be greatly enhanced before GPG removed an undesirably thick layer of silicon, as the saw damage layer is quite thick- ~10μm- and must be removed as part of further cell processing.

One of the major advantages of Cl_2 GPG is that is has been seen to be effective at temperatures in excess of 1000 ^{o}C. This means that it can be used at temperatures where other gettering processes would have become ineffective. This is significant as it means that at possible process temperatures, precipitate dissolution will be more advanced and rapid. As such Cl_2 GPG may be able to getter a larger fraction of all impurities in a wafer than possible via conventional gettering processes. It is therefore thought that GPG may be an effective additional gettering process for a wide range of silicon solar cell applications.

SHP has been introduced as a technique to enhance the chemical passivation of silicon wafers. As part of this work the mechanisms which can lead to plasmas damaging silicon/silicon dioxide layers have been investigated. This work has clearly identified two separate damage mechanisms which are simultaneously active, and as such it is thought that it provides a clearer understanding of this system than has previously been achieved.

SHP has been seen to be an effective mechanism for exposing samples to monatomic hydrogen. It is likely that this will provide significant advantages to any passivation scheme, as SHP is both a highly effective technique for improving chemical passivation, and has minimal effect on pre-existing passivation layers. As such it could be readily applied to improve a wide range of different passivation schemes where it could be used as an extrinsic source of chemical passivation. It is expected that this will be particularly useful for high efficiency cells as surface recombination is a more important phenomenon in these systems. However, it is anticipated that SHP could also be used on lower efficiency cells. In these applications it could be used to enable the passivation of bulk defects including dislocations and grain boundaries.

8 References

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