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Electron mobility enhancement in solution-processed low-voltage In₂O₃ transistors via channel interface planarization

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The quality of the gate dielectric/semiconductor interface in thin-film transistors (TFTs) is known to determine the optimum operating characteristics attainable. As a result in recent years the development of methodologies that aim to improve the channel interface quality has become a priority. Herein, we study the impact of the surface morphology of three solution-processed high- k metal oxide dielectrics, namely AlO_x, HfO_x, and ZrO_x, on the operating characteristics of In₂O₃ TFTs. Six different dielectric configurations were produced via single or double-step spin-casting of the various precursor formulations. All layers exhibited high areal capacitance in the range of 200 to 575 nF/cm², hence proving suitable, for application in low-voltage n -channel In₂O₃ TFTs. Study of the surface topography of the various layers indicates that double spin-cast dielectrics exhibit consistently smoother layer surfaces and yield TFTs with improved operating characteristics manifested, primarily, as an increase in the electron mobility (μ). To this end, μ is found to increase from 1 to 2 cm²/Vs for AlO_x, 1.8 to 6.4 cm²/Vs for HfO_x, and 2.8 to 18.7 cm²/Vs for ZrO_x-based In₂O₃ TFTs utilizing single and double-layer dielectric, respectively. The proposed method is simple and potentially applicable to other metal oxide dielectrics and semiconductors. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/1.5036809>

The development of high carrier mobility semiconductors¹⁻³ is only one necessary component of solution-processed, low-temperature and low-voltage thin-film transistors (TFTs). In fact, low-voltage operation of TFTs is more dependent on the use of a high capacitance dielectric and an often-overlooked component, at least in the field of large-area electronics. Experimentally silicon dioxide (SiO₂) on highly doped p-type silicon wafers (Si⁺⁺) is commonly used since it acts as an integrated gate contact and dielectric. However, the weakness of SiO₂ is its low relative dielectric constant (k) of 3.9 and fabrication cost due to the vacuum-based processing.⁴ Hence, replacing SiO₂ with a high- k material will enable the development of TFTs with lower operating voltages, and hence power consumption, that are suitable for low-power logic applications.

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Multiple metal oxides have been proposed as alternatives to SiO_2 including aluminium oxide (AlO_x),^{5,6} hafnium oxide (HfO_x),^{7,8} and zirconium oxide (ZrO_x),^{9,10} all of which have higher dielectric constants. These alternative metal oxide dielectrics can also be produced from solutions by employing analogous routes to those used by solution-processed metal oxide semiconductors. Furthermore, the selection of dielectric has been shown to affect more than just the operational voltage and leakage currents within devices. Significantly, there exist multiple reports demonstrating a dielectric dependence to the charge mobility of semiconductors.^{11,12} Yet, the mechanisms used to explain these differences vary greatly, from templated growth,¹³ to interfacial trap states,¹⁴ and planarization of the interface.¹⁵

In this work, we present a direct comparison of In_2O_3 TFTs and dielectric-only capacitors, produced with single and double layers of three different materials namely; AlO_x , HfO_x and ZrO_x . Both the semiconductor and dielectric layers were solution-processed at temperatures $\leq 200^\circ\text{C}$ via spincoating. The dielectric films were produced from the precursors of aluminium nitrate hydrate,¹⁶ hafnium chloride,¹⁷ and zirconium oxynitrate hydrate,¹⁸ chosen due to their proven compatibility with 2-methoxyethanol or other alcohols. The semiconductor solution consisted of indium nitrate hydrate in 2-methoxyethanol.^{1,19} By employing identical fabrication techniques for each dielectric, the electron mobility within the subsequently deposited In_2O_3 film can be directly compared. From this we observe a significant increase in semiconductor mobility with decreasing interface roughness as a result of the double-step coating of the dielectric layer, as well as an empirical relationship between dielectric material and TFT mobility. To avoid specialized and expensive substrates all devices were produced using thermally evaporated Al bottom gate contacts on Borofloat glass substrates. Figure S1a-e in the [supplementary material](#) shows that aluminium provides a much rougher surface (root mean squared (RMS) roughness R_{RMS} of 1.7 nm) when compared to SiO_2 ($R_{RMS} = 0.4$ nm), doped silicon ($R_{RMS} = 0.2$ nm) or Borofloat glass ($R_{RMS} = 0.2$ nm). The surface roughness of the aluminium gate electrodes was reduced by simply increasing the evaporation rate to 3 Å/s under high vacuum conditions (10^{-6} mbar). Figure S1f ([supplementary material](#)) shows the evolution of the surface R_{RMS} for Al gate electrodes as a function of deposition rate. On the basis of this result the deposition rate of 3 Å/s was chosen for the processing of all Al gate electrodes throughout this work.

The coverage of the six dielectric configurations on top of aluminium gate contacts was studied using atomic force microscopy (AFM). $1\ \mu\text{m} \times 1\ \mu\text{m}$ topography images are presented in Figure 1a–c with a matched height axis between all scans. The HfO_x consistently produced the smoothest films for both single and double layers, followed by ZrO_x , whilst AlO_x produced the roughest films. For each dielectric material, a second spincoated layer reduced the film roughness significantly as seen in the height distributions in Figure 1d–e and the RMS roughness. This planarizing effect is not only ideal for reducing the impact of the rough aluminium gate contacts, but it also improves the dielectric/semiconductor interface which strongly affects the charge carrier transport in TFTs. Deposition of additional dielectric layers via sequential spin casting did not lead to further TFT improvement both in terms of electron mobility and gate leakage current.

The thicknesses of the six dielectric configurations produced on $\text{SiO}_2/\text{Si}^{++}$ substrates were measured using ellipsometry. Values and their corresponding errors were calculated by starting from optical models in Woolam's WVASE software database and allowing for optimization of both thickness and optical constants. These results are shown in Figure 1f, and demonstrate a doubling in film thickness for the AlO_x and ZrO_x films upon deposition of a second layer. However, for the HfO_x film, the error bars on the measurement of thickness indicate that the second layer produces a less than proportional increase in thickness.

To characterize the breakdown electric field and capacitance of each dielectric layer, metal-dielectric-metal capacitor structures were fabricated. The capacitors consisted of the six dielectric configurations between perpendicular rectangular (18 mm by 0.8 mm) aluminium top and bottom contacts, producing capacitors with device area of (0.8 mm by 0.8 mm) $0.64\ \text{mm}^2$. Figure 2a contains box plots of the breakdown fields for 10 devices of each dielectric configuration. The single layer ZrO_x exhibits the highest breakdown field, closely followed by the single layer of AlO_x , whilst the single layer HfO_x performs the worst. It would be expected that by doubling the number of dielectric layers the breakdown field would remain unchanged, leading to a doubling in the breakdown voltage due to increasing thickness, yet this was not observed. Instead, upon addition of a second dielectric

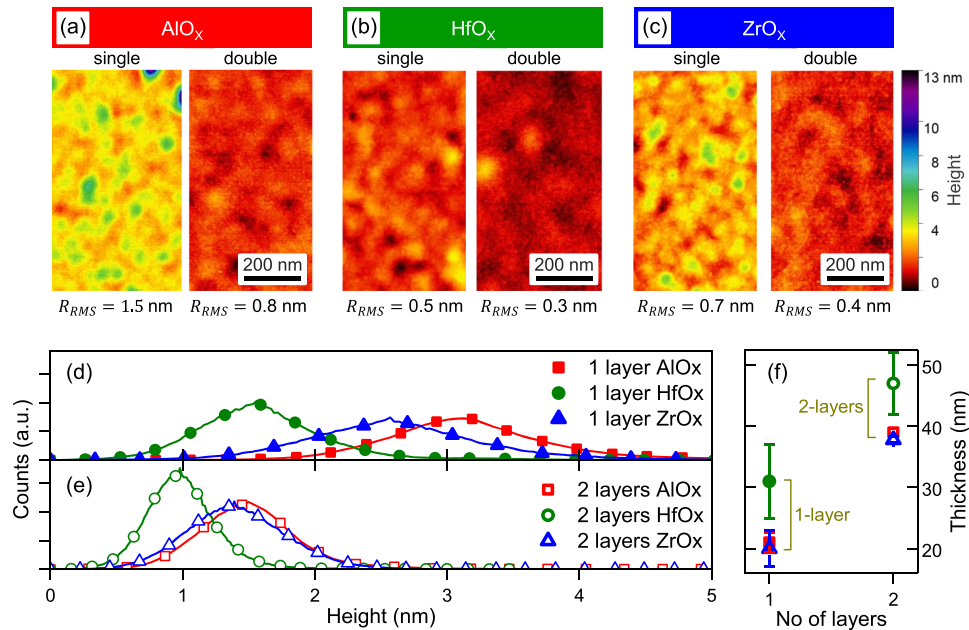


FIG. 1. AFM scans ($1 \mu\text{m} \times 1 \mu\text{m}$) of: (a) AlO_x , (b) HfO_x , and (c) ZrO_x . Also included are height distributions of the single (d), and double (e) layers AFM topography scans. (f) The thickness of each dielectric layer was calculated via ellipsometry.

layer, the breakdown field decreased for all dielectric materials, though the variation also decreased. Furthermore, even the mean breakdown voltage decreased for AlO_x capacitors upon the addition of a second layer.

Avis *et al.*²⁰ have previously demonstrated, via high resolution transmission electron microscopy, the existence of an interface between subsequent spincast layers of dielectric. It is proposed that this interface presents a potential source of instability, for example, by causing a non-uniform distribution of the electric field across the dielectric. This intermediate layer may reduce the voltage required to break the capacitor, hence explaining the lower breakdown fields of the double layer dielectrics within this work.

Capacitance measurements were performed on identical devices to those tested for the breakdown field. Three devices were measured for each dielectric configuration as shown in Figure 2b and the areal capacitance was taken from the mean at 100 Hz. From Figure 2b HfO_x and ZrO_x single and double layers exhibit repeatable results with a frequency stable capacitance at lower than 10^5 Hz with a drop off above this frequency due to the low pass filter nature of the experimental setup. All double layer films exhibited lower capacitance, as expected from the increased thickness, though the difference between the capacitance of single and double layers was not completely proportional to the thickness of each layer. Similar to the changes in the breakdown field and voltage, the cause could be due to the interface between the two sequentially deposited layers, producing a difference between the calculated relative permittivity values for single and double layers of each high- k dielectric (Table I).

AlO_x films exhibited the common feature²¹ of increasing capacitance at lower frequencies with two possible origins. Previous reports assigned this to either, (i) the rotation of trapped solvent in the film¹⁶ increasing the dielectric constant at lower frequencies, or (ii) the movement of hydrogen ions producing an electric-double-layer (EDL).²² Although this increasing capacitance gives the AlO_x film the highest capacitance at the low frequency range, it is also an indication of a relatively unstable dielectric with decreasing performance at high frequencies.

TFTs were fabricated using the six dielectric configurations with a single spincast layer of In_2O_3 as the semiconductor (Figure 3a). Multiple TFTs were produced for each configuration, all with channel width (W) $1000 \mu\text{m}$ and channel lengths (L) in the range $30\text{-}50 \mu\text{m}$. Figure 3b shows representative transfer characteristics for transistors with W/L of $1000/50 \mu\text{m}$ for each dielectric material

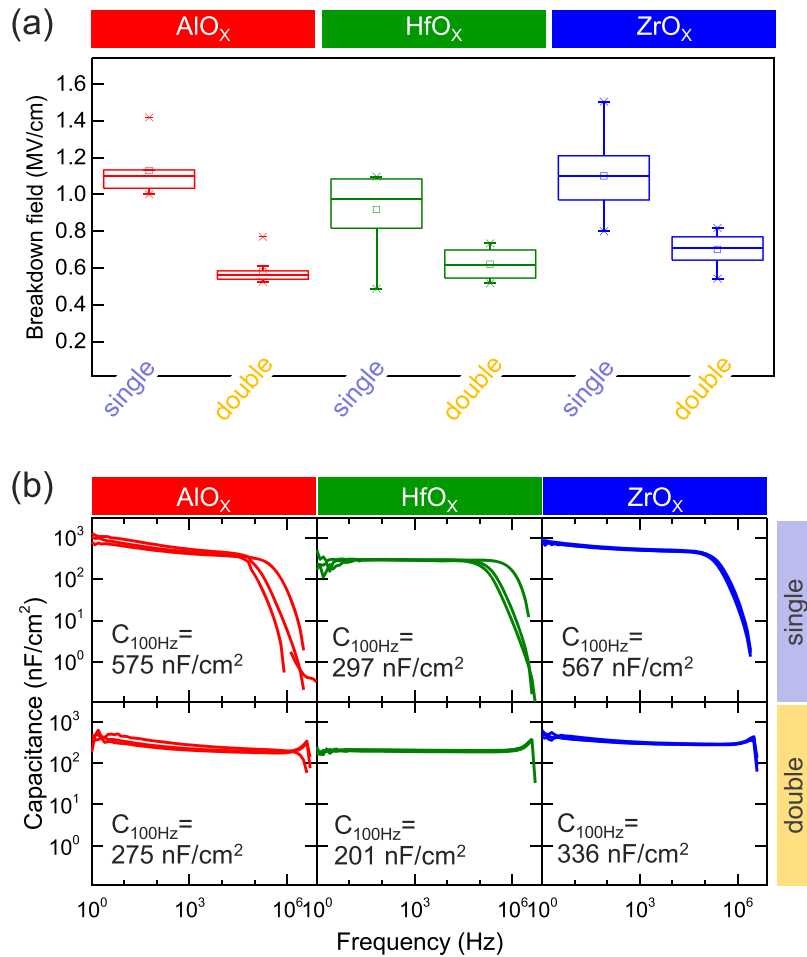


FIG. 2. (a) Statistical distributions of the breakdown (BD) field acquired from sets of 10 devices fabricated in parallel. (b) Capacitance vs. frequency measurements for each dielectric system investigated and the mean value measured at 100 Hz.

and configuration (single and double spincast). There is an obvious difference in the maximum drain current (I_D), dependent on the selection of dielectric with ZrO_x and AIO_x exhibiting the highest and lowest currents, respectively. Also, drain current hysteresis is exacerbated upon addition of a second layer, an effect most apparent in the ZrO_x-based In₂O₃ TFTs. The latter is attributed to the

TABLE I. Summary of properties of capacitors and TFTs made using single and double layers of AIO_x, HfO_x and ZrO_x. Trap states were calculated from the mean of results from Eq. 1 whilst ignoring negative outliers.

Parameter	AIO _x		HfO _x		ZrO _x	
	1 layer	2 layers	1 layer	2 layers	1 layer	2 layers
Capacitance (nF/cm ²)	575 ± 77	275 ± 43	297 ± 5	201 ± 7	567 ± 18	336 ± 16
Thickness (nm)	21 ± 1.7	39 ± 0.7	31 ± 6	47 ± 5	20 ± 3	37.8 ± 0.5
Calculated ε _r	13.6 ± 2.1	12.1 ± 1.9	10.4 ± 2.0	10.7 ± 1.2	12.8 ± 2.0	14.4 ± 0.7
ε _r reported in the literature ^a	9 - 10	9 - 10	20 - 25	20 - 25	20 - 25	20 - 25
Breakdown field (MV/cm)	1.13 ± 0.13	0.58 ± 0.05	0.92 ± 0.24	0.62 ± 0.10	1.10 ± 0.23	0.70 ± 0.07
Electron mobility (cm ² /Vs)	1.0 ± 0.5	2.0 ± 1.2	1.8 ± 0.5	6.4 ± 5.5	2.8 ± 0.9	18.7 ± 16.0
Threshold voltage (V)	0.54 ± 0.27	0.45 ± 0.30	0.50 ± 0.26	0.25 ± 0.43	0.30 ± 0.23	0.09 ± 0.43
Subthreshold swing (V/dec)	0.10 ± 0.06	0.17 ± 0.11	0.16 ± 0.13	0.26 ± 0.37	0.15 ± 0.07	0.26 ± 0.31
Areal trap states (cm ⁻²)	4.3 × 10 ¹²	3.6 × 10 ¹²	3.5 × 10 ¹²	4.4 × 10 ¹²	5.7 × 10 ¹²	7.6 × 10 ¹²

^aLiterature values for the permittivity range for each material were taken from Manchanda *et al.*³³

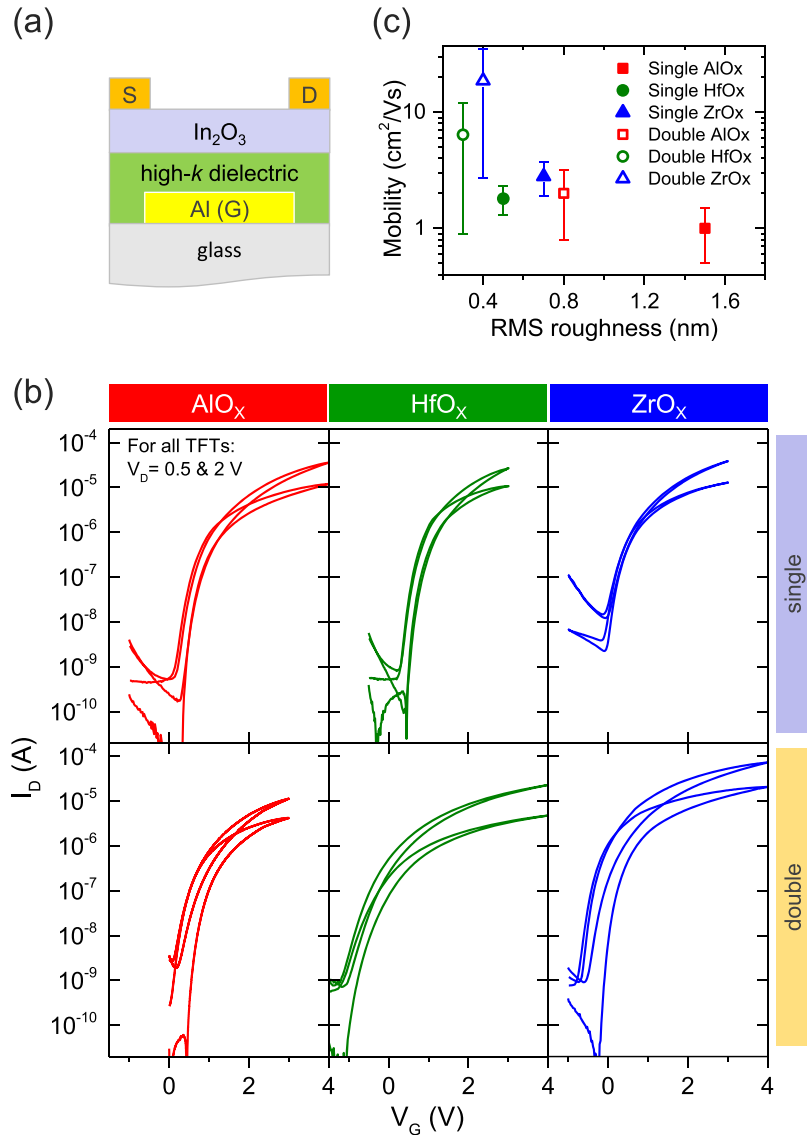


FIG. 3. (a) Schematic of the TFT architecture used. (b) Transfer characteristics of In₂O₃ TFTs measured at V_D of 0.5 V and 2 V. Here the drain currents is represented by the solid lines and the gate currents by the dashed lines. (c) Mean electron mobility as a function of RMS roughness for over 24 devices of each dielectric layer (statistical box shown in Figure S2, supplementary material).

relatively low annealing temperature employed ($\leq 200^\circ\text{C}$) and the incomplete precursor conversion to the targeted oxide.

The trends evident in the transistor characteristics of Figure 3b carry through to the statistical analysis of mobility presented in Figure 3c. First, the dielectric dependence of the maximum I_D obtained, translates to a dielectric dependence of mobility. Specifically, the In₂O₃ exhibited the lowest values of mobility when deposited on AlO_x, and the highest values of mobility when deposited on ZrO_x. Secondly, the larger maximum I_D in double layer devices, is observed as an increase in In₂O₃ mobility with the addition of a second layer for each dielectric. It should be noted that, while the spread in results of mobility is large, the difference in mean values is too significant to be assigned to error in the measurement of the gate dielectric capacitance.

Three possible mechanisms between the semiconductor and dielectric are often cited to explain a dielectric dependence of carrier mobility and include: i) interfacial trap states,^{23–25} ii) templated growth at the interface,²⁶ and iii) planarization of the interface.^{11,12,15} Each of these three mechanisms

can affect the carrier mobility within the channel of a TFT, and all are dependent on the quality of the interface between the dielectric and semiconductor. Interface trap states are specifically due to the bonding interaction between semiconductor and dielectric.²⁷ They include impurities and imperfections at the semiconductor/dielectric interface which trap charge carriers, reducing the channel mobility. The more trap states there are, the greater the fraction of trapped charge, and the lower the measured field-effect mobility.¹⁴ Templated growth occurs when the matched lattice spacing at an interface produces greater crystallinity within the second of the deposited layers. If the first deposited layer is the dielectric and the secondary layer is the semiconductor, this may increase mobility due to the larger crystallite size, with one example being the growth of cadmium oxide (CdO) layers, albeit using metal-organic chemical vapor deposition.¹³ Finally, planarization/smoothing of the interface also represents an extremely important factor that can affect TFT operation. In particular, a rough interface with large topographical variations, greater than the charge accumulation depth, provides electrostatic boundaries for charge carriers that must be overcome, reducing the channel conductivity.¹² Indeed, smoothing of the semiconductor/dielectric interface has been shown to increase in the carrier mobility down to a minimum surface roughness.²⁸

On the other hand, the effects of interfacial trap states are hard to isolate from the bulk trap states within a semiconductor. Although methods exist to separate the two, they rely on specialized techniques such as ionizing radiation,²³ temperature dependent capacitance measurements,²⁴ or photo-excited charge-collection spectroscopy.²⁷ To this end, simpler methods that are directly applicable to TFTs include trap state density estimation via subthreshold slope analysis,²⁹ as well as the more detailed Grünwald analysis.^{30,31} Although these cannot distinguish the bulk from interface states, they do provide an indication of the energetic trap states within the active channel, including the interface. To analyze the results from our experiments the following equation was used:³²

$$N_{t,areal} = \frac{C_{ins}}{q} \left(\frac{q SS \log_{10}(e)}{k_B T} - 1 \right), \quad (1)$$

Here, $N_{t,areal}$ is the areal density of trap states, C_{ins} is the areal capacitance of the insulator, SS is the subthreshold swing and q , k_B , and T are the elementary charge, Boltzmann constant and experimental temperature respectively. Extracted values of subthreshold swing that produced negative values of trap states were treated as erroneous outliers caused by experimental error. The mean values for the areal density of trap states together the various other dielectric, capacitor and transistor parameters are summarised in Table I. Ranges of previously reported ϵ_r values are also provided for the three dielectrics for comparison.³³ Based on this analysis, no trend between the interface trap states and the empirical dielectric dependent mobility could be established.

Templated growth at the dielectric/semiconductor interface is another possibility that can affect carrier mobility. Previous literature provides x-ray diffraction (XRD) data for AlO_x films, processed from aluminium nitrate hydrate in 2-methoxyethanol, demonstrating its amorphous nature at temperatures up to 500 °C.^{16,18} Similar XRD studies on HfO_x films, produced from HfCl_4 in various alcohols, exhibited no obvious crystalline peaks, leading the authors to assume it is amorphous as well.^{20,34} Yet further research, using grazing incidence x-ray diffraction (GIXRD)¹⁷ showed that a higher temperature (450 °C) spray-coating technique, also using the precursor of HfCl_4 , produced a monoclinic polycrystalline film with small crystallite sizes of <10 nm. Finally, XRD measurements performed on ZrO_x films produced from zirconium oxynitrate in H_2O with a co-solvent of 2-methoxyethanol at low-temperatures of ≤ 150 °C¹⁸ exhibited only short range order, and no long-range crystallinity. Therefore, on the basis of previous literature it may be loosely assumed that the AlO_x films produced in this work are likely amorphous, while the HfO_x and ZrO_x films may potentially exhibit short range order in the form of nanocrystals. This does not lend itself to any clear conclusions on templated growth of these films and concrete experimental results are required to further this line of research.

Finally, the increase in the electron mobility, upon addition of a second dielectric layer, is most likely due to the smoothing of the dielectric/semiconductor interface. This has previously been demonstrated with solution-processed layers,³⁵ though the latter work did not conclusively deconvolute the effect of decreased interfacial trap states from the different materials used. Here, the spincoating of a single or double dielectric layers makes it possible to correlate the carrier mobility

with the roughness of the channel interface. However, planarization cannot be the only mechanism as it does not explain the material dependence of mobility values in Figure 3b. For this reason, further investigations into the crystallinity and also the semiconductor/dielectric interface is required to elucidate the full mechanism.

In summary, we have studied the influence of surface roughness of several different high- k dielectrics, namely AlO_x , HfO_x , and ZrO_x , on the electron mobility of solution-processed In_2O_3 TFTs. Transistors based on smooth layers of ZrO_x were found to exhibit the highest electron mobility of $18.7 \text{ cm}^2/\text{Vs}$. On the other hand, TFTs based on optimised HfO_x dielectric layers were shown to combine good electron mobility ($6.4 \text{ cm}^2/\text{Vs}$) and improved on/off current ratio ($\approx 10^5$), with higher breakdown field. Irrespective of the dielectric material employed, electron mobility was found to increase with decreasing channel interface roughness. The simple channel planarization method described here provides a straightforward, yet effective, approach for improving the performance of TFTs based on In_2O_3 , and potentially other metal oxide semiconductors.

See [supplementary material](#) for additional sample preparation and characterization, device fabrication and characterization, and additional experimental results.

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