Stable Organic Static Random Access Memory from a Roll-to-roll Compatible Vacuum Evaporation Process

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ABSTRACT:

An organic Static Random Access Memory (SRAM) based on p-type, six-transistor cells is demonstrated. The bottom-gate top-contact thin film transistors composing the memory were fabricated on flexible polyethylene naphthalate substrates. All metallization layers and the p-type semiconductor dinaphtho[2,3-b:2',3'-f] thieno[3,2-b]thiophene were deposited by thermal evaporation. The gate dielectric was deposited in a vacuum roll-to-roll environment at a web speed of 25 m/min by flash-evaporation and subsequent plasma polymerisation of tripropyleneglycol diacrylate (TPGDA). Buffering the TPGDA with a polystyrene layer yields hysteresis-free transistor characteristics with turn-on voltage close to zero. The static transfer characteristic of diode-connected load inverters were also hysteresis-free with maximum gain >2 and noise margin ~2.5 V. When incorporated into SRAM cells the time-constatnt for writing data into individual SRAM cells was less than 0.4 ms. Little change occurred in the magnitude of the stored voltages, when the SRAM was powered continuously from a -40 V rail for over 27 hours testifying to the electrical stability of the threshold voltage of the individual transistors. Unencapsulated SRAM cells measured two months after fabrication showed no significant degradation after storage in a clear plastic container in normal laboratory ambient.

Key words: Organic electronics, thin film transistors, inverters, SRAM

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1. Introduction

The potential of organic/plastic electronics for fabricating large-area electronics (LAE) [1] on flexible substrates with different form factors, has created major new directions for electronic product design and applications. The key driver is the ability of organic materials to form robust films on thin, flexible substrates using low temperature production processes. Significant progress is now being made in fabricating circuits ranging from multistage ring oscillators (see for example [2-5] and references therein) and logic gates [6,7] through to 8-bit microprocessors [8], 8-bit transponders [9] and programmable logic arrays [10].

The ability to store data, either temporarily or semi-permanently, is an important requirement for many electronic circuit applications. Not surprisingly, then, many different types of organic memory devices have also been reported e.g. switchable resistive memory [11,12], floating gate memory devices [13] and memory transistors [14]. Also reported are organic versions of dynamic [15] and static [16-19] random access memory i.e. DRAM and SRAM respectively.

SRAM is an essential component of silicon-based electronics. For example, it is used in cache memories, microprocessors, systems-on-chip and applications for which speed is more important than capacity. Although SRAM is a volatile memory, so long as it is connected to a voltage supply, the stored data is stable for long periods and, unlike DRAM, does not require regular refreshing. Hence the larger cell area, accommodating two cross-coupled inverters and two access transistors (6-T SRAM), is partially compensated by removing the 'refresh' circuit requirement. Furthermore, in organic LAE applications, integration density is significantly lower than for silicon circuits so that achieving good operational speed is of greater importance than smaller cell size.

An early report on organic SRAM was by Takamiya et al [17] who used a 12 x 12 array of 5-T write-only pentacene-based SRAMs to overcome the slow actuator transition rate in a Braille sheet display. The same approach was used in a later publication [18] in which faster SRAMs were fabricated from low-voltage transistors based on the more stable semiconductor dinaphtho[2,3-b:2',3'-f] thieno[3,2-b]thiophene (DNTT) [20] deposited onto a thin aluminium oxide dielectric capped with a self-assembled monolayer [21]. Only a few other reports on SRAMs have appeared, notably by Kumar et al [19] on the design and performance analysis of 6-T organic and hybrid (organic/oxide) SRAMs and Guerin et al [16] who fabricated a complementary 6-T SRAM using p-type polytriarylamine and an n-type acene-diimide.

To date most organic circuits have been produced using small-scale laboratory-based techniques involving electrodes defined by shadow mask or photolithography and with the organic semiconductor deposited by spin-coating or vacuum-evaporation. A wide range of dielectrics have been used including both organic and inorganic, with the former generally being deposited by spin-coating. Solution-based mass-printing technologies have been reported [22,23] for organic LAE production. The best circuit performances, though, have been achieved using batch-processing approaches derived from silicon technology [5,24-26] and applied under clean room conditions. Such processes, however, require many deposition and patterning steps. For example, the basic transistor array reported by Sou et al [10] required 10 process steps with additional steps then necessary for the e-display and ink-jet printed interconnects for programming the logic array.

It has been suggested that a vacuum roll-to-roll (R2R) process, in which all layers are vacuum-evaporated [36], could provide the route to fewer production steps and better circuit performance than achieved to date using mass-printing methods. Clear benefits of vacuum-evaporation include solvent-free production, high deposition rates and high yield. Furthermore, deposition and patterning methods compatible with R2R production are already available for each layer [27] and allow significant reduction in the number of process steps. In the following, we show that R2R-compatible, vacuum-evaporation processes can be used to produce stable organic SRAM arrays with good response times.

2. Experimental

Single 6-T SRAM cells and 4x4 SRAM arrays were fabricated on pre-cleaned 125 μm thick polyethylenenaphthalate (PEN) film (Dupont-Teijin Ltd). The circuits (Figure 1) were based on p-type, bottom-gate top-contact thin film transistors (TFTs) fabricated using our previously described methods [3,6,28]. After the evaporation of aluminium gate electrodes and associated tracks, the 5 cm x 5 cm substrates were attached to the cooled drum of a webcoater (Aerre Machines) which rotated at a linear speed of 25 m/min. Tripropyleneglycol diacrylate (TPGDA) was then flash evaporated under vacuum onto the substrates and cross-linked *in situ* in a plasma discharge to form a robust dielectric layer, typically ~300 nm thick. To minimise the surface polarity of the TPGDA [29], a polystyrene (M_W=350,000) film was spin-coated at 1000 rpm in a nitrogen glove box from a 3% wt:wt solution in toluene and annealed at 100°C in air for 10 mins yielding a capacitance C_i = 4.38 nF/cm^2 for the two-layer TPGDA-PS dielectric.

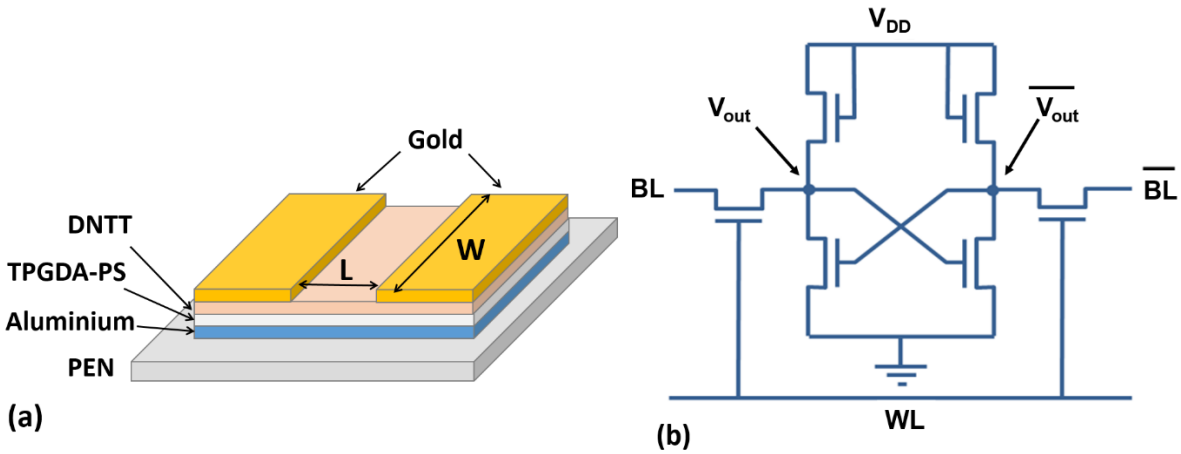

Figure 1 (a) Structure of the vacuum-evaporated bottom-gate top-contact transistors used for fabricating the SRAM arrays. (b) Circuit diagram of a single SRAM cell. Data is written into and read from the cell via BL and $\overline{BL}$. During this investigation, the state of the SRAM was also monitored directly at the inverters connected to BL or $\overline{BL}$.

A 70 nm thick film of the air stable, high-mobility p-type organic small-molecule DNTT was evaporated onto the polystyrene followed by evaporation of the gold source-drain electrodes and associated tracks. Prior to this final step, vias through the polystyrene were created either by mechanical scribing or in later devices by an oxygen plasma etch. All layers apart from polystyrene were patterned by evaporation through shadow masks (Laser Micromachining Ltd) in order to minimise parasitic effects. Evaporation of metal and semiconductor layers was undertaken in a Minispectros vacuum evaporator (Kurt Lesker Ltd) integrated into a nitrogen glovebox. Polystyrene and TPGDA monomer were obtained from Sigma Aldrich. DNTT was synthesised using the method of Yamamoto and Takimiya [29] and purified by recrystallisation.

Single 6-T SRAM cells (Fig. 1(b)) as well as 4x4 arrays of cells (Figure 2) were fabricated in this study. Each cell consisted of two cross-coupled inverters and two access TFTs to input and read stored data. The inverters were composed of a driver TFT and a diode-connected (enhancement) load TFT, the latter being possible owing to the negative threshold voltage of DNTT transistors produced using our method. In the single SRAM cell design, the load TFTs had a channel width, W, to channel length, L, ratio (W/L) of 625 µm/100µm. For the access and driver TFTs, W/L = 2500 µm/50 µm. In the SRAM arrays, the corresponding values were 500 µm/50 µm and 4000 µm/50 µm respectively.

With the voltage supply, V_{DD} set to -40 V, data was stored in the cells by applying -40 V pulses to the word line (WL) to turn on the access TFTs and simultaneously applying pulses to

the bit line (BL). The state of BL when WL turns off determines whether the stored data corresponds to logic 0 or logic 1. The stored data would normally be read by once again activating WL to turn on the access TFTs and reading the voltages on (or voltage difference between) BL and $\overline{\text{BL}}$. In this study, and in order to observe the state of the memory throughout the write/read process, the memory was also read directly at the inverters using probes to make contacts at the positions marked V_{OUT} and $\overline{V_{OUT}}$ in Figure 1(b). When the access transistors are turned off, BL and $\overline{\text{BL}}$ are disconnected from the cell and cannot be used to interrogate the memory.

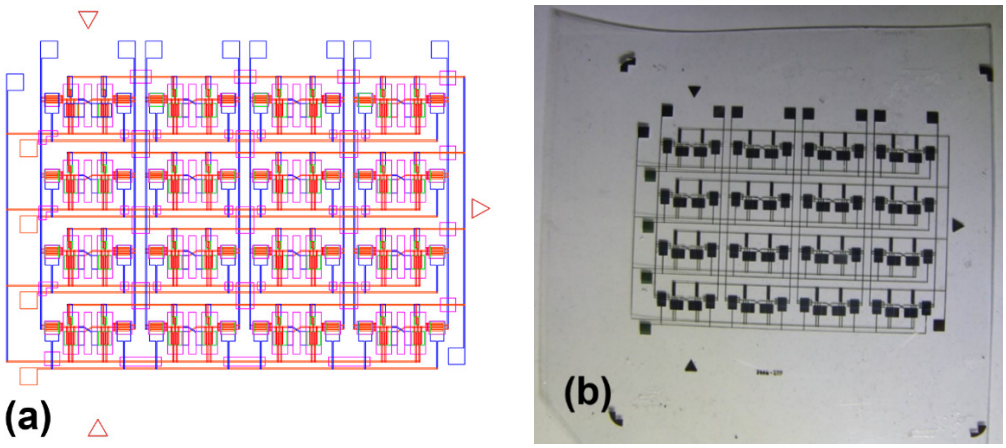

Figure 2 (a) CAD layout diagram and (b) photograph of a 4x4 SRAM circuit fabricated on a flexible PEN substrate.

Individual transistor and static inverter transfer characteristics were obtained using a Keithley Model 4200 Semiconductor Characterization System. SRAM cells were characterized by applying square wave pulses to the BL and WL contact pads from a TTi TGA1242 Waveform Generator connected to a high voltage amplifier (Falco Systems Model WMA01) and monitoring V_{OUT} and/or $\overline{V_{OUT}}$ via a buffer amplifier connected to an Agilent DSO-X-2014a oscilloscope. All the measurements were carried out in the dark, in a probe station under ambient conditions and without encapsulating the devices.

3. Results and Discussion

We have already reported extensively [3,30] on the characteristics of TFTs produced using our fabrication protocols. Figure 3 shows that the transfer characteristics of TFTs from the

SRAM cells, in this case an access transistor from the array, are also of the same consistently good quality and follow the usual relationships

$$I_D = \frac{W}{L}\mu C_i (V_G - V_T) V_D \quad (1)$$

in the linear regime (V_D = -1V), and

$$I_D = \frac{W}{2L}\mu C_i (V_G - V_T)^2 \quad (2)$$

in saturation (V_D = -40 V), where I_D is the source drain current, μ the mobility, C_i the gate capacitance per unit area and V_G, V_T and V_D the gate, threshold and drain voltages respectively. The characteristics are free of hysteresis - both the forward and reverse sweeps of V_G yield identical plots. The slopes of the linear sections of the transfer plots yield mobilities ~1.2 cm^2/Vs and ~1.3 cm^2/Vs in the linear and saturation regimes respectively – values that lie in the middle of the range reported previously [3,30]. Threshold voltages in the two regimes are -7.3V and -6.2 V respectively. The ON-OFF ratio at ~10^6 in saturation is similar to values we have previously reported [3,30]. This is despite the larger OFF-currents here which we attribute to the parasitic bulk current flowing parallel to the channel in the higher aspect ratio TFT (W/L = 80) reported in Fig.3.

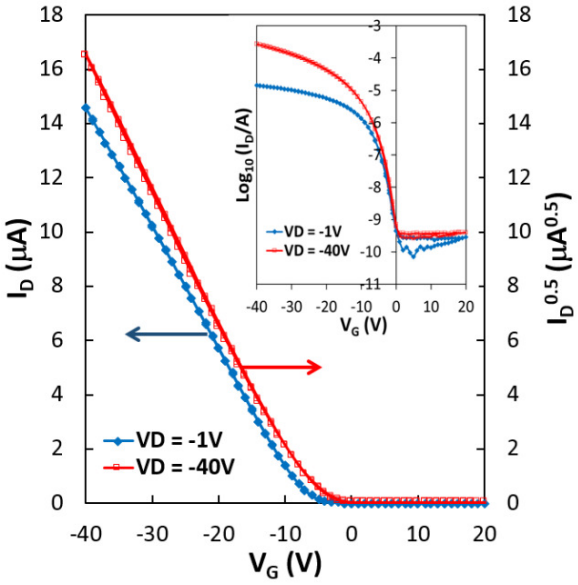

Figure 3 Transfer characteristics in both linear (V_D = -1 V) and saturation (V_D = -40 V) regimes of an access transistor from a cell in the SRAM array. The inset shows the same data plotted in semilog form.

Figure 4 is the voltage transfer characteristic of one of the inverters isolated from a SRAM cell. Again, identical plots were obtained for both the forward and reverse sweeps of V_{IN} between 0 V and -40V with the output switching from around -34 V to -2.6 V. The maximum gain, 2.07, is very similar to our previously reported values [6] with a noise margin ~2.5 V.

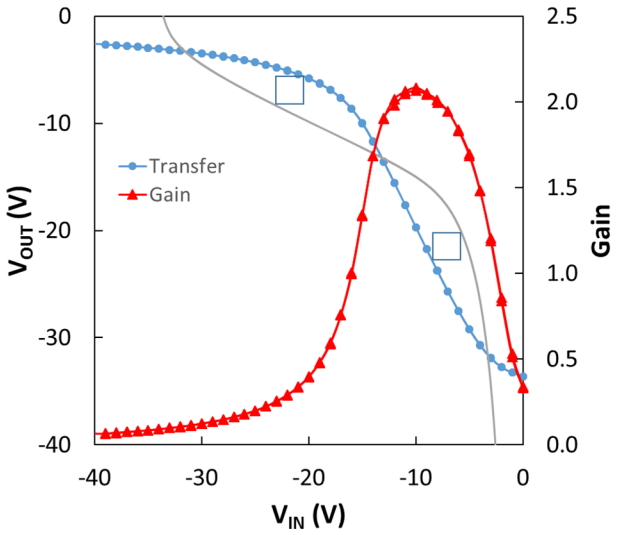

Figure 4 Voltage transfer and gain plots of an inverter isolated from a cell in the SRAM array. The construction used for estimating the noise margin is also shown. V_{DD} = -40 V.

In Figure 5 we show the dynamic response of one of the single SRAM cells when a -40 V square wave is applied to BL while WL is enabled and disabled. In this case, the output voltage, V_{OUT}, is measured at the inverter connected to BL in Figure 2(b). As can be seen, when WL is activated, V_{OUT} follows BL (regions 1 and 3 in Figure 5). The time constant for the falling edge to -25.6 V is estimated to be ~0.5 ms while that for the rising edge is ~0.3 ms. The maximum negative swing is less than expected from the static transfer characteristics. This is a consequence of loading effects by (a) the gate leakage current of the second inverter in the SRAM cell and (b) the bias current of the buffer amplifier. The latter has the greater effect as has been observed in previous measurements [6].

When WL is turned off, V_{OUT} remains close to -3 V in region 4, but reduces to -20 V in region 2 reflecting the stable states of the SRAM cell. As seen in Figure 6, so long as the 'write' voltage applied to BL exceeds the trip voltage of the inverters, V_{OUT} always stabilises at -20 V.

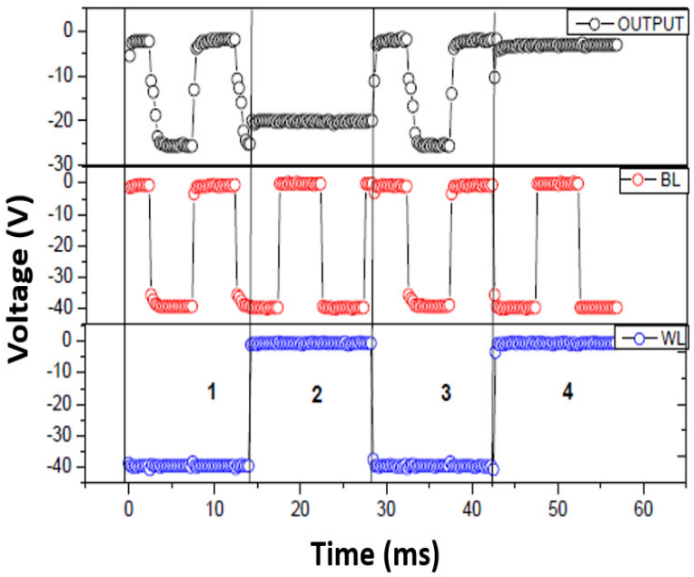

Figure 5 Response of a single SRAM cell to changes in BL voltages when WL is enabled (regions 1 and 3) and disabled (regions 2 and 4). V_{OUT} is the voltage measured at the output of the inverter connected to BL. V_{DD} = -40 V.

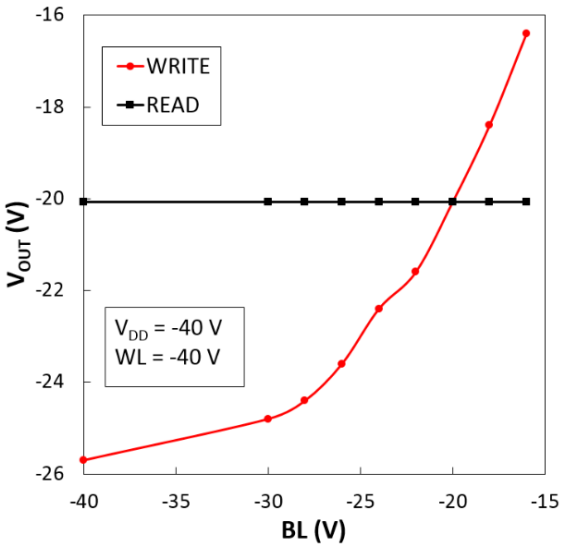

Figure 6 Measured V_{OUT} for different values of BL voltages during write (red circles, WL enabled) and read (black squares, WL disabled) actions. V_{DD} = -40 V.

Following the initial success with single SRAM cells, we proceeded to fabricate a 4 x 4 SRAM array. In Figure 7(a) we show the switching and memory operations of a cell from within such an array. This time, while square-wave pulses were applied to WL and BL, $\overline{V_{OUT}}$ was

measured at the output of the inverter connected to $\overline{BL}$. When WL is disabled, depending on the whether BL is at 0 V or -40 V, $\overline{V_{OUT}}$ remains at -24 V or -5 V.

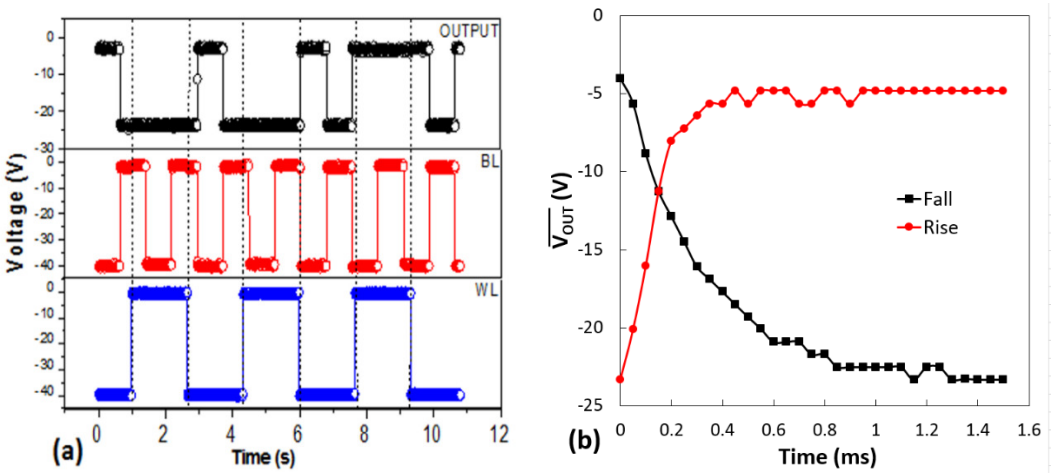

Figure 7 (a) Response of a SRAM cell from the 4 x 4 array to changes in BL when WL is enabled and disabled. The output voltage, $\overline{V_{OUT}}$ is measured at the inverter connected to $\overline{BL}$ in Fig.2. (b) The rising and falling edges of the $\overline{V_{OUT}}$ transients when switching voltages are applied to BL. V_{DD} = -40 V.

Figure 7(b) shows an expanded view of the response of $\overline{V_{OUT}}$ to changes in BL when WL is enabled. The time constants for the switching transients are ~0.22 ms for the rising edge and ~0.36 ms for the falling edge. These time constants are almost 40% shorter than for the single SRAM cells because the transistors used in the array had higher channel conductances arising from their higher aspect ratios, coupled with lower gate overlap capacitances. These time-constants are much shorter than reported by Guerin et al [16] and Takamiya et al [17], and comparable with those reported by Fukuda et al [18]. They are, however, longer than reported by Kumar et al [19] for cells in which the aspect ratios of access, driver and load TFTs were optimised.

Bias stress effects can often cause organic TFT circuits to shift outside their effective operating range. Clearly, the stability of the data stored in the SRAM will be dependent on the electrical stability of its constituent TFTs. The hysteresis-free characteristics of both the TFTs (Fig. 3) and inverters (Fig. 4) are indicative of good short-term stability. To test the long-term stability, a cell was programmed by applying -40 V to BL while WL was enabled briefly.

Subsequently, and with V_{DD} = -40 V applied continuously, the state of the memory was read periodically by enabling WL and measuring the voltages appearing on BL and $\overline{\text{BL}}$. The results are shown in Figure 8 and cover a period in excess of 27 hours. As can be seen, $\overline{\text{BL}}$ remains constant at about -3 V throughout this period. BL also remains well-defined changing only slightly from -21.5 V to -23.1 V, thereby increasing slightly the discrimination between 'high' and 'low'.

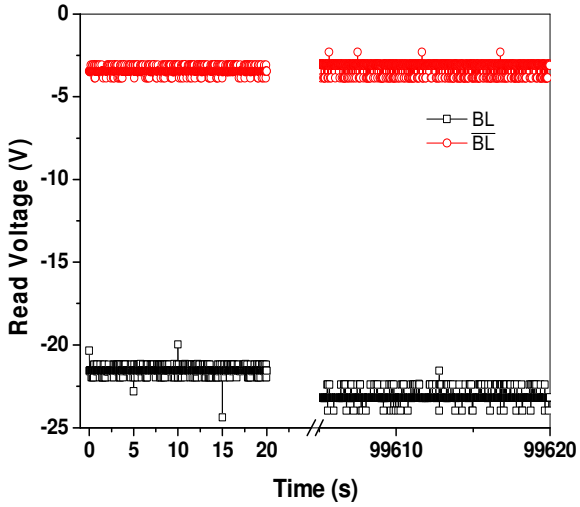

Figure 8 Long-term data retention in an SRAM cell with V_{DD} = -40 V applied continuously. The discrimination between BL and $\overline{\text{BL}}$ improves slightly with time.

In addition to excellent stability against bias stress, our SRAMs showed good environmental stability. Cells tested two months after fabrication and stored in a closed plastic box in a normal laboratory environment showed very little difference in performance to that reported above.

4. Conclusions

We have fabricated single SRAM cells as well as 4 x 4 arrays using a roll-to-roll compatible vacuum-evaporation approach for all but one of the process steps. The devices were based on a two-layer TPGDA/PS dielectric and p-type DNTT as the active semiconductor. Turn-on voltages close to zero coupled with negative threshold voltage facilitated a cell design comprising cross-coupled, diode-connected (enhancement) load inverters. The sub-ms response time of the inverters enabled rapid writing of data into the memory. Furthermore, once programmed the stored voltages (data) remain virtually unchanged after 27 hours. Switching

speed of cells in the 4x4 SRAM array was ~40% faster than in the single cell design, consistent with a higher TFT aspect ratios (*W/L*) and reduced parasitic gate overlap capacitance in the array. The cells were found to be stable against bias stress and showed good environmental stability with performance remaining virtually unchanged after two months of storage in the laboratory ambient.

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