Silicon nanowires, cryogenic control and radio-frequency read-out for quantum devices

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Abstract:
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For the last two decades research on grown nanowires has been motivated by their potential application as efficient transistors, sensors and building blocks of quantum information processing architectures. While these applications can benefit from quantum effects, such as tunneling and quantum interference, the integration of bottom-up grown nanowires into larger circuits is technologically challenging. Top-down fabricated nanowires, that recently became available due to progress in semiconductor fabrication, provide a means of overcoming this barrier. In combination with silicon spin qubits, they could enable a fully integrated quantum processor with silicon nanowire control electronics that comply with the cooling requirements in a cryogenic environment.

I will present silicon nanowire transistors that were fabricated using CMOS-compatible processing and operate at room temperature as well as in the cryogenic regime. With a diameter of only 8 nm, the nanowire devices exhibit excellent electrostatic control of the channel and show evidence for one dimensional transport. Transport in these nanowires is dominated by scattering off dopants and off the nanowire walls rather than off the rough nanowire surface or other surface defects that often dominate in nanowire devices. Optimized nanowires with lower doping and shorter channels could therefore enable ballistic cryogenic CMOS with ultra low heating in a cryogenic quantum processor.

In addition to DC experiments, I will use a measurement technique where the impedance of a quantum device in a resonant circuit can be inferred from the reflection of radio-frequency signals. The sensitivity to a changing device impedance is improved via in-situ impedance matching of the resonant circuit to the measurement electronics. As a result charging events in a silicon nanowire device can be detected with a good charge sensitivity. In case the quantum device requires small input powers, for example if measurement back-action is significant, further improvement is achieved by employing a low noise SQUID amplifier. The measured sensitivity to changes in the quantum capacitance enables the read-out of a singlet-triplet qubit much faster than the typical decay time of the quantum state. Since the technique does not require additional sensing devices and the read-out circuit can be connected directly to a gate electrode of the qubit, this type of read-out is promising for scalable quantum information processing architectures.

List of associated publications

- F.J. Schupp, M.M. Mirza, J.A. Mol, D.A. MacLaren, G.A.D. Briggs, D.J. Paul, "Quantum Interference in Silicon 1D Quasi-Ballistic Junctionless Nanowire Field Effect Transistors", under review, arXiv:1802.07013, 2018

- F.J. Schupp, N. Ares, A. Mavalankar, G. Rogers, J. Griffiths, G.A.C. Jones, I. Farrer, D.A. Ritchie, C.G. Smith, G.A.D. Briggs, E.A. Laird, "Sensitive Capacitive Read-out at Radio-frequency with a SQUID Amplifier", manuscript in preparation, 2018

- F.J. Schupp, "Single-electron devices in silicon", Material Science and Technology 33 (8), 2017

- M.M. Mirza, F.J. Schupp, J.A. Mol, D.A. MacLaren, G.A.D. Briggs, D.J. Paul , "One dimensional transport in silicon nanowire junction-less field effect transistors", Scientific Reports 7, 2017

- N. Ares, F.J. Schupp, A. Mavalankar, G. Rogers, J. Griffiths, G.A.C. Jones, I. Farrer, D.A. Ritchie, C.G. Smith, A. Cottet, G.A.D. Briggs, E.A. Laird, "Sensitive Radio-Frequency Measurements of a Quantum Dot by Tuning to Perfect Impedance Matching", Physical Review Applied 5 (3), 2016

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1 Introduction

Scientific and technological progress in microelectronic devices is among the most significant developments in technology of the last century. The rapid progress predicted by Moore's law in 1965 has lead to technologies, that have revolutionized modern life and set the stage for the internet era [1, 2]. Modern electronics became possible due to reduced power consumption, smaller devices, increased operation speed and reduced costs per device through mass fabrication – all enabled by improvements of semiconductor fabrication techniques and miniaturization. As semiconductor devices are reaching scales where the macroscopic approximations of discrete microscopical phenomena are failing, this rapid progress might slow down [3]. For example, in modern devices with a length scale of few 10 s of nanometres, charge densities can vary significantly due to the discrete number of dopants in the channel and as a result of dopant deactivation through screening effects that strongly depend on device geometry [4].

On a more fundamental level, if device dimensions reach below ~ 10 nm, quantum confinement in one- or two-dimensions can dominate and systems become two- or one-dimensional. The effect of quantum confinement derives from the wave-like nature of electrons that can interfere and form standing waves causing charge carrier localization and restriction of movement in one or more dimensions. Quantum confinement from interfering electron waves can also play a role in small zero dimensional systems but the quantization of charge is already sufficient to fundamentally change the device physics compared to a classical system where continuous charge densities are considered. A zero dimensional system consists of a charge island that is weakly coupled through a tunnel barrier to one or more charge reservoirs such that the quantization of charges on the island is significant for the electrostatic energy of the system.

While electrical transport in these systems is impossible according to classical physics, transport can still be facilitated by quantum tunneling on and off the island.

The prospect of device dimensions in the few nanometre regime therefore poses new questions about future semiconductor devices: Given the impurities and imperfections in a silicon device, how does a one-dimensional transistor perform compared to bulk devices? Is there an advantage to zero dimensional transistors? What type of measurement is needed to exploit the benefits of such a quantum electronic system especially if current measurement is not an option? What are the applications?

The answers to these big questions can only be found with sufficient knowledge about the relevant transport physics as well as the environmental requirements of a specific application. In this thesis, I will therefore study transport through quantum confined systems in silicon to identify the relevant transport physics and add to the fundamental understanding of device physics that will be critical for the development of future devices. I will also present my work on the improvement of a device read-out technique based on reflection of radio-frequency waves. This technique does not require current transport through the device and can be employed with little measurement back-action. Additionally, the $1/f$-noise component is typically negligible such that signal-to-noise ratios are higher than in DC measurements and e.g. charge sensors can operate faster. Apart from zero dimensional transistors, the technique can be used for the read-out of fundamental quantum properties and is therefore interesting for quantum information processing [5, 6].

1.1 Silicon nanowires

I will begin by exploring quantum confinement and electric transport in top-down fabricated silicon nanowires. These devices have been suggested as the successor of the state-of-the-art "FinFET" transistor technology due to improved electrostatic control of the transistor channel with a gate all around [7]. Improved electrostatic control leads to reduced leakage currents due to short channel effects compared to e.g. FinFETs, such that channels can be shorter and transistors are potentially more energy efficient with less resistive heating per channel cross section area [7].

While this sounds promising, the performance and resistivity of a 1D quantum confined system is also subject to 1D screening, 1D scattering, 1D electron-electron interactions etc. Moreover, there can be one dimensional effects such as transport through subbands [8], 1D quantum interference [9, 10] as well as exotic phenomena including Luttinger-liquids [11] or Majorana Fermions [12]. Especially the formation of subbands and strong electron-electron interaction represent an aspect of device modeling that was not previously implemented in the industrial device optimization process [13, 14, 15]. For the design of future devices it will be crucial to understand these 1D phenomena when deciding if a 1D transistor is beneficial for a certain application.

Possible benefits can only be exploited if the fabrication of nanowires can be optimized. This is particularly challenging since nanowires often show an increased sensitivity to imperfections compared to industrial FinFET devices – for example surface effects can become even more relevant in nanowire devices with a higher surface to volume ratio than FinFETs [16]. The price for improved electrostatic control is therefore less tolerance for imperfections such as charged impurities in the oxide or on material

interfaces. On the other hand, if unintentional imperfections can be largely avoided, the high sensitivity to surface effects also represents an opportunity for e.g. building a nanowire charge sensor or for the detection of dielectric materials on the surface of a nanowire [17, 18]. For all commercially viable applications, it is crucial to understand and control the factors that can impact the device performance and optimize fabrication methods to ensure reproducibility and scalability.

In case the device physics can be understood and fabrication is optimized sufficiently, silicon nanowire transistors could replace FinFET technology in many existing applications. In addition, future applications could include, so called, "cryogenic CMOS", where the transistors need to operate at low temperatures in e.g. the control layer of a quantum processor [19]. Depending on the number of used transistors this is likely to require ultra low energy dissipation, such that ballistic transport without scattering in the channel would be beneficial [20]. Characterization of nanowire devices is therefore needed in all temperature regimes from 10 mK to 300 K and higher.

In this thesis I will explore transport in silicon nanowires that were etched from a silicon wafer and are therefore more comparable to state-of-the-art CMOS technology than e.g. CVD grown nanowires (Chapters 3.2 and 3.3). In these technologically relevant devices, I will study and characterize one-dimensional transport at temperatures from 12 mK up to room temperature.

1.2 Transport through charge islands and radio-frequency read-out

While quantum confinement in one-dimensional devices does not necessarily change basic transistor behaviour, such as a monotonic increase in current due to a gate voltage, transport in zero-dimensional devices requires tunneling of single charges and the device behaviour is fundamentally different [21]. A fundamental change in electric properties can also be observed in a device without significant zero dimensional quantum confinement when charge carriers are trapped on an island and the quantization of charge translates into discrete levels in the energy spectrum through purely electrostatic effects. The probably most widely known example for such a system is a single electron transistor (SET), where current is made up from one electron at a time tunneling onto/off a charge island. If there is an additional contribution from 0D quantum confinement in very small systems (typically < 100 nm) such a system is often called a "Quantum dot". Since the first SET was demonstrated using a charged metal island in 1987 by Fulton *et al*. [22], SETs have been realized in a large number of systems such as GaAs [23], silicon [24], graphene [25] or carbon nanotubes [26] with charge islands on the length scale of 10s of nanometres to micrometres. More recently it was also shown that similar transistors can be fabricated with charged islands that only consist of a single atom [27].

Single electron transport through an island requires that the energy difference between the $N/N+1$ charge degeneracy point and the $N/N-1$ charge degeneracy point is larger than thermal energy (for details see Sec. 3.1.5). This difference in energy, called "addition energy", has a contribution from quantum confinement in 3D and a contribution from the electrostatics of the system. The electrostatic contribution can be increased by reducing the overall capacitance of the island such that SETs can be operated easily

at cryogenic temperatures. There is, however, a limit to reducing the capacitive coupling since it is also required for controlling the SET with a gate electrode.

Another way to increase the addition energy is by tightening the quantum confinement, which increases the energy spacing between the quantum levels associated to N and $N+1$ occupation analogous to the eigenenergies of a particle in a box. Since this spacing is increasing with decreasing island size, ultra small SETs have been built to achieve room temperature operation [28, 29, 30]. One promising approach employs single dopants in a semiconductor as small islands, but to date the addition energies were not sufficient to effectively prevent thermal activation of transport at room temperature [31, 32, 33]. For example the addition energy in a single electron transistor made from a phosphorous dopant in silicon is 47 ± 3 meV [27] and therefore on the same order of magnitude as thermal energy (25 meV at 290 K). Although, so called, deep donors have a significantly higher ionization energy (e.g. ionization energy of selenium in silicon: 312 meV [34]), there have not been reports on single electron transistors made from these donors.

Shin *et al*. [28, 35] have fabricated a room temperature SET starting from a FinFET geometry that was modified to feature a very small island and tunnel barriers induced by strain in the material. The devices show Coulomb blockade up to 300 K and excited states at lower temperatures can be explained in an atomistic model [28, 35]. Especially the agreement with the atomistic model is strong evidence for a single charge island with strong confinement. Room temperature operation of an SET has further been reported by e.g. Lavieville *et al*. [29] using a 10 nm gate in a silicon nanowire device, that was fabricated from a FinFET architecture and oxidized in order to reduce the diametre to 3.5 nm.

Apart from logical transistor circuits, SETs can be used as single electron pumps to define a current that

is created by periodic modulation of tunnel barriers and island potential [36, 37]. This has applications in metrology since the Ampere could be redefined in terms of electron charge and frequency if the charge pumps can be accurate enough and produce sufficient current [38]. Another application for SETs is fast charge sensing with high accuracy that is particularly interesting for the read-out in quantum information processing schemes [39, 6]. In Ch. 4.4 of this thesis I present a zero dimensional system in a silicon nanowire and demonstrate charge sensing with sensitivities close to the best reported values from a quantum dot device with multiple gates on a silicon two dimensional electron gas (2DEG) [40] as well as a FinFET device [41].

The type of measurement used to detect the charge is often referred to as "RF-reflectometry". In this measurement one studies the reflected signal from a tank circuit that includes the sample. The reflection is a function of the complex impedance of the tank circuit such that a change in sample impedance affects the reflected signal. If the sample is tuned to a point where e.g. the conductance changes drastically in the presence of outside charges, the circuit becomes a sensitive charge sensor that is less affected by $1/f$ noise than a DC sensor. This technique has been demonstrated in a number of device types including quantum dots [40], metal SETs [42] and nanowires [43]. Since the measurements are performed at radio-frequencies, a direct current from source to drain is not required and the technique can be used to measure any kind of system where electrons change their configuration with respect to charge distribution. Additionally the technique is sensitive to changes in inductance, since that also affects the impedance of the tank circuit.

If sufficient sensitivity can be achieved, RF-reflectometry is promising for the read-out of semiconductor qubits that can be built from two quantum mechanical states of one or more confined charges/spins in

zero-dimensions [44, 5, 45]. In previous work, the spin state of an electron was read out using a spin selective tunneling event between two quantum dots that was detected with reflectometry on a nearby charge sensor [46, 47]. In the context of large quantum information processing architectures, however, this additional charge sensor is detrimental for scaling. Alternatively, spin qubits can be read out with an RF circuit connected directly to the qubit through detection of the quantum capacitance that arises when spatially separated electrons hybridize and the quantum state becomes compressible [48, 47, 49]. To date this technique has not been demonstrated with sufficient sensitivity to enable read-out before the qubit state decays.

In Ch. 4.2 and 4.3 of this thesis I will demonstrate how sensitivities in a reflectometry circuit can be optimized to achieve fast and precise read-out of e.g. semiconductor qubits. First I will show improved sensitivity from tuning the tank circuit impedance into perfect impedance matching with the radio-frequency source. For devices that require low input powers, I will then report on further improvements that were achieved by implementing a low noise SQUID amplifier. The optimized circuit is sensitive enough to detect the quantum capacitance of a state in a singlet-triplet qubit before the qubit eigenstate decays. I have therefore demonstrated a system that could be used to directly read out a spin qubit via quantum capacitance without the need to average over multiple repetitions of the quantum computation – read-out in a "single-shot".

2 Measurement system and samples

This section describes the samples, cooling systems and measurement circuitry used for the measurements presented in this thesis. While I did parts of the process development for the next generation of silicon nanowire devices, e.g. developing a process to etch short metal gates $\geq$20 nm (not part of this thesis), I was not involved in the fabrication of any devices presented here. The silicon samples were fabricated at the James Watt Nanofabrication Centre (JWNC) at the University of Glasgow by Muhammad Mirza. The GaAs quantum dot, that was used as a reference sample to compare the performance of the RF-circuit with different modifications, was fabricated by Aquila Mavalankar in at the University of Cambridge. The measurements presented in this thesis were carried out in a temperature range from 300 K to 12 mK, which required multiple cooling systems: a cryogenic probe-station (at the University of Glasgow), a liquid helium bath and a dilution refrigerator (both at the University of Oxford). This section also introduces the measurement circuitry for direct current and radio-frequency measurements, that is particularly elaborate in the dilution refrigerator where thermal coupling, attenuation and filtering is crucial to achieve electron temperatures of few 100s of mK. My contributions to this setup are the modifications of the radio-frequency wiring in the dilution refrigerator to accommodate an additional low temperature SQUID amplifier.

2.1 Samples

The experiments presented in this thesis involve two types of samples: a GaAs quantum dot and several silicon nanowires with different doping densities and channel diameters. The GaAs quantum dot is not

investigated in terms of transport physics, but used as a reference sample to compare the performance of the RF circuit with different modifications. Silicon nanowires could have been used for this purpose, but might have caused additional uncertainties in the evaluation of the RF-circuit performance from poor reproducibility between cool-downs. Since the goal was to study the RF circuit rather than the sample, the physics of the GaAs quantum dot is not the main focus of the experiment and I will therefore not go into detail about the fabrication at this point. Instead I want to refer the interested reader to the associated publication [50].

The silicon nanowires, that were studied in more detail with respect to their physical properties, were fabricated "top-down" from silicon-on-insulator wafers (SOI). In this context top-down as opposed to "bottom-up" means that the nanowires were not grown with e.g. chemical vapor deposition [51], but etched out of an existing piece of material in a process that is more comparable to industrial fabrication of semiconductor devices. The silicon nanowire samples were fabricated from a homogeneously Si:P doped SOI wafer such that the doping density does not change along the nanowire channel and the resulting transistor type samples are "junctionless". A transmission electron picture of the cross section of an 8 nm diameter nanowire is shown in Fig. 1a. The silicon channel is surrounded by an oxide layer with a slightly varying thickness of 16 ± 4 nm depending on the radial angle. The silicon channel and oxide are wrapped in an aluminum gate that stretches along the entire channel and can be used to control the channel with an electric field. Figure 1b is an image of a device that was taken with a scanning electron microscope and shows the top view when looking at the wafer. The nanowire has a length of 150 nm and is contacted by larger silicon leads that increase in width several times until they reach the bondpads (not shown). The figure also shows the aluminum gate that wraps around the nanowire along the entirety of

its length and then overlaps with the leads – the gate has no electrical connection to the channel or leads due to an oxide that separates these layers of the device.

2.1.1 Nanowire fabrication

The silicon nanowire samples were fabricated from silicon-on-insulator (SOI) wafers that are comprised of a silicon layer with a thickness of 753 µm covered with 150 nm of SiO_2 and 55 nm of doped silicon. These wafers were purchased from SOITEC where they were exposed to phosphorous ion implantation doses of $4 \times 10^{14}\,\mathrm{cm}^{-2}$ and $5 \times 10^{15}\,\mathrm{cm}^{-2}$.

In a first fabrication step, the dopants were activated in a rapid temperature anneal at 950°C for 90s. Next

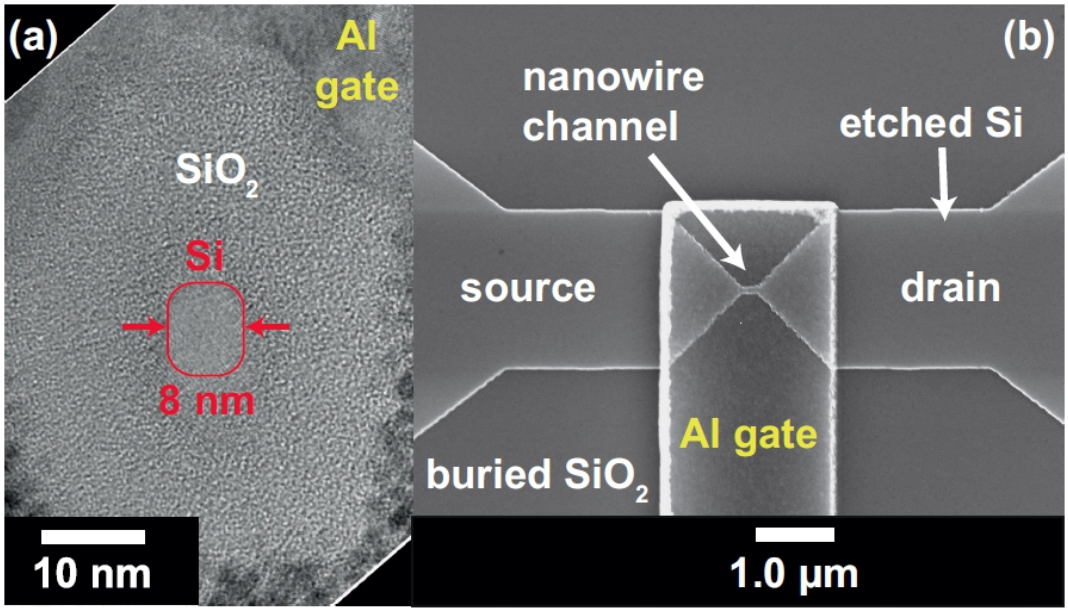

Figure 1: a) Cross section of a silicon nanowire device with nanowire diameter 8 nm in a transmission electron microscope picture b) Top-view of a 150 nm nanowire with large Al gate and leads in a scanning electron microscope image. [52]

the wafers were etched in reactive ion etching (RIE) to reduce the top silicon layer thickness from 55 nm to 15 nm and ensure a round cross-section in the final nanowire devices as opposed to a FinFET-type cross section with 55 nm height. Afterwards the wafers were cleaned in successive ultrasonically excited baths with acetone, propanol and deionized water before they were blown dry with nitrogen and baked at 140° C. The cleaning also included piranha, hydrofluoric and hydrochloric acid– a procedure that is commonly used in the semiconductor industry [53].

The nanowire structure was then defined with electron-beam lithography (EBL). In this process a resist is spun on the wafer and locally electrochemically altered when it is exposed to an electron beam. When using a "negative" resist, the electron beam draws a cross-linked pattern into the resist that does not dissolve in a developer liquid. In the subsequent development step, the unexposed resist is washed away such that a resist mask is formed. EBL was carried out using a resist, called Hydrogen Silsesquioxane (HSQ), that was diluted with methyl isobutyl ketone (MIBK) at a ratio of 1:2 and spun onto the wafer at 2000 rpm resulting in a resist thickness of 150 nm. After being baked at 90° C for 2 minutes to remove solvent in the resist, the resist mask was written in a Vistec VB6 UHR electron-beam tool operating with an acceleration voltage of 100 kV and a spot size of $\sim 4\,\mathrm{nm}$ at 1 nA electron beam current. The electron dose of $\sim 2500\,\mu\mathrm{C/cm^2}$ was found to produce optimal results in the subsequent development step in tetramethyl ammonium hydroxide (TMAH) that was mixed with deionized water 1:16. After development for 1 minute at 23° C the process produced a resist mask with feature sizes down to 10 nm.

The resist pattern was then used as an etch mask to transfer the device layout to the silicon in a highly optimized RIE step using a mixture of SF_6 and C_4F_8 ($25 : 90\,\mathrm{SCCM}$) in an STS-RIE system with 600 W coil power and 6 W platen power (for details see Ref. [54, 55]). This process was optimized for small

processing damage from ion bombardment as well as straight etch profiles as opposed to rounded profiles where ultra small nanowire features would have been destroyed.

After RIE the sample was cleaned again with piranha and hydrofluoric acid to ensure high cleanliness before oxidation and avoid trapped charges [54]. Apart from removing impurities and leftover resist, the etching with hydrofluoric acid also underetched the nanowires and suspended them between the leads. The nanowires were then exposed to an oxygen flow of 525 l/h at 950°C for 1:40 min to oxidize the silicon starting from the exposed silicon surface of the wire. This process was optimized to leave only a small diameter silicon core of 8 ± 0.5 nm (or larger if thicker structures were defined in EBL) that is surrounded by a clean oxide shell with a thickness of 16 ± 4 nm.

At this stage of the fabrication process a device consisted of a suspended silicon wire that is surrounded by an oxide layer and connected to larger silicon structures on both ends. To build a transistor geometry and enable contacting with bond wires, the device requires metal bondpads for source/drain as well as a gate electrode. The source/drain bondpads were fabricated using a resist window, that was defined on top of the larger silicon structures on both ends of the nanowire channel using optical lithography. Hydrofluoric acid was then used to remove the oxide layer that had developed in the oxidation process before the Al bondpads for source/drain were deposited. The gate electrode together with the associated bondpad was deposited on top of the oxide layer around the nanowire using EBL, aluminum evaporation and lift-off. The metallization was carried out such that the Al vapor surrounded the suspended nanowire and created a wrap-around gate. It is crucial for the device performance, to achieve a low interface trap density between the gate and the oxide layer. Before the metal electrode for the gate was deposited, the samples were therefore thoroughly cleaned and annealed in "forming gas" (mixture of N_2 and H_2) at

380 °C for 15 min to passivate dangling bonds on the oxide surface around the wire.

2.1.2 Characterization of similar silicon channels

Similar devices to the nanowires investigated in this thesis, with a FinFET-type cross section and no gate electrodes, were characterized previously by Mirza *et al*. [56]. Figure 2a shows the 300 K resistivity ρ of these devices as a function of FinFET channel width d at different phosphorous doping concentrations. The resistivity decreases with increasing doping concentration and increases with decreasing FinFET width. In the remainder of this thesis I will refer to the activated doping concentration of a wafer, measured in the large Hall-bars, as the "nominal doping concentration".

Since the resistivity is a function of the activated charge carrier concentration n_{3D} and the mobility μ_H, these quantities are shown in Fig. 2b as a function of temperature T. The Figure shows data from FinFET channels doped $8 \times 10^{19}\,\mathrm{cm}^{-3}$ with width 4 nm (green), 7 nm (red), 12 nm (blue) and 18 nm (black) that were studied in a Hall-bar type of measurement. The increase in resistivity with decreasing FinFET channel width from Fig. 2a can be related to reduced mobility from e.g. more dominant surface effects and reduced charge carrier density from dopant deactivation [16]. The authors interpret the changing curvature of the mobility for different FinFET width as a transition in the dimensionality of transport that crosses over from bulk transport to lower dimensional transport as the FinFET width is decreased. Similar to a result that will be presented in this thesis, they base this conclusion on screening effects in a highly doped system (for details see Ref. [56] and Ch. 3.1.1).

Figure 2c shows the theoretical behaviour of the mobility in the 7 nm FinFET channel with nominal

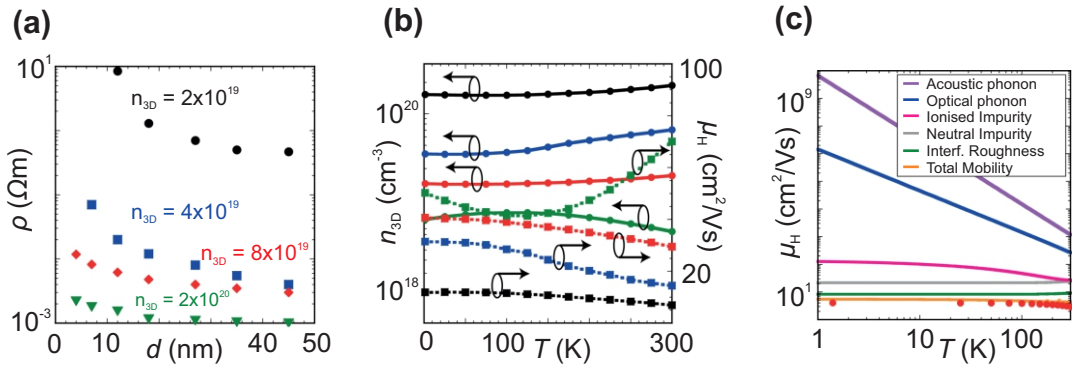

Figure 2: a) Resistivity ρ as a function of device width d in the measurements from Mirza *et. al*[56] at different nominal doping densities as indicated in cm^{-3}. b) Charge carrier density n_{3D} and Hall-mobility μ_H as a function of temperature T in devices doped $8 \times 10^{19}\,\mathrm{cm}^{-3}$ with width 4 nm (green), 7 nm (red), 12 nm (blue) and 18 nm (black). c) Predicted behaviour of the mobility as a function of temperature with different scattering mechanisms and fitted mobility (orange) to the data points (red).

doping density $8 \times 10^{19}\,\mathrm{cm}^{-3}$ as a function of temperature for different dominant scattering processes. The orange line is a fit for the data points (red) to a formula that implements all scattering mechanisms and shows qualitative agreement with the predicted behaviour for neutral impurity scattering dominated transport (for details see Ref. [56]). Mirza *et al*. therefore concluded that neutral impurity scattering from unactivated dopants is dominant in the system.

Based on these measurements, the nominal doping concentrations for the devices in this thesis were chosen to be $4 \times 10^{19}\,\mathrm{cm}^{-3}$ and $2 \times 10^{20}\,\mathrm{cm}^{-3}$, since the tested FinFETs with these doping concentrations are reasonably conductive and likely to work at low temperatures. While the activated doping density is generally lower than the density of implanted ions because not all dopants are being activated, this should yield sufficient charge carrier density even at low temperatures where the activated doping density is further reduced. Additionally, the fraction of activated dopants depends on device geometry due to surface segregation and dielectric effects [16]. While the addition of a gate in the presented devices in this thesis

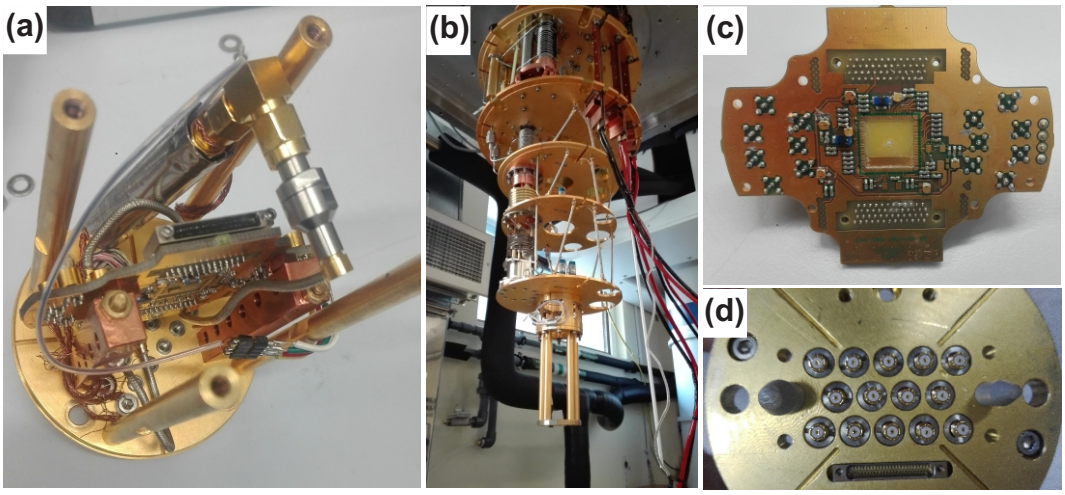

Figure 3: a) Open puck with sample board mounted and SQUID amplifier connected to the RF lines. b) Triton 200 without shields and magnet. c) Sample board. d) Puck interface that connects to the wiring in the dilution refrigerator. The RF-connectors (middle) and DC-connector (bar on the bottom) attach to their counterparts in the dilution refrigerator when loading the puck. The white guiding rods (right and left side) are used to align the puck with the dilution refrigerator connectors in the loading process.

should improve the fraction of activated dopants significantly according to Ref. [16], the higher doping densities were chosen to ensure operation at low temperatures.

2.2 Cryogenic systems

The measurements at room temperature presented in Sec. 3.2 were performed at the University of Glasgow by Muhammad Mirza with a semiconductor parameter analyzer (Agilent B1500) and a Cascade microtech probestation, while lower temperature measurements were carried out in a Lakeshore CRX-6.5 K cryogenic probestation. For more details about these measurements I want to refer the reader to the associated publication from Mirza *et al*. [52].

I have carried out the measurements at 4.2 K in Sec. 3.3 in a custom-made "dipstick" that consists of

a cylindrical vacuum shield around a metal rod that supports the DC wiring. On top of the dipstick the wiring is connected via a 52 pin connector by Fisher Connectors (type "core series") and the sample is bonded to a sample carrier on the bottom of the dipstick. To measure at 4.2 K, the vacuum shield is pumped and the dipstick is lowered into a liquid helium dewar.

I have carried out the other measurements from Sec. 3.3 and all following chapters in DC and RF in a Triton 200 dilution refrigerator from Oxford Instruments that uses multiple cooling stages and reaches around 12 mK base temperature (see Fig. 3b). The cooling stages are separated by the circular plates shown in Fig. 3b, that include clamps for the DC wires as well as copper posts around which the wires are wrapped to ensure thermal connection to the system and minimize heat flux to the base temperature stage. Additionally the DC lines are filtered at base temperature with a series of commercially available filters and thermalized using a saphire heat-sink (for details see Appendix Fig. 45, Fig. 46). While the phonon bath reaches around 12 mK in this system the electron temperature only gets to around 100 mK because the electron-phonon scattering, that couples phonon bath and electrons, is suppressed [57].

The input line to the RF circuit is attenuated by 25 dB at 4 K and by 6 dB at 1 K to avoid heating the lower temperature stages and attenuate thermal noise. Additionally the cold part of the input line sitting below 4 K is made from superconducting materials (CuN) to minimize heat flux and cable losses. Just like in the DC wiring, the phonon system at base temperature is largely decoupled from the electron system and the electron temperature does not reach 12 mK. The coupling is maximized in a custom made copper powder filter at the base temperature stage to ensure minimal electron temperature in the RF lines.

The RF output line includes low noise amplifiers at low temperatures that are thermally isolated from higher temperature stages with superconducting lines (NbTi) and amplify the signal as well as the noise

at low temperatures. Hence the signal-to-noise ratio is limited by the lowest noise level at the base temperature stage as opposed to the increased noise at higher temperatures.

To measure a sample, it is glued to the centre of a sample board (shown in Fig. 3c) and wire bonded. The sample board is then connected to the DC and RF lines in the dilution refrigerator via a "puck" that can be screwed into the lowest temperature stage of the dilution refrigerator to ensure good thermal coupling and electrical connection. The puck is a metallic cylinder that is shown in Fig. 3a with RF and DC connectors to the dilution refrigerator wiring shown in Fig. 3d. The puck can be transferred into the dilution refrigerator using a load-lock while the system is at 4 K, such that a sample change and full cool-down to 12 mK can be done in around 14 hours with no need to warm up or open the system.

2.3 Measurement circuit

I will now describe the measurement setup, wiring and electronics that were used in the presented experiments in this thesis. The measurements in Sec. 3.2 were carried out at the University of Glasgow by Muhammad Mirza with an Agilent B1500 parameter analyzer and two different probe stations depending on the measurement temperature (see Sec. 2.2). I have carried out the other DC experiments in Oxford with battery powered low noise measurement electronics from QT in Delft. These electronics include a high voltage source, 16 digital to analog converters that can be used as low noise voltage sources in a range $\pm 2\,\mathrm{V}$ as well as a series of current amplifiers. Since the digital data acquisition requires a voltage rather than a current, the amplifiers convert a DC current to a DC voltage with gains from 10^6-$10^9\,\mathrm{V/A}$.

In the RF measurements a Keysight 8267D vector signal source was used for the input "carrier" signal into port 1 shown in Fig. 4. The output signal of the circuit at port 2 was either measured with an Agilent EXA9010A signal analyzer (not shown in Fig. 4) or a demodulation circuit that converts the reflected signals into a DC voltage. To determine the resonance in reflected power vs carrier frequency of the circuit between port 1 and port 2, I have used a Rigol 815 (or Rigol 875) spectrum analyzer. For the measurements that included information about the phase shift in the reflected signal an Agilent 8510C vector network analyzer was used.

The schematic in Fig. 4 shows a basic version of the sample board with a transistor type device at the 12 mK stage. This simplified version of the sample board comprises of an integrated inductor L and the sample that generally has conductive, inductive and capacitive properties depending on e.g. gate-voltage. In a reflectometry measurement one measures the reflected signal from the sample board that is given by a complex reflection coefficient Γ multiplied with the incoming signal. The sample board is a resonant system with an impedance Z that is a function of frequency and tuning of the sample, such that the complex reflection coefficient is:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{1}$$

where $Z_0 = 50\,\Omega$ is the impedance of the RF-lines [58].

Figure 4 shows the signal path in a reflectometry experiment where the carrier signal is injected into port 1, attenuated in the input line and coupled towards the sample board with a directional coupler. The reflected signal from the sample board is then amplified in the output line and measured at port 2. The third line (shown in green) is only present in the experiments with the SQUID amplifier presented in

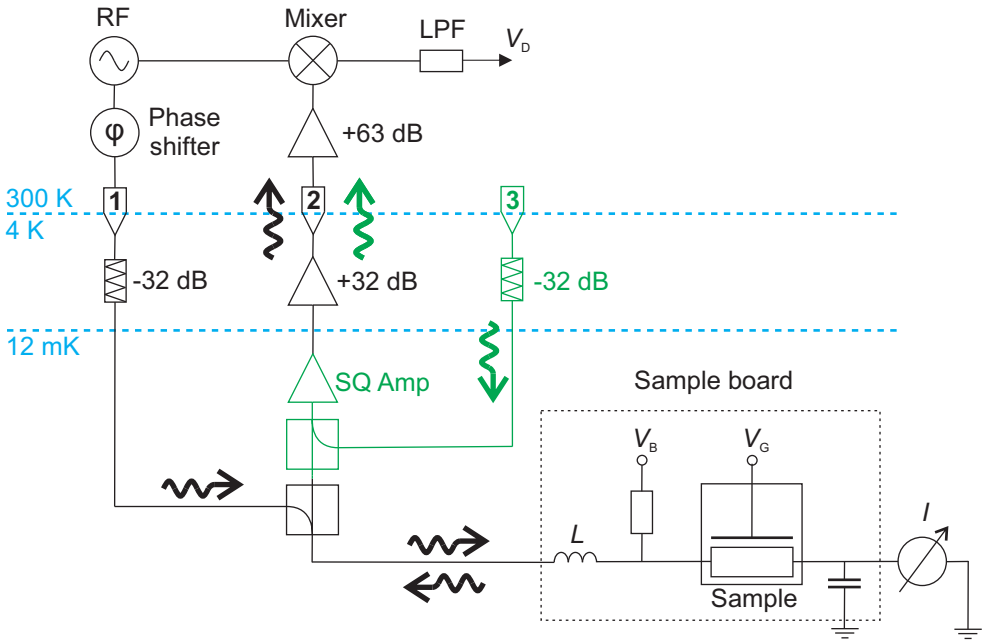

Figure 4: RF wiring of the dilution refrigerator with demodulation circuit and a simplified schematic of the sample board. The sample board contains an inductor L in series with a transistor type sample that is tunable with gate voltage V_G and bias voltage V_B. The DC current I can be measured in parallel to the RF signal. The RF-line from port 1 is coupled towards the sample board with a directional coupler and used for the input signal in a reflectometry measurement. The reflected signal is amplified in the output line and fed into the demodulation circuit at port 2. The demodulation circuit, comprised of a phase shifter, mixer and low pass filter (LPF), mixes-down the reflected signal to a DC voltage V_D. The green part of the circuit is only present in experiments with the SQUID amplifier (SQ Amp). A signal from port 3 is coupled towards the amplifier chain in the output line (towards port 2) such that the amplifiers can be tested independently of the reflection coefficient of the sample board. For part numbers and details see Appendix Tab. 2, Fig. 43, 44, 45 and 46.

Sec. 4.3. The input signal from port 3 is coupled into the output line ending in port 2 to test the amplifier chain independently of the reflection coefficient of the tank circuit.

For the RF measurements in Sec. 4.2 the output line included only one low temperature bipolar junction transistor (BJT) amplifier at 4 K (CITFL2 from Weinreb), while a superconducting quantum interference device (SQUID) amplifier with lower noise was added at the 12 mK stage in Sec. 4.3 (custom made by ez SQUID [59]). In both experiments the output signal at port 2 was either directly measured with

a spectrum/signal/vector network analyzer as described earlier or demodulated to a DC signal in the demodulation circuit. The signal-to-noise ratio at port 2 is dominated by the noise level at the input of the first low temperature amplifier, since the noise is subsequently amplified together with the signal to a higher level than any noise at a higher temperature stage. Since the noise at the input of the first amplifier often comes from the amplifier itself, it is crucial to employ low noise cryogenic amplifiers.

The demodulation circuit is shown in the 300 K section of Fig. 4. A measurement with the demodulation circuit uses the signal from the RF source, that is split and can therefore serve as the local oscillator for a mixer as well as the carrier signal for the reflectometry circuit. The carrier signal is reflected on the sample board, then amplified at low temperature and in the demodulation circuit, before it is fed into the RF input of the mixer. Since the local oscillator and the reflected signal are at the carrier frequency, the mixer produces a signal at twice the carrier frequency as well as at DC. The signal at twice the carrier frequency is filtered out with a low pass filter (LPF in Fig. 4) such that only the DC component V_{D} remains. Since this component depends on the amplitude and phase shift of the reflected signal, both quadratures of the reflected signal can be probed when the phase of the carrier signal is adjusted with the phase shifter in the demodulation circuit.

In a typical measurement the observed demodulated voltage V_{D} contains information about the amplitude as well as the phase of the reflection coefficient. For the case shown in Fig. 4, where the RF line is connected to one of the leads of the sample, most changes in V_{D} are due to a shift in both phase and amplitude of the reflected signal. This behaviour can correspond to a change in inductance, capacitance or conductance of the sample. If inductive changes can be neglected and the DC conductance is equal to the RF-conductance, it is possible to relate the changing impedance to capacitance and/or conductance

of the sample by comparing it with the DC conductance [50]. In a configuration where the RF line is connected to the gate of the sample and the tunnel rates into the island are comparable to the frequency of the input signal, the phase shift of the reflected signal can be related to a capacitance change and dissipative processes can be explained via “Sisyphus resistance” (for details see Ref. [44]). Gate based reflectometry is not used in this thesis, such that I will not explain this technique and refer to Ref. [44] for more details.

3 Quantum transport in silicon nanowires

Unlike electric transport in bulk transistors at room temperature, transport in nanowires can be heavily affected by confinement effects [60, 61]. In the limit of large nanowire diameters and high temperatures, however, transport through nanowires reaches the classical limit similar to bulk transistors [60].

The transition temperature and critical nanowire diameter separating quantum confined and classical bulk-like regime depends on the competition between two energy scales: the thermal energy of the electrons and the spacing of eigenenergies between different solutions of Schrödinger's equation in the boundary condition given by the nanowire cross section. If that energy spacing dominates over thermal effects, thermal excitation of electrons from one radial state to the next is very unlikely and the wavefunction in the radial direction is fixed. In that case the associated transport channel can carry at most one conductance quantum per spin/valley degeneracy in a channel without scattering [21]. As higher energy electrons become available due to e.g. a gate voltage, the conductance channels associated to the radial wavefunctions get populated successively and the associated conductance steps can be observed (for details see Sec. 3.1).

In an experiment, the associated step-like features in DC conductance can be less pronounced or not be observable due temperature effects [61] or scattering in the channel [62]. Instead, scattering from longitudinal potential variations can dominate and one might observe features from quantum interference of electron wavefunctions travelling along the nanowire axis [63] or even the formation of charge islands and zero dimensional transport [64]. In a temperature regime where thermal effects prevent clear features from zero dimensional transport or quantum interference, one-dimensional transport can manifest in the

scaling behaviour of the conductance as a function of temperature and bias voltage [62].

I will begin this chapter by introducing these theoretical concepts in more detail. Next, I will present my analysis of conductance data from Muhammad Mirza as a function of temperature, bias- and gate-voltage in a temperature range from 14 to 300 K that shows signatures of one dimensional transport. I will then present my measurements at 12 mK where I studied a sample with strong enough potential variations on the ends of the nanowire to form a charge island in the nanowire channel. The section will finish with the analysis of my low temperature measurements on nanowires in the one-dimensional transport regime. In the analysis of that experiment I will characterize the role of longitudinal scattering in the framework of quantum interference and determine the dominant scattering as well as decoherence mechanisms.

3.1 Theoretical concepts

This section covers some key concepts that are important for the experiments and data interpretation. Since the diameters of the presented nanowire devices are sub 10 nm I will introduce 1D confinement in a clean circular nanowire without scattering at zero temperature. In this context I will also explain how screening limits the doping density in large transistors and compare it to one-dimensional systems. This is essential for the interpretation of the data, because screening of a field from the gate electrode has an essential impact on the operation of nanowire transistors. Next I will show the transport models that are valid in a clean ballistic channel, a “dirty” system with many impurities and a channel with few impurities. This includes the discussion of the characteristic length scales that become relevant for determining the transport regime in the nanowire devices. I will finish the theory section by introducing the concept

of a single electron transistor and transport through a 3D confined system, since all measured nanowires show the associated features at low temperatures and gate voltages. A detailed explanation of the related quantum and mesoscopic physics is far beyond the scope of this thesis and I want to refer to the literature (e.g. Ref. [21]) for a more detailed discussion starting from fundamental quantum mechanics.

3.1.1 Metallic behaviour in highly doped semiconductors

The bandstructure of a crystal is calculated using Schrödinger's equation in periodic boundary conditions [21]. It describes the electron energy in conductive states as a function of momentum and therefore indicates the bands of electron energy where transport of charges through the crystal is possible. The system is conductive if the Fermi-energy in the crystal is in one of the energy bands from the bandstructure and non-conductive when the Fermi-energy is outside of the energy bands. In semiconductors there are two types of conductive bands that are separated by the "bandgap": the conduction band, where additional electrons enable transport through an otherwise unoccupied band, and the valence band, where a reduced number of electrons creates "holes" that correspond to missing electrons in the band and can carry a current. Holes in the valence band are commonly treated as positively charged quasiparticles that can travel through the crystal rather than a large electronic system missing one charge. In the following I will refer to electrons and holes as "charge carriers".

In a field-effect transistor the semiconductor is manipulated via capacitive coupling to a gate electrode such that charge carriers can be attracted. The gate electrode can thus be used to populate/depopulate the conductive states of the semiconductor in the valence band (for holes) and conduction band (for elec-

trons). In that way the conductivity and therefore the state of the transistor can be switched ON/OFF. The existence of an accessible conductive region (conduction/valence band) and non-conductive region (bandgap) is the defining property of a semiconductor. In contrast, metals do not have an accessible bandgap such that the material is conductive at all charge carrier energies and it is not possible to switch the conductivity OFF. Electrical insulators have a very large bandgap and it is not possible to attract charge carriers sufficiently to raise/lower the Fermi-energy into one of the conducting bands with a gate electrode.

In "normally-ON" semiconductor devices, that are conductive at zero gate voltage, there is another consideration that determines whether the device can be switched OFF completely: is the field screened at the surface of the material or does it remain sufficiently strong throughout the device to switch the bulk of the material? The ability to screen fields at the surface depends on the concentration of free charges that can shift position in response to the outside field. In semiconductor devices this property can be manipulated by introducing "dopants" in the crystal lattice. Dopants are atoms for which it is energetically favourable to integrate into the crystal lattice due to the bonds formed by the valence electrons. There are, however, either not sufficient bonds for all valence electrons, such that one electron is only very loosely bound to the dopant creating a free electron at finite temperature, or there are too few valence electrons, such that a free hole is created at finite temperatures. The resulting free charge carriers increase the ability to screen outside fields. One characteristic length scale is the distance that an outside electric field can penetrate into a semiconductor surface before it gets screened completely. In a regime where quantum confinement

of charge carriers is not relevant, this length scale is given by the 3D Debye-length [65]:

$$l_{\mathrm{D}} = \sqrt{\frac{\varepsilon_{\mathrm{r}}\varepsilon_0 T k_{\mathrm{B}}}{n_{3\mathrm{D}} e^2}} \tag{2}$$

In this expression $n_{3\mathrm{D}}$ is the charge carrier concentration, T is the temperature, e is the electron charge, k_{B} is Boltzmann's constant, ε_{r} is the relative- and ε_0 the vacuum permitivity.

Normally-ON transistors can only be switched OFF completely when the Debye-length is larger than the thickness of the semiconductor material – otherwise there is a conductive section of the semiconductor that the field does not reach. For the doping concentrations in the presented silicon nanowire samples on the order of 10^{19}-$10^{20}\,\mathrm{cm}^{-3}$, the Debye length is 1.3-0.4 nm at room temperature and 24-8 pm at 100 mK. In the presented devices this means that all bulk structures including the silicon under the bondpads, the leads and especially the sections of the leads that are covered by the gate (see Fig. 1b) are conductive at all gate voltages and temperatures. For bulk like transport in the nanowire channels, it would not be possible to switch the transistors OFF unless dopant deactivation from dielectric or surface effects significantly increases compared to the previous devices from Sec. 2.1.2 – This is unlikely since the added gate electrode should reduce dopant deactivation [16].

In quantum confined systems on the other hand, charge carriers are not able to move freely in confinement direction and are therefore unable to effectively screen outside field components in the associated dimension (see Sec. 3.1.2). In a nanowire at zero temperature this means that radial fields cannot be screened because charge carriers can only travel along the nanowire axis and not in radial direction. Even for higher temperatures, where thermal fluctuations enable more movement in radial direction, the ability

to screen radial fields can be significantly suppressed. Nanowires with high carrier concentrations can therefore still be switched OFF with a field from the gate if the nanowire radius is small enough and quantum confinement is significant.

3.1.2 Quantum confinement into one dimension

Quantum confinement into one dimension refers to a situation where the boundary conditions for a charge carrier wave in two dimensions are tight enough to lead to quantized energy states associated to standing wave modes. If there is no confinement in the remaining dimension, the energy of a charge carrier E_{tot} consists of the energy of the confined mode E_{n} as well as the kinetic energy of a free travelling wave in the unconfined dimension with effective mass m^* and wave vector $k_{||}$ [21]:

$$E_{\mathrm{tot}} = E_{\mathrm{n}} + \frac{\hbar^2 k_{||}^2}{2m^*} \tag{3}$$

If the boundary is not tight, i.e. the sample is large in confinement direction, the consequences are very minimal because the energy spacings between different modes are much smaller than e.g. thermal energy $E_{\mathrm{th}} \gg |E_{\mathrm{n}} - E_{\mathrm{n+1}}|$. In that case the distributions of energy and momentum in the confined dimensions are heavily thermally broadened and approach a continuum that corresponds to the classical limit. If thermal broadening is smaller than the energy spacing of the confined modes ($E_{\mathrm{th}} \ll |E_{\mathrm{n}} - E_{\mathrm{n+1}}|$), quantum confinement becomes significant and every charge carrier is trapped in a mode with the associated energy E_{n}. This implies that the movement of charge carriers in the confined direction is suppressed, which affects

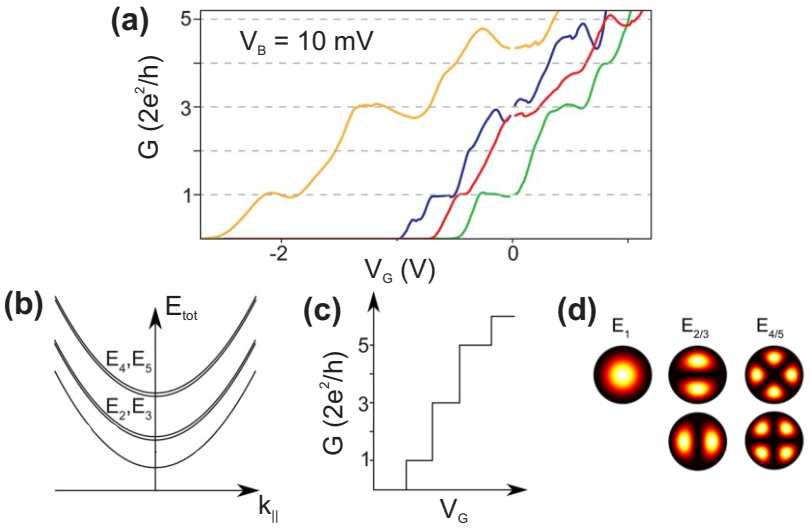

Figure 5: Transport in a InSb nanowire from Kammhuber *et al*.[13]: a) Conductance G in a measurement as a function of gate voltage V_G for 4 different devices with different gate coupling b) Calculated charge carrier energy E_{tot} as a function of the wave-vector in the unconfined dimension $k_{||}$ for the first 5 subbands in a perfectly circular nanowire geometry. c) Calculated conductance G as a function of gate voltage V_G at temperature 0 K. d) Absolute of the 5 lowest eigenenergy solutions to Schroedinger's equation in a nanowire boundary condition as a function of radius and angle.

the electric properties of the system such as the screening of outside fields (see Sec. 3.1.1).

The confining boundary of a nanowire is given by the diameter and the modes for a perfect circular cross section are shown in Fig. 5d. The bandstructure for this case was calculated by Kammhuber *et al*. [13] and is shown in Fig. 5b, where the conduction band splits into subbands corresponding to the confined modes. Each subband carries a maximum of one conductance quantum e^2/h per valley and spin degeneracy if there are no other reflections from e.g. impurities or a contact resistance [21]. The resulting conductance G as a function of gate voltage V_G is shown in Fig. 5c, where the conductance increases by an integer multiple of the conductance quantum when a subband becomes accessible at increasing gate voltage. The number of conductance quanta in a step depends on the degeneracy of the subband due to spin and valley. Depending on the geometry of the nanowire cross section there can also be two degenerate subbands

that become accessible at the same energy. This step-like behaviour is a signature of one dimensional transport with negligible scattering in the channel – also called "ballistic" transport.

Figure 5a shows the data in four different InSb nanowire samples with different gate couplings and clear conductance steps. Compared to the theory in Fig. 5c, the steps in the measurement are less sharp due to the broadened energy distribution of electrons at finite temperature. The measurement also shows additional fluctuations that are likely due to longitudinal quantum interference effects from scattering on impurities or lattice defects as described in the next section.

3.1.3 Quantum interference and weak localization

In the context of electric transport, quantum interference refers to the interference of charge carrier waves with their time-reversed counterparts after a reflection. In principle this also describes the standing wave modes in the nanowire cross section, such that we sometimes speak of "transverse quantum interference modes". In contrast to this strong confinement of electrons by the high boundary potentials at the walls of the nanowire, other quantum interference phenomena do not require 100% reflection probability. In this case constructive interference of partly reflected electron waves can lead to an increased probability of charge carriers being localized in a device. This phenomenon is called "Weak localization" (WL) [21, 60] and manifests in a reduced conductance because the localized charge carriers do not contribute to transport.

In ballistic nanowires without scattering in the channel, WL can originate from reflections at the ends of the wire. This phenomenon, called "Fabry-Pérot interference", is reproducible over different samples if

they are geometrically identical. Strong features from Fabry-Pérot interference can be observed when the coherence length of the charge carriers l_ϕ, which is defined as the average distance a charge carrier travels before its phase gets randomized by inelastic scattering, is larger than the length of the channel L. At the same time elastic scattering in the channel needs to be unlikely, since otherwise the interference path would be interrupted with a high probability. The associated parameter is called the "elastic mean-free-path" l_e that a charge carrier travels on average before scattering. If either inelastic or elastic scattering in the channel is likely, i.e. $l_\Phi < L$ or $l_e < L$, features from Fabry-Pérot interference will average out in a DC measurement since most charge carriers do not interfere coherently or do not get reflected from the ends of the nanowire. Averaging over many charge carriers can also be related to the energy distribution of charge carriers injected into the channel and is relevant for all kinds of features in DC transport – larger bias voltages or temperature broadening can therefore cause averaging.

In systems with more impurities or longer channels there is significant elastic scattering in the channel and $l_e < L$. Quantum interference and WL can occur on average in this regime if $l_\phi > l_e$ and there is constructive interference from reflected carrier waves on potential variations due to imperfections in the crystal or on the surface. Since these fluctuations are typically randomly distributed and can usually not be reproduced over many samples, this type of quantum interference produces signatures that are unique to the sample unless there is averaging over many localization sites. If there are many localization sites this results in a constant correction term to the Drude conductivity from averaging over multiple independently fluctuating parts of the channel ($l_\phi \ll L$) and/or over many localization sites ($l_e \ll L$) [21]. This diffusive WL regime was described by Altsuhler and Aronov with a correction term δG in case the

coherence length is larger than the mean-free path [66, 67]:

$$\delta G_{\mathrm{WL}} = -g_{\mathrm{s}} g_{\mathrm{v}} \frac{e^2}{hL} l_{\phi} \tag{4}$$

where g_{s} (g_{v}) is the spin (valley) degeneracy of the channel.

In mesoscopic devices with fewer localization sites the conductivity can depend on the charge carrier energy because resonances at different localization sites might not average to the same effect for all charge carrier energies. Since the charge carrier energy in a transistor is controlled indirectly with an electric field from a gate, this results in conductance fluctuations as a function of the gate voltage – so called "Universal Conductance Fluctuations" (UCF).

The smallest conductance is reached when the localization site is in resonance with the charge carrier energy such that one transport channel is blocked and the conductance drops correspondingly. In the ideal case with perfect contacts to the channel and an otherwise ballistic device, the conductance drop is one conductance quantum per degeneracy of the channel. This corresponds to the maximum fluctuation amplitude in WL and can only be reached at low temperatures [21].

At higher temperatures the amplitudes can decrease with increasing temperature due to the broadened charge carrier energy distribution. This causes a smaller fraction of carriers to be on resonance with the localization site, such that a smaller effect is observed in the total conductance. Another mechanism that reduces the amplitude of UCF with temperature is a decreasing coherence length l_{ϕ} due to averaging over independently fluctuating parts of the channel in the regime $l_{\phi} < L$. At higher temperatures this phenomenon is often caused by increased phonon scattering, but at croyogenic temperatures phonon

scattering is usually suppressed and decoherence is dominated by e.g. thermal fluctuations in the electron bath [68].

We can asses whether the amplitude is dominated by averaging over muliple fluctuating segments or thermal broadening by comparing l_ϕ to the "thermal length":

$$l_T = \sqrt{\frac{\hbar D}{k_B T}} \tag{5}$$

Here D is the diffusion constant, k_B is Boltzmann's constant and T is the temperature. In case $l_T \gg l_\phi$, thermal broadening is negligible while it affects the conductance fluctuations significantly for $l_T \lesssim l_\phi$.

The behaviour of the UCF amplitude can be studied using the root-mean-square of the conductance over the gate voltage ΔG. In case thermal broadening is negligible compared to the width of the resonance from the localization site and there is no averaging over independently fluctuating parts of the channel ($l_\phi < L$), ΔG can be calculated following:

$$\Delta G = \beta e^2/h \tag{6}$$

Here β is a factor on the order of 1 that includes the degeneracies g_s and g_v as well as reduced conductance in the device from e.g. contact resistance. In case $l_\phi \ll l_T$ and $l_\phi < L$ the averaging over independently fluctuating segments dominates over thermal broadening and the expression for ΔG reads [21]:

$$\Delta G = \beta \frac{e^2}{h} \left(\frac{l_\phi}{L} \right)^{3/2} \tag{7}$$

If, on the other hand, $l_\phi \gg l_T$ and $l_\phi < L$ there is an additional factor from the broadening of the energy distribution and the behaviour follows the form [21]:

$$\Delta G = \beta \frac{e^2}{h} \left(\frac{l_\phi}{L} \right)^{3/2} \frac{l_T}{l_\phi} \tag{8}$$

Using these equations, the temperature dependence of $\Delta G(T)$ can be used to determine the dominant processes that are suppressing UCF if the temperature dependence of the coherence length is known. The devices presented in this thesis are one dimensional nanowires with a very high charge carrier concentration, such that electrons are spaced closely together and electron-electron interactions are relevant. At low temperatures, where electron-phonon scattering is unlikely, we therefore expect a dominant dephasing mechanism from electron-electron interactions called "Nyquist-dephasing" [66]. In this regime the coherence length is:

$$l_\phi = \left(\frac{Dh^2}{4\pi^2 \sqrt{2} R_0 e^2 k_B T} \right)^{1/3} \tag{9}$$

where D is the diffusion constant and R_0 is the classical Drude resistance without WL.

For the case in Eq. 6, where the coherence length is larger than the nanowire length, the temperature dependence of the coherence length is irrelevant and $\Delta G(T)$ is constant. For the cases where the coherence length is smaller than the nanowire, Nyquist dephasing in 1D predicts a coherence length $l_\phi \propto T^{-1/3}$ such that $\Delta G \propto T^{-1/2}$ for $l_\phi \ll l_T$ and $\Delta G \propto T^{-2/3}$ for $l_\phi \gg l_T$.

3.1.4 1D transport models from nearest neighbour hopping and weak localization to Luttinger liquids

In the previous section I have discussed WL from partial reflection of charge carriers on local impurity fluctuations in the conduction band or the ends of the channel. In case there are many potential fluctuations and charge carrier energies are smaller than the maxima of the potential, transport can be modelled as hopping of charges from one localized state to another. The conductance in this regime, called "strong localization", heavily depends on temperature because conductivity requires thermal activation of charge carriers over the barriers between localized states. Strong localization can be used to model e.g. the transport in the "impurity-band", that is made from localized states attached to charged dopants, when charge carriers do not have enough energy to reach the conduction band [69]. The predictions for temperature scaling of the conductance in this regime depend on the existence of a "Coulomb gap" due to a series of tunnel coupled islands in the channel [70, 71]. For strong localization without a Coulomb gap the conductance reads [67]:

$$G = G_0 \exp\left(-\left(\frac{T_0}{T}\right)^n\right) \tag{10}$$

where G_0 and T_0 are device dependent constants and $n = (dim+1)^{-1}$ depends on the dimensionality of the transport dim. For strong localization with a Coulomb gap, $n = 0.5$ independent of the dimensionality [70].

While strong localization is dominated by interactions of charge carriers with potential fluctuations and describes a systems with many impurities, one-dimensional low-temperature transport in a clean ballistic channel is dominated by strong electron-electron interactions. It is not possible to model such a system

in the framework of a Fermi liquid where electrons are described as quasi-particles with an effective mass that accounts for weak electron-electron interactions [21, 72]. Instead electrons are localized into a periodic lattice and transport is carried by wavelike excitations of the electron lattice in a, so called, "Luttinger liquid" [11] (or "Tomonaga-Luttinger liquid"). One important experimental signature of this system is the excitation of separate spin- and charge carrier waves that were measured in tunnel experiments between two nanowires [14]. The conductance G in a Luttinger liquid as a function of temperature T and source-drain bias V_{B} is given by [73]:

$$G = AT^{\alpha}\cosh\left(\gamma\frac{eV_{\mathrm{B}}}{2k_{\mathrm{B}}T}\right)\left|\Gamma\left(\frac{1+\alpha}{2}+\gamma\frac{ieV_{\mathrm{B}}}{2\pi k_{\mathrm{B}}T}\right)\right|^2 \tag{11}$$

where A is a proportionality constant, k_{B} is Boltzmann's constant and $\Gamma(x)$ is the Gamma-function. If the channel is connected to the leads via tunnel barriers, γ is a constant that depends on the relative voltage drop across the two barriers. If one barrier dominates in an asymmetric sample $\gamma = 1$, while $\gamma = 0.5$ for symmetrical barriers. The constant α is a measure of the electron-electron interaction strength where $\alpha \approx 0$ corresponds to weak interaction in the Fermi liquid limit.

There are two characteristic conductance regimes with a power-law dependence:

For $eV_{\mathrm{B}} \ll k_{\mathrm{B}}T$

$$G \propto T^{\alpha} \tag{12}$$

and for $eV_{\mathrm{B}} \gg k_{\mathrm{B}}T$

$$G \propto V_{\mathrm{B}}^{\alpha} \tag{13}$$

In an experiment it is often difficult to prove that a system is a Luttinger liquid beyond doubt without showing the separation of spin and charge excitation. Nevertheless power-law dependent conductance has been associated to Luttinger liquids in several systems including carbon nanotubes [73], MoSe nanowires [74] and polymer nanowires [75]. In this chapter I will show a similar power law dependence in highly doped and non-ballistic nanowires, where a clean Luttinger liquid is not possible. The scaling according to Eq. 12 and Eq. 13 is therefore no unequivocal proof of a clean Luttinger liquid.

The three models introduced so far correspond to a diffusive "dirty" regime, a non-diffusive WL regime as well as a ballistic regime where electron-electron interactions are dominant. However, transport could be in an intermediate regime, where hopping between localized states or quantum interference are also affected by strong electron-electron interactions.

The transition from clean Luttinger liquid to the diffusive regime is described in Refs. [76] and [77]. I will focus on the model by Mishchenko *et al*. [77] that fits the data from the nanowires and describes the transition from Luttinger liquid to strong localization. The model by Mora *et al*. [76] covers the transition from Luttinger liquid to WL averaged over many sites. While there are WL effects in the nanowire samples at low temperatures, the associated features indicate WL in the framework of UCF rather than the averaged correction term to diffusive transport from Eq. 4. The model by Mora *et al*. [76] does not fit the data and I will not discuss it in detail. Nevertheless, transport in the nanowires certainly is affected by WL and the concepts discussed in the model might be of use for the interested reader.

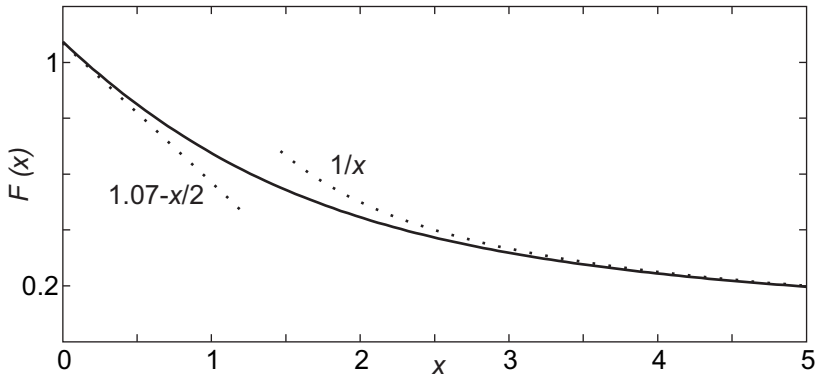

Figure 6: Scaling function $F(x)$ from the theory by Mishchenko *et al*.[77]. The dashed lines show the behaviour for $x \ll 1$ according to $F(x) = 1.07 - x/2$ and $F(x) = 1/x$ for $x \gg 1$.

The model from Mishchenko *et al*. predicts a conductance in a 1D non-ballistic channel:

$$G \propto \exp\left(-\sqrt{\frac{T^*}{T}} F\left(\frac{eV_\mathrm{B}}{k_\mathrm{B}\sqrt{T^* T}}\right)\right) \tag{14}$$

with $k_\mathrm{B}T^*$ being a measure of the height of the potential fluctuations in the channel and $F(x)$ being a scaling function shown in Fig. 6. At $V_\mathrm{B} = 0$ the scaling function is constant at $F(0) = 1.07$, such that the conductance follows the behaviour from 1D strong localization described in Eq. 10. The scaling function is approaching $F(x) = 1/x$ for $x \gg 1$ and $F(x) = 1.07 - x/2$ for $x \ll 1$.

The number of parallel conducting channels per valley in a silicon nanowire device can be extracted from the parameter T^* using:

$$N = \frac{e^2}{16\varepsilon_0\varepsilon_\mathrm{r}\pi T^* k_\mathrm{B}\tau v_\mathrm{F}} \ln\left(d_\mathrm{g}/R\right) \tag{15}$$

where τ is the elastic momentum relaxation time, $\varepsilon_\mathrm{r} = 3.9$ is the relative permitivity of SiO_2, ε_0 is the vacuum permitivity, v_F is the Fermi-velocity, d_g is the distance to the gate and R is the nanowire radius.

The average Fermi-velocity in the channels can be calculated from the 1D charge carrier density n_{1D}:

$$v_F = \frac{\hbar 2\pi n_{1D}}{g_s g_v m^*} \tag{16}$$

with m^* being the effective mass and g_s (g_v) being the spin (valley) degeneracy.

3.1.5 Transport in single electron transistors

After discussing transport in nanowires with confinement into one dimension, I will now discuss transport through a charged island. While there can be quantum effects from 3D quantum confinement for very small islands, this system is typically dominated by the quantization of charge rather than the modes of confined wave functions. The presented model is relevant for the experiments on the GaAs quantum dot as well as for transport in the nanowire samples just before the channel switches OFF at low temperatures. Transport through an island requires leads that are separated via tunnel barriers. Inevitably this geometry causes capacitive coupling from the leads to the charge island such that electrostatic effects become important. In a transistor-type device additional capacitive coupling to the island comes from a gate electrode. Since transport through the tunnel barriers is not allowed in classical physics I will introduce a semiclassical picture, where energies in the island are calculated classically with a quantum mechanical correction term depending on island size and transport is facilitated by the tunnel effect. This model requires an integer number of trapped charges, which implies an access resistance of the charge island larger than resistance quantum.

Apart from charge island, tunnel barriers and leads, the relevant sample geometry for this thesis also

includes a gate electrode and the devices are called “Single electron transistors” (SET). In such a system the charge carrier energy can be calculated in the, so called, “Constant Interaction Model"(CIM) [78, 79]. The CIM assumes constant interaction in the sense that the island is coupled to the environment as well as the source, drain and gate contacts via fixed capacitances that do not depend on the number of charge carriers on the island. It considers two contributions to the energy of the system: a classical contribution where charges interact via constant capacitances as well as a quantum mechanical contribution that depends on the details of the island and its charge state. The classical contribution for N electrons on the island is written in terms of capacitance C_{G} to the gate, C_{SO} to the source and C_{DR} to the drain as well as the associate voltages across the capacitances V_{G}, V_{SO} and V_{DR}. The overall energy $U(N)$ is the sum of both contributions, in which the single particle energies on the island E_{n} add up to the full quantum mechanical contribution of the island [80]:

$$U(N) = \frac{[-|e|(N-N_0) + C_{\mathrm{SO}}V_{\mathrm{SO}} + C_{\mathrm{DR}}V_{\mathrm{DR}} + C_{\mathrm{G}}V_{\mathrm{G}}]^2}{2C} + \sum_{n=1}^{N} E_{\mathrm{n}} \tag{17}$$

In this equation $N_0|e|$ is an offset charge that compensates for a background charge from e.g. dopants on the island and $C = C_{\mathrm{SO}} + C_{\mathrm{DR}} + C_{\mathrm{G}}$ is the total capacitance.

For weak interaction between the leads and the island, e.g. in devices with large tunnel barriers, transport at low temperatures is dominated by processes that conserve energy in the CIM (see Fig. 7) [81]. It is therefore useful to consider the electrochemical potential μ_{N} defined as the difference between overall

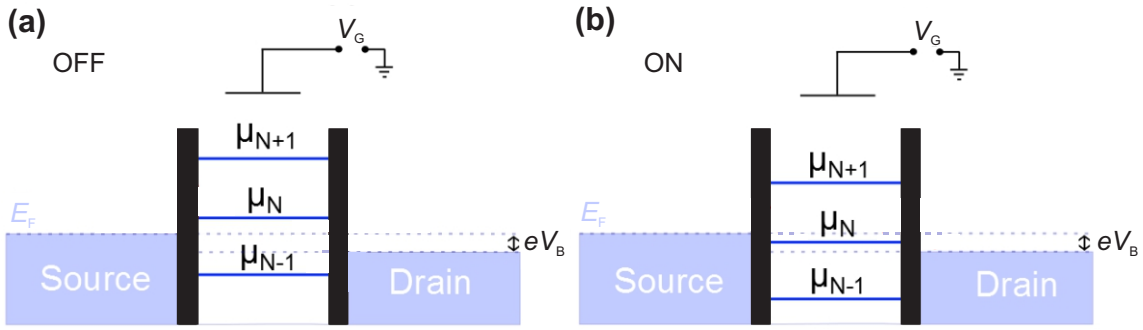

Figure 7: Schematic of the potential landscape in an SET device along the axis from source to drain with the y-axis denoting energy. The source lead is occupied with electrons up to the Fermi energy E_F, while the highest charge carrier energy in the drain is lowered by the bias voltage V_B. The tunnel barriers are drawn in black and the island is represented by a ladder of chemical potentials μ_N. a) Device in the OFF state: "Coulomb-blockade" b) Device in the ON state: Single electron current.

energy for N and $N-1$ charges on the island [80]:

$$\mu_N = U(N) - U(N-1) = (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|}(C_{SO}V_{SO} + C_{DR}V_{DR} + C_G V_G) + E_N \qquad (18)$$

The expression $E_C = \frac{e^2}{C}$ is called charging energy and appears in the first two terms that are attributed to classical electrostatics. The last term is a chemical/quantum mechanical contribution due to level filling from N-1 to N in an island with 3D quantum confinement. Notably Eq. 18 is proportional to the gate voltage V_G, such that the "ladder" of electrochemical potentials for different charge states can be shifted with the gate.

Fig. 7a shows the potential landscape in a device with the horizontal axis corresponding to the path from source to drain and the vertical axis denoting energy. The energy of electrons in the source reaches up to the Fermi energy E_F while the highest electron energy in the drain is lowered by a bias voltage V_B. The tunnel barriers are drawn in black and the island shows the chemical potentials associated with the

addition of a charge according to Eq. 18. Since the electrostatics of the island can be manipulated by a gate or outside field, it is possible to turn a current OFF/ON by driving the electrochemical potential on the island out of/into the energy window defined by the source and drain potentials. These two configurations are depicted in Fig. 7, where a) corresponds to a device that is switched OFF and b) to a device in the ON-state. If the island potential is adjusted close to one of the edges of this window, a small field is sufficient to switch the transistor and charge/field sensing is possible with high accuracy [82].

For high temperature operation the distance between two rungs of the electrochemical potential ladder, called "addition energy", needs to exceed thermal energy such that the SET does not experience OFF state current through thermally excited transport [28]. Assuming all voltages stay constant, the addition energy is given by:

$$E_{\text{add}} = \mu_{\text{N}} - \mu_{\text{N-1}} = E_{\text{N}} - E_{\text{N-1}} + \frac{e^2}{C} \tag{19}$$

In order to achieve high temperature operation, the overall capacitance can only be reduced to some extent, because it is also needed for electrostatic control of the system. This leaves the quantum mechanical component of the addition energy $E_{\text{N}} - E_{\text{N-1}}$. Similar to a particle in a box, this contribution increases with decreasing island size, such that SETs with smaller islands can operate at higher temperatures. I have briefly discussed efforts towards high temperature operation of transistors in the Introduction and also want to refer to one of my articles in this context [37].

3.2 Transport from 293 K to 14 K

The following section presents current and conductance data from nanowire samples with a nominal doping density of Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ at temperatures from 14 K to 293 K. At room temperature (293 K) the switching behaviour of the nanowire transistors shows a strong dependence on the nanowire diameter which could be related to a dimensional crossover in the screening of outside fields. This agrees with previous measurements on similar devices presented in Sec. 2.1.2, where a transition to lower dimensional transport was already suggested. At low bias and lower temperatures there is a zero-bias feature in the conductance that has been observed before in 1D systems and further substantiates the hypothesis of confined electrons into 1D [73, 26, 75]. The feature disappears following a power-law as a function of bias voltage similar to previous reports in 1D systems where the feature was related to a Luttinger liquid [73, 74, 75]. In the presented non-ballistic devices, however, this cannot be related to a clean Luttinger liquid. Instead the temperature scaling of the conductance at zero bias follows Eq. 10 from Sec. 3.1 suggesting one dimensional strong localization.

3.2.1 Transistor performance

The nanowire devices were studied at room temperature and high bias voltage to compare their performance to CMOS transistors. For that purpose M. Mirza has measured the current through the samples as a function of gate voltage at 293 K using an Agilent B1500 parameter analyzer and a Cascade microtech room-temperature probestation [52].

The inset of Fig. 8 shows a transmission electron microscope image of a device similar to the measured nanowire. The image shows data from electron energy loss spectroscopy (EELS), where the energy of the detected electrons from different parts of the device cross section can be used to distinguish oxide from silicon and metal. Apart from the nanowire cross section and oxide thickness, the EELS measurement reveals a gap in the oxide and gate below the nanowire. This could impact the gate-coupling and might be detrimental to the nanowire performance as a transistor.

The main panel of Fig. 8 shows the source-drain current I at a bias voltage of 1.5 V as a function of gate voltage V_{G} through three nanwowires with diameters 8 nm (red), 16 nm (blue) and 24 nm (black). The 8 nm nanowire device can be pinched OFF to below the detection limit of 0.1 pA and the ON/OFF current ratio between -1 V and 1.5 V gate voltage is over 10^7. The current switches ON exponentially below a characteristic gate voltage called "threshold voltage" V_{th}. The sharpness of the switch-ON is characterized by the subthreshold slope (SS) that is defined as the inverse slope of the logarithm of the current as a function of gate voltage below V_{th}. Theoretically the lower limit to the SS in a FET transistor is $58.6\,\mathrm{mV\,dec^{-1}}$ at 293 K, where "dec" means an order of magnitude in current[83]. For the 8 nm nanowire transistor the SS is $66\,\mathrm{mV\,dec^{-1}}$, which is 112 % of the theoretical limit but only 104 % of the best performing FinFET transistors at $63\,\mathrm{mV\,dec^{-1}}$ [84]. The switching performance of the 8 nm nanowire is therefore comparable to state-of-the art transistors.

Figure 9a shows the current I in the 8 nm diameter nanowire above threshold voltage as a function of bias voltage V_{B} at gate voltages from -0.25 to 2 V. As expected for a field-effect transistor, there is a region where the current is linear with bias voltage ($V_{\mathrm{B}} < V_{\mathrm{G}} - V_{\mathrm{th}}$, $V_{\mathrm{G}} > V_{\mathrm{th}}$) and a region where the current saturates when the capacitive effect from the accumulated charge at the source dominates over the gate

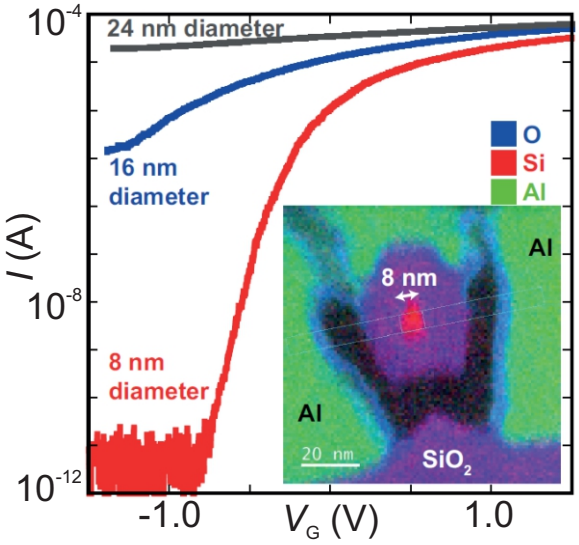

Figure 8: Current I as a function of gate voltage V_G through Si nanowires with nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ and three different diameters. The devices were measured with a bias voltage of 1.5 V and at a temperature of 293 K. Inset: elemental map of a cross section of the smallest nanowire measured by TEM-EELS [52]. The linecut indicated by the white box is shown in the Appendix.

($V_B > V_G - V_{th}$ and $V_G > V_{th}$) [83]. The 8 nm diameter nanowire therefore behaves like an FET, with an electrostatic control of the channel that is sufficient to enable state-of-the-art transistor performance, despite the gap in the wrap-around gate below the nanowire (shown in the inset of Fig. 8).

In contrast to this transistor-like switching behaviour, the 16 nm and 24 nm devices only reach ON/OFF ratios of 10 and 2. Additionally it is not possible to deplete the channel in the measurement range of the gate voltage, such that the OFF state of the transistor and therefore the bandgap is not accessible. Consequently it is not possible to quantify the switching in terms of the SS for the 16 nm and 24 nm devices since there is no clear region with exponential increase in current as a function of gate voltage. The 16 nm and 24 nm devices are therefore not suitable for transistor applications at room temperature.

The diameter dependent switching behaviour suggests that the devices are semiconducting at small diam-

eters and become increasingly metallic as the diameter increases. This could be related to screening of the electric field from the gate, that is characterized by the Debye length in 3D according to Eq. 2. The Debye length depends on the activated doping concentration which is likely to be higher than in the previously measured samples from Sec. 2.1.2 due to the addition of a gate [16]. Assuming at least the activated doping density from the previous measurements on similar devices with the same nominal doping, the Debye length at room temperature can be estimated to be $l_{\mathrm{D}} \leq 0.12\,\mathrm{nm}$. If the screening is 3D, the nanowires should then behave metallic with very limited response to a gate-voltage since the field cannot penetrate all the way through the channel to switch the device OFF. This could explain the behaviour of the 16 nm and 24 nm devices, but does not agree with the excellent transistor performance of the 8 nm diameter nanowire. This suggests a transition in the screening of outside fields for decreasing nanowire diameter from 3D screening, with charges having freedom of motion in radial direction, to 1D screening where the movement in radial direction is suppressed as discussed in Sec. 3.1.2. For decreasing nanowire diameter the outside field can therefore not be screened effectively and the channel can be switched with nearly optimal SS for the 8 nm diameter device. More evidence for 1D transport can confirm this interpretation and will be presented in the remainder of this chapter.

Other 1D features, such as the signature conductance steps for ballistic 1D transport as described in Sec. 3.1.2, are not observed in Fig. 8. Given the temperature of 293 K and the large number of scattering sites from the high doping density, this is to be expected due to thermal broadening and non-ballistic transport. Additionally, the bias voltage of 1.5 V leads to a broad range of electron energies that average out the effect of a resonance from e.g. quantum interference that is only significant in a smaller energy window.

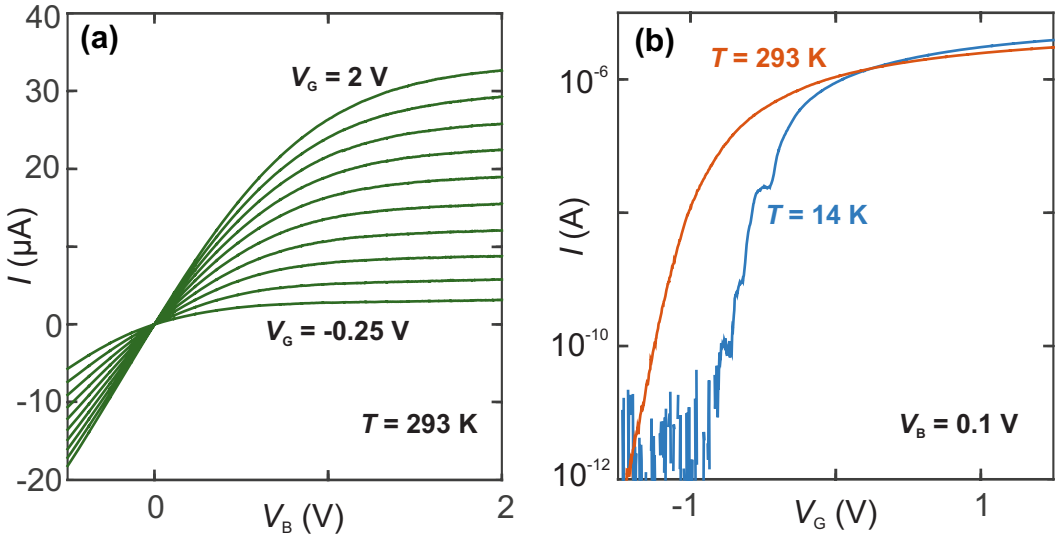

Figure 9: Transport in an 8 nm diameter nanowire with nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$. a) Current I at 293 K as a function of bias voltage V_B at different gate voltages V_G from -0.25 V to 2 V. b) Current I as a function of gate voltage V_G measured at temperature T = 293 K (red) and at 14 K (blue) with a bias voltage $V_\mathrm{B} = 0.1\,\mathrm{V}$.

Next we reduce thermal broadening by cooling the device to 14 K and use a lower bias voltage of $V_\mathrm{B} = 0.1\,\mathrm{V}$. Figure 9b shows the current I as a function of gate voltage V_G for two temperatures 293 K (red) and 14 K (blue). As expected for FETs, the 293 K curve is shifted in gate voltage due to thermally excited charge carriers that produce a current before the conduction band is populated with ground state electrons [83]. While the data at 293 K is smoothed from thermal broadening, the 14 K curve shows additional fluctuations. The features in the low gate voltage region ($V_\mathrm{G} < -0.8$ V) can be attributed to Coulomb blockade from one or multiple charge islands with Coulomb peaks above the noise level of the measurement (0.1 pA). The fluctuations above a gate voltage of -0.8 V could be associated to quantum interference in the framework of UCF and/or transport through subbands as discussed in Sec. 3.1. A detailed analysis of similar features is part of Sec. 3.3, where I will investigate whether the fluctuations could be related to subbands or UCF. In the remainder of this chapter, I will analyze the behaviour as a

function of bias at lower temperatures to find more evidence for 1D transport.

3.2.2 Zero-bias gap

In the previous section I have characterized the transistor behaviour as a function of gate voltage and at relatively large bias voltages. In this section I will focus on measurements at low bias voltages, where the energy distribution of charge carriers is less broad and there is less averaging over many charge carrier energies. I will present DC measurements on the 8 nm diameter nanowire from the previous section as a function of gate voltage V_G, bias voltage V_B and temperature T. The samples were cooled down in a Lakeshore CRX-6.5 K Cryogenic probe station and measured with an Agilent B1500 parameter analyzer by Muhammad Mirza [52].

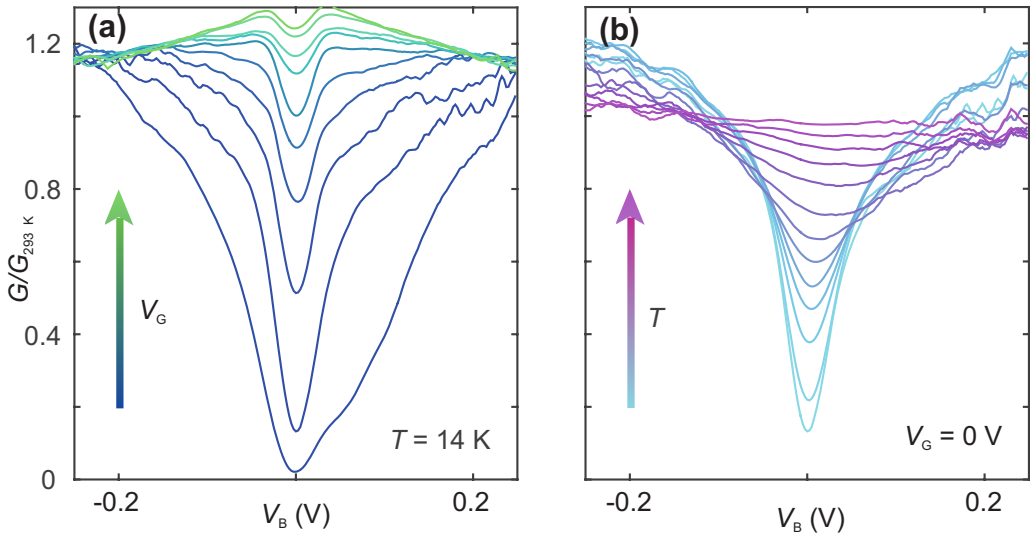

Figure 10: Transport in an 8 nm diameter nanowire with nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$. Conductance as a function of bias voltage V_B normalized by the corresponding data at 293 K. The normalization removes the regular transistor behaviour from the data and isolates the zero-bias feature. a) Normalized conductance as a function of bias voltage at different gate voltages from -0.25 V to 2 V. b) normalized conductance at different temperatures from 14 K to 293 K.

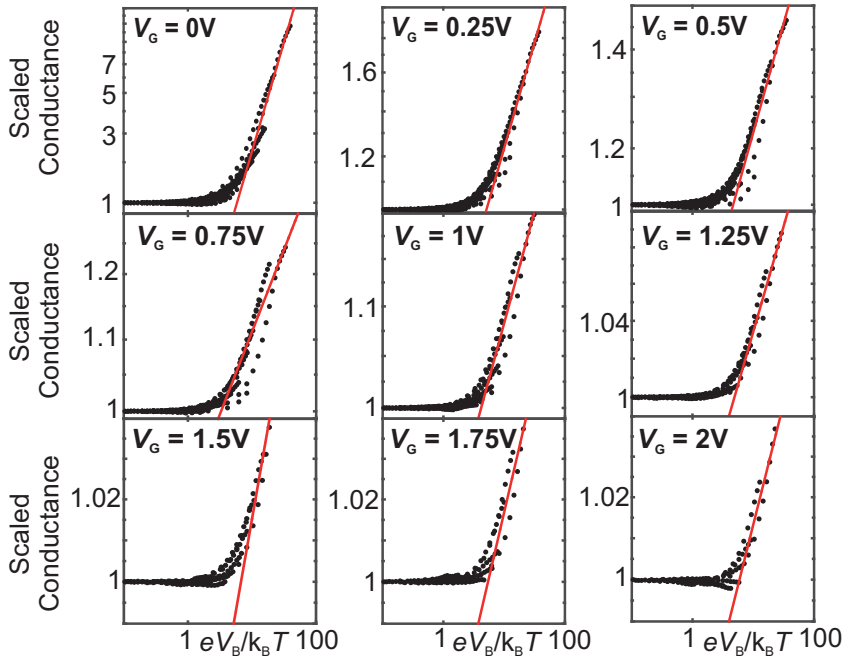

Figure 11: Transport in an 8 nm diameter nanowire with nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ at different gate voltages V_G. Each plot shows multiple data sets of normalized conductance taken at temperatures from 14 K to 293 K that were each scaled by the normalized conductance at zero bias at the respective temperature. The data is plotted as a function of the temperature normalized bias eV_B/k_BT and show a power law dependence for $eV_B > k_BT$ that is fitted to extract the power (red).

Figure 10 shows the conductance (numerical derivative) as a function of bias voltage with a clear dip in conductance around zero-bias. To isolate this feature from the transistor behaviour observed in Fig. 9, each conductance trace G is normalized by the corresponding 293 K curve $G_{293\,\mathrm{K}}$ – at this temperature the zero-bias feature is washed out from thermal broadening and only the transistor behaviour remains. Figure 10a shows the normalized conductance $G/G_{293\,\mathrm{K}}$ at 14 K as a function of bias voltage V_B at different gate voltages from -0.25 to 2 V. With increasing gate voltage the zero bias feature becomes less pronounced. A similar effect can be observed for increasing temperature in Fig. 10b, where $G/G_{293\,\mathrm{K}}$ is shown at $V_G = 0$ as a function of bias voltage V_B and temperatures from 14 K to 293 K. This behaviour

could be related to potential variations along the nanowire, that suppress conductance at low electron energies and therefore become increasingly averaged out for a broadening electron energy distribution from an increasing bias voltage or temperature [85, 86]. The effect of an increasing gate voltage could also be explained in this framework, since higher electron energies would lead to less pronounced zero-bias features from potential fluctuations. More insight can be gained from the temperature scaling of the conductance in the next section.

In the remainder of this section I will discuss another possible explanation for zero-bias features in the framework of a Luttinger liquid. In previous work on 1D systems, zero-bias features and a power-law dependence of the conductance on the bias voltage have been interpreted as signatures for clean Luttinger liquids [74, 73, 87]. Our devices cannot support a clean Luttinger liquid because transport is not ballistic due to the high doping density (see Sec. 3.3). Nevertheless we find features that are very similar to the signatures that were related to transport in the Luttinger liquid regime. This includes the power-law increase of the conductance as a function of bias voltage according to Eq. 13 as shown for the 8 nm nanowire device in Fig. 11. Each subfigure shows multiple data sets taken at temperatures from 14 K to 293 K as a function of bias voltage. For every temperature in each subfigure, the $G/G_{293\,\mathrm{K}}$ curves were divided by the value at zero-bias. After scaling, the data was plotted as a function of the temperature renormalized bias voltage $eV_\mathrm{B}/k_\mathrm{B}T$, such that all bias traces start at the same point. A linear behaviour on the double logarithmic scale then indicates possible power law behaviour as a function of bias voltage for all data sets at all temperatures. Indeed the data scales universally with the temperature renormalized bias for every gate voltage and shows two regimes: for $eV_\mathrm{B} < k_\mathrm{B}T$ the scaled conductance is constant and for $eV_\mathrm{B} \gg k_\mathrm{B}T$ the scaled conductance increases in a power-law (red fits in Fig. 11).

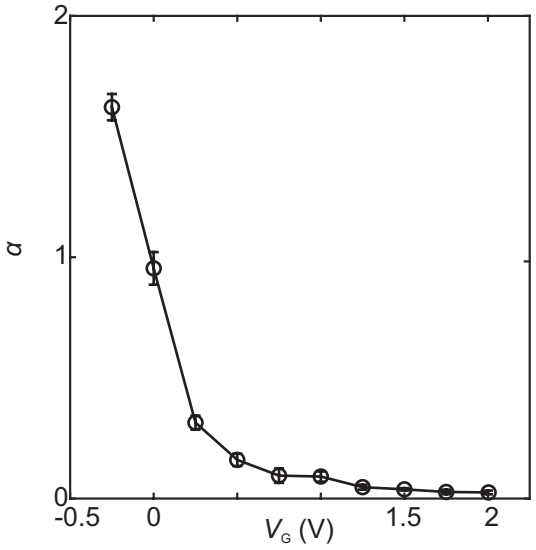

Figure 12: Extracted powers α from Fig. 11 as a function of gate voltage V_G.

In the Luttinger liquid interpretation, the strength of the electron-electron interaction is indicated by the power α, that can be extracted from the linear fits in Fig. 11 and is shown in Fig. 12 as a function of gate voltage. The powers would then suggest decreasing interaction strength for increasing gate voltage as expected for an increasing number of parallel conducting channels in a multi-channel Luttinger liquid [73, 76, 77, 88].

The interpretation of these signatures as evidence for Luttinger liquids has been challenged before in e.g. Ref. [89] and Ref. [75], where the scaling was attributed to transport in the 1D diffusive regime or at the transition from Luttinger liquid to the diffusive regime. These interpretations are in line with our previous conclusion, that the zero-bias feature is related to conductance suppression at low electron energies due to potential fluctuations in the channel.

3.2.3 Temperature scaling

To identify the relevant transport model in the 8 nm nanowire, I will now present the analysis of data at zero gate voltage as a function of temperature and compare the behaviour to the theories discussed in Sec. 3.1. Since a clean Luttinger liquid can be excluded, the zero-bias features could be interpreted in the framework of strong localization, where thermal activation increases the conductance consistent with the behaviour in Fig. 10b. The conductance at zero-bias would then also increase with gate voltage as in Fig. 10a, because the Fermi-energy is increasing relative to the potential fluctuations. Furthermore, in a 1D system with only few potential fluctuations and strong electron-electron interactions, it is possible that an intermediate regime between Luttinger liquid and strong localization needs to be considered – this is the model described by Mishchenko *et al*. [77] (see Sec. 3.1). Finally I will consider a model that is based on WL as well as a model that considers WL and strong electron-electron interactions.

Figure 13 shows the conductance G at zero bias voltage and gate voltage as a function of temperature T. In an FET device, this data would follow the model of thermionic transport over a single potential barrier of height B with the conductance proportional to $T^2 \exp(-B/k_B T)$ [90] – this is clearly not the case in Fig. 13. Instead, the data was fitted to the hopping model from Eq. 10, that describes thermal activation over many barriers and can depend on dimensionality via the parameter n. The grey shaded area corresponds to the fits for n between 0.25 and 1 (0D to 3D bound), while the yellow line is the fit corresponding to $n = 0.5$ (1D case). We also fit the data with n as a free parameter (red) and find $n = 0.6 \pm 0.2$. Since the fit for $n = 0.6$ as well as the fit for $n = 0.5$ lie within the measurement error of the data points but only $n = 0.5$ corresponds to a physical theory, the fits indicate 1D hopping ($n = 0.5$) without a Coulomb gap or

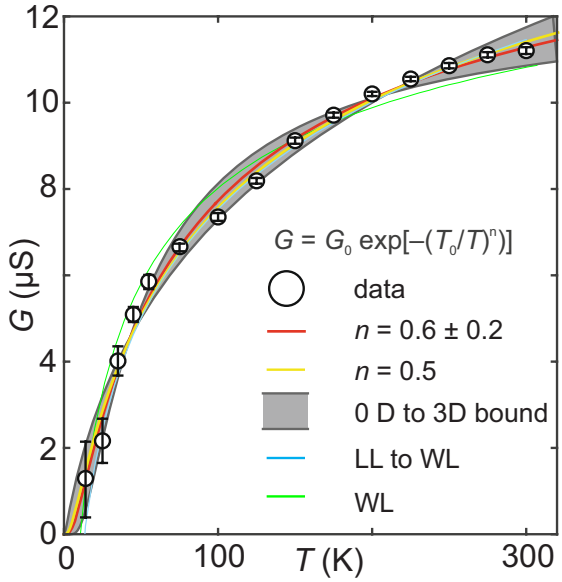

Figure 13: Conductance G at zero-bias and gate-voltage from Fig. 10b as a function of temperature T. The grey shaded area corresponds to the 0D and 3D boundaries of the nearest neighbour hopping model. The red line is the fit with n as a free parameter while the yellow line corresponds to a fit with fixed $n = 0.5$. The light blue line indicates the fit according to Mora *et al*.[76] in the transition from weak localization to LL and the green line is the fit according to WL in the diffusive regime.

hopping with a Coulomb gap in any number of dimensions. The fit for $n = 0.5$ produces $T_0 = 116 \pm 35\,\mathrm{K}$ which corresponds to a characteristic transport "activation energy" of $10 \pm 3\,\mathrm{meV}$. A sanity check for this parameter could be done at zero temperature where we would expect washing out of the strong localization features at similar energies when increasing the bias voltage. While we cannot measure at 0 K, a 12 mK measurement on a 8 nm nanowire in a later chapter (Sec. 3.3.3) shows a width in bias on the order of few mV to 10 mV – the extracted value for the fit parameter therefore seems reasonable.

The same functional form with $n = 0.5$ is predicted by the theory from Ref. [77] that includes the contributions from electron-electron interactions. The fit parameter $T^* = 101 \pm 31\,\mathrm{K}$ corresponds to 4.8 ± 2 parallel channels according to Eq.15 when assuming an effective mass $m^* = 0.19 m_\mathrm{e}$ and using the param-

eters $n_{1D} = 1.62 \times 10^6\,\mathrm{cm}^{-1}$ and $\tau = 11.4\,\mathrm{fs}$ from the measurements on similar devices in Sec. 2.1.2 [56]. The activated doping density is likely higher in our nanowire devices, such that the channel number is likely to be slightly overestimated. Nevertheless the extracted channel number agrees with the expected overall degeneracy of 4, that is originating in 2 degenerate spin states and 2 valleys. This is expected for a nanowire device, since the other 4 valley degeneracies from bulk silicon are lifted in a heavily confined system [81].

Next I consider the WL regime according to Eq. 4 with a correction term to the conductance $\propto l_\phi$. Assuming 1D Nyquist dephasing according to Eq. 9, the data is fitted to the form $A - BT^{-1/3}$ (green in Fig. 13) – this assumption is justified in Sec. 3.3.2. The fit does not lie within the range of the errors of the data points, such that the temperature scaling of the zero-bias conductance at this gate voltage does not agree with WL of this form. The light blue fit in Fig. 13 corresponds to the theory describing the transition from the Luttinger liquid to the WL regime. The model fits the data within the errors but requires 5 fit parameters such that the explanatory power is limited. While later data in Sec. 3.3.3 confirms that WL is relevant in these devices, the data suggests WL in the framework of UCF as opposed to the averaged contribution that is considered in this theory.

While the analysis in this section cannot unequivocally identify a transport regime, it confirms that the zero-bias feature is related to potential fluctuations in the nanowire channel and indicates 1D transport in the diffusive regime. The diffusive transport through our nanowire device can be modeled in the framework of strong localization as well as strong localization with strong electron-electron interactions. It is also possible that a regime with WL and strong electron-electron interactions is relevant in the devices, but the results are inconclusive in that regard. In case the potential fluctuations allow for tunneling as well

as thermally activated transport over many barriers, it is also possible that weak localization and strong localization are relevant at the same time [67]. This interpretation is supported by the data in Sec. 3.3.3, where I find conductance fluctuations from WL as well as zero-bias features that are most likely related to strong localization.

3.2.4 Conclusion

This section presented DC transport measurements on junctionless nanowire transistors with an activated Si:P doping density that is sufficient to screen incoming fields at the surface if charges can move in 3 dimensions. In a measurement at room temperature and high bias, nanowire transistors with diameters 16 nm and 24 nm can therefore not be pinched OFF with an electric field from a gate electrode. A nanowire transistor with 8 nm diameter, however, switches with a high ON/OFF ratio and a subtreshold slope close to the theoretical limit. This indicates suppression of 3D screening and suggests confinement of charges into 1D. The metallic behaviour in the larger devices can therefore be attributed to bulk-like screening of outside fields, while a significant suppression of 3D screening persists all the way up to room-temperature in the 8 nm device.

Next the conductance in the 8 nm nanowire is measured as a function of temperature, bias voltage and gate voltage showing the expected behaviour for an FET at high bias and high temperature. For lower temperatures down to 14 K and low bias voltages below 0.5 mV, the device shows a zero-bias dip in conductance which disappears with increasing temperature and gate voltage. We find a power law scaling of the conductance as a function of bias voltage, similar to other reports in 1D systems where such features have been associated with a Luttinger liquid in a ballistic channel. Since the channel is not ballistic in the

presented devices this interpretation is false. Our result therefore suggests that transport in the Luttinger liquid regime cannot be unequivocally identified using conductance scaling. In future devices, such a demonstration would require signatures from the separation of spin and charge excitation as shown in Ref. [91].

To identify the relevant transport model in our devices, we analyze the conductance at zero bias and zero gate voltage as a function of temperature. The strong localization transport model produces a fit within the errors of the data and a fit parameter that seems reasonable compared to a similar energy scale in the system. The same functional form is also predicted by a theory that includes strong electron-electron interactions and describes the transition between Luttinger liquid and strong localization regime. From this theory, we extract the number of contributing transport channels to be 4, which is consistent with a nanowire that has a spin and valley degeneracy of 2.

Finally the WL regime does not produce a fit within the errors of the data, but a theory describing the transition from Luttinger liquid to WL fits the data within the errors. While this fit does not have strong explanatory power due to many fit parameters and the theory does not consider the form of WL that was found in later data, WL with strong electron-electron interactions could be a relevant transport model especially at different gate-voltages and temperatures. Transport could also be affected by strong localization and WL at the same time in agreement with previous reports [67] and measurements in Sec. 3.3.3. Ultimately there is not sufficient evidence to support any claims about the significance of electron-electron interactions in this analysis. There is, however, evidence for diffusive 1D transport and the significance of 1D confinement for transistor operation. The results show that future 1D nanowire CMOS devices can be fabricated with much higher doping densities than bulk transistors and still maintain excellent subtreshold

slopes close to the theoretical limit. While the mobility in the transistor can be reduced from scattering at high doping densities, the transistor channel could also be shorter due to improved electrostatic control. Depending on the need for miniaturization and the required operation temperature this could be an advantage in future applications.

The measurements also contribute to the understanding of 1D transport in future top-down fabricated devices, where researchers will need to identify the correct transport regime for modelling and device design. In associated work Georgiev *et al*. [15] have therefore implemented 1D effects in their simulation environment based on the results presented in this chapter.

3.3 Quantum transport from 28 K to 12 mK

In the following section I will present my measurements on silicon nanowires with different Si:P doping concentrations, length 150 nm, diameter 8 nm and a wrap-around gate along the entire channel. I have measured the nanowires in liquid helium at 4 K and in a Triton 200 dilution refrigerator for temperature dependent measurements as well as measurements at the base temperature of 12 mK.

In this regime decoherence from thermal effects is suppressed, such that the coherence length can become larger than the distance between scattering sites or even exceed the geometrical constraints of the nanowire. I will study the emerging universal conductance fluctuations as a function of temperature to extract the relevant decoherence mechanisms and obtain the mean free path in two nanowires with different doping concentrations by analyzing the spacing of quantum interference features.

For large potential variations at low gate voltages the nanowire can break up into charge islands and transport is governed by sequential tunneling of single electrons onto/off the islands. The charge islands have discrete energy levels that correspond to the charge state according to the constant interaction model presented in Sec. 3.1.5. In one nanowire I will report on a single island that stretches along the entire nanowire channel and can be successively charged with over 500 electrons.

3.3.1 Coulomb blockade and gate coupling

In most of the devices that were studied in this thesis Coulomb blockade occurs in a small gate voltage region close to pinch-off at cryogenic temperatures. Transport in one device, however, is dominated by Coulomb blockade over a very large gate voltage region (> 6 V) with a periodicity that suggests a

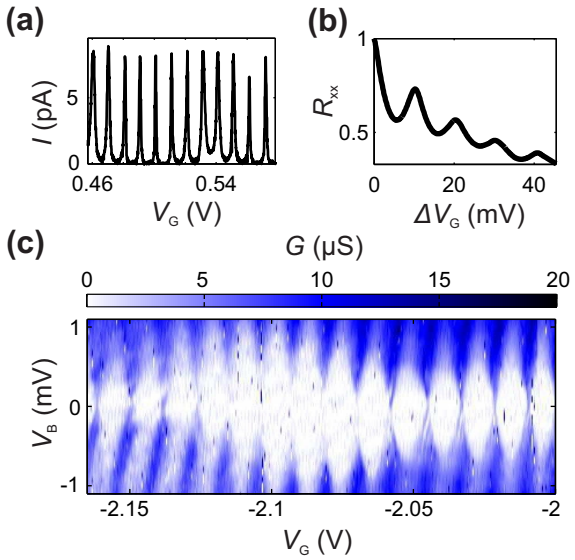

Figure 14: Device A (8 nm silicon nanowire device doped Si:P $2 \times 10^{20}\,\mathrm{cm}^{-3}$): a) Current I at 12 mK as a function of gate voltage V_G at a bias voltage of 0.1 mV. b) Autocorrelation function $\mathrm{R_{xx}}$ of the current in a gate voltage window from -4.5 V to +2 V. c) Conductance G as a function of gate voltage V_G and bias voltage V_B in the Coulomb-blockade regime.

single island along the entire channel length (L=150 nm). From the gate voltage spacing of the Coulomb blockade in this device, called device A, I will extract the capacitance between the channel and the gate for all 8 nm devices.

Fig. 14 presents data from device A with a nominal P doping density of $2 \times 10^{20}\,\mathrm{cm}^{-3}$ measured at 12 mK. When biased at 0.1 mV the current I through the device shows signatures of single electron transport with over 500 evenly spaced Coulomb peaks over a large gate voltage range from -4.5 V to +2 V. Figure 14a shows a fraction of this gate range while the entire data set is presented in the Appendix. Figure 14c shows the corresponding Coulomb diamonds in conductance G as a function of gate voltage V_G and bias voltage V_B. Note that the Coulomb diamonds do not show sharp corners especially at higher bias voltage. This indicates strong tunnel coupling to the leads and lifetime broadening in agreement

with the relatively high conductance up to $20\,\mu S$ (or $50\,k\Omega$) compared to e.g. the GaAs quantum dot presented in the next chapter ($\sim 6.7\,M\Omega$). In this regime there are typically strong co-tunneling effects which could explain the diagonal lines of enhanced conductance in the bottom left part of Fig. 14c or the finite conductance away from zero-bias in the Coulomb blocked regions. Since a detailed analysis of the co-tunneling effects is beyond the scope of this thesis, I want to refer the interested reader to Ref. [92] for more details.

The spacing of the Coulomb peaks is characterized in Fig. 14b using the autocorrelation function of the current as a function of gate voltage:

$$R_{xx} = \int I(V_G) I(V_G - \Delta V_G) dV_G \tag{20}$$

The autocorrelation was calculated using the entire gate-voltage range of the measurement with over 500 Coulomb peaks and shows clear oscillations corresponding to a Coulomb peak spacing of $\Delta V_G = 10 \pm 1\,mV$. The highly regular spacing of the Coulomb peaks indicates that there is a fixed capacitance between charge island and gate. Consequently the size of the island along the nanowire is fixed in the investigated gate voltage range. The capacitance from the gate to the channel can then be calculated via [79]:

$$C_G = e/\Delta V_G = 16 \pm 2\,aF \tag{21}$$

The island length can be inferred by comparing the capacitance extracted from ΔV_G to a theoretical value that follows from a simple cylindrical capacitor model:

$$C_G = \frac{2\pi\varepsilon_r\varepsilon_0}{\ln(b/a)}L \tag{22}$$

Here ε_0 is the vacuum permitivity and $\varepsilon_r = 3.9$ is the relative permitivity of the oxide. The geometry is taken from Transmission and Scanning Electron Microscope images [56]. The Transmission Electron Microscopy studies were carried out by Donald MacLaren at the University of Glasgow, where the nanowire cross section was imaged in Electron Energy Loss Spectroscopy as shown in Fig. 8 (a line cut is shown in the Appendix). With this technique it is possible to distinguish the materials in the device due to the characteristic energy loss of the detected electrons from different points of the cross section. We extract the radius of the nanowire a=4 nm, the distance to the gate b=31 nm and the length of the nanowire L=150 nm such that we can calculate the gate capacitance as 15.8 aF.

The close agreement between the experimental and theoretical values for the total capacitance indicate that the charge island stretches along most of the nanowire channel with tunnel barriers on both ends. Possible reasons for the formation of tunnel barriers at the ends of the channel are strain [28] and/or the accumulation of impurities. Since no other device on the same chip or on any other chips shows a similar behaviour, the tunnel barriers are formed in a process that is specific to the device and therefore most likely related to a local effect in an area on the order of 100 μm^2. Given that the chip was cleaned in an asher with lower cleanliness standards than other chips, the tunnel barriers might be related to local

impurities that have diffused into the channel in fabrication. Either way the device is not reproducible. Another device, called device B, which was measured to collect the data in Fig. 15, 16 and 17a+b, is geometrically identical with a 150 nm channel length and diameter 8 nm but doped to a lower nominal doping concentration of $4 \times 10^{19}\,\mathrm{cm}^{-3}$. The associated low temperature measurements do not show the regular Coulomb blockade pattern over a large gate range. Instead Coulomb blockade features can only be observed at low gate voltages in a small window that is followed by a region of increased conductance. The highly irregular Coulomb peaks in the low gate voltage region correspond to Coulomb diamonds that strongly vary in size and often do not close completely (see Appendix). This is a signature of transport through one or more islands in the nanowire with varying sizes as a function of gate voltage. In contrast to device A, it is therefore likely that islands in other samples form as a result of potential variations along the channel and not solely due to effects on the ends of the nanowire.

3.3.2 Universal conductance fluctuations

In the previous section I have presented a device in which transport is dominated by Coulomb blockade in a large gate voltage window and there is no higher conductance regime. All other measured devices show such a higher conductance region without Coulomb blockade that corresponds to an opening channel. In this section I will present data from device B with diameter 8 nm and nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ at gate voltages outside of the Coulomb blockade regime.

The main panel in Fig. 15 presents the conductance G as a function of gate voltage at 4 out of 54 measured temperatures from 30 mK to 28 K (for the other temperatures see Appendix). The conductance fluctuates

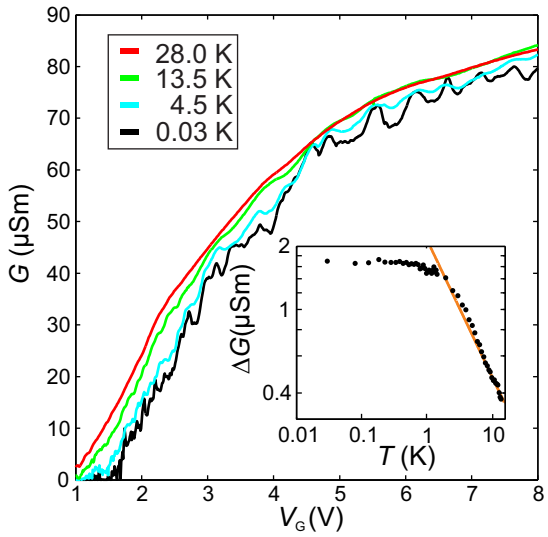

Figure 15: Main panel: Conductance G in device B as a function of gate voltage V_G at different temperatures. Inset: Root-mean square of the conductance traces as a function of temperature T after subtracting the background to determine the amplitude of the fluctuations in the temperature traces. The red fit corresponds to a power law $\Delta G \propto T^{-2/3}$ for $T > 1.9\,\mathrm{K}$.

as a function of gate voltage with decreasing amplitude for increasing temperature. This behaviour can be attributed to quantum interference in the framework of UCF as described in Sec. 3.1.3.

The inset of Fig. 15 shows the root-mean-square of the conductance ΔG calculated from the gate voltage traces as a function of temperature T. Since ΔG is meant to be a measure of the conductance fluctuation amplitude, not the larger scale conductance increase with gate voltage, a 2$^{\mathrm{nd}}$ order polynomial fit was subtracted from each trace before the root-mean-square was calculated. This fit was carefully chosen to capture the conductance increase on a large gate voltage scale but not the small scale fluctuations (see Appendix).

ΔG displays a low temperature regime below 1.9 K, where the fluctuation amplitude is constant, and a higher temperature regime, where ΔG decreases in a power law. Considering the theory presented

in Sec. 3.1.3, the temperature region with constant ΔG below 1.9 K corresponds to a regime without averaging from multiple independently fluctuating sections of the channel and a coherence length that is larger than the channel length $l_\phi > L$ [21]. In this temperature regime thermal broadening of the charge carrier energy distribution is not significant, indicating that the width of the WL resonance in the energy spectrum is larger than thermal broadening.

At $T > 1.9$ K the transport regime is characterized by fitting ΔG with a power-law (red in Fig. 14), which produces a power of -0.67 ± 0.04. As discussed in Sec. 3.1.3, the strong electron-electron interactions in a highly doped 1D system and the lack of phonon scattering at cold temperatures suggest dephasing from 1D Nyquist electron-electron scattering. Assuming this dephasing mechanism and $l_\phi < L$, the extracted power from the fit is in excellent agreement with the predictions in the regime $l_\phi >> l_T$. 1D Nyquist dephasing is therefore likely to be the dominant dephasing mechanism, which is consistent with the interpretation of the constant ΔG regime, since the coherence length is transitioning from $l_\phi > L$ to $l_\phi < L$ with increasing temperature. Furthermore, this result adds to the evidence for 1D transport from the previous chapter.

3.3.3 Mean free path

In this section I will present a study of quantum interference at the base temperature of the dilution refrigerator (12 mK). From this data I can extract the average distance between two scattering sites that localize a charge carrier in 1D quantum interference. This length is also the mean free path l_e that an electron travels on average before it gets scattered. The coupling from the channel to the gate, that was determined in Sec. 3.3.1, is required to extract l_e from a measurement as a function of gate voltage fol-

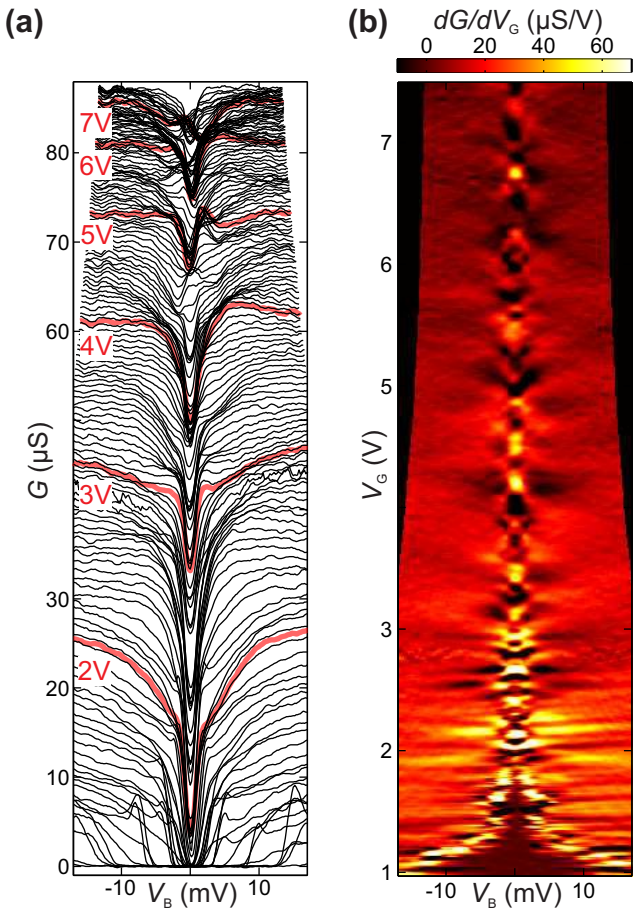

Figure 16: Device B (length 150 nm, diameter 8 nm and nominal doping concentration Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$): a) Conductance traces G as a function of bias V_B at gate voltages from 0.97 V to 7.5 V. The red lines indicate the traces at 2, 3, 4, 5, 6, and 7 V gate voltage. b) Transconductance dG/dV_G as a function of bias voltage V_B and gate voltage V_G in the same device.

lowing Ref. [93].

Figure 16a shows the conductance G as a function of bias voltage V_B in device B from Sec. 3.3.2 for gate voltages from 0.97 V to 7.5 V. Since the conductance increases with the gate voltage, the traces are separated without an additional offset. The red lines mark the traces at 2, 3, 4, 5, 6 and 7 V in gate voltage for better orientation. WL in Fig. 16a manifests in regions that appear darker because the conductance

changes only very little in a certain gate range and the lines are closer together. These regions, where the conductance is forming a plateau as a function of gate voltage, are most visible at zero-bias but some features are visibly extending into higher biases. The features at zero bias are attributed to resonances in the energy spectrum of the device due to quantum interference and the features away from zero bias correspond to the point where these resonances enter the bias window [94]. The resulting diamond-shaped pattern is most pronounced between 5 and 6 V as well as 6 and 7 V in gate voltage, but can be difficult to identify when several quantum interference paths have similar lengths and therefore produce features in the same energy window. All conductance traces show a dip centered around zero bias that has been investigated in Sec. 3.2.2 and is likely related to strong localization. The low temperature data therefore agrees with the temperature scaling in Sec. 3.2.3, where strong localization and WL were identified as possible dominant processes in transport.

Figure 16b shows the numerically derived transconductance dG/dV_{G} as a function of gate voltage V_{G} and bias voltage V_{B} from the data in Fig. 16a. For lower gate voltages ($V_{\mathrm{G}} \lesssim 2$ V) there are Coulomb-blockade features that correspond to multiple charge islands in series (see Appendix). At higher gate voltages, when the overall conductance increases (see Fig. 16a), quantum interference results in diamond shaped patterns as a function gate and bias voltage. The position and size of those features agree with the representation of the data in Fig. 16a but not all features can be clearly seen in both figures.

The sizes and distances between the features in Fig. 16b correspond to characteristic energy spacings that are associated to the the microscopic origin of the quantum interference and the mean free path. In Fig. 17 these energy spacings of the conductance fluctuations are analyzed in two different devices with length 150 nm and diameter 8 nm: device B that was presented previously in Fig. 15 and 16 with nominal doping

density Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ as well as device C with a higher nominal doping density Si:P $2 \times 10^{20}\,\mathrm{cm}^{-3}$. Figure 17a shows the transconductance dG/dV_G as a function of gate voltage V_G and bias voltage V_B for device B at 12 mK while Fig. 17b shows the transconductance for device C at 4 K. Both data sets show fluctuations in the transconductance, that correspond to quantum interference because the gate voltage range is chosen outside of the Coulomb blockade regime. Given that these features are clearly visible $l_\phi > l_\mathrm{e}$ in both devices.

Figure 17c,d show the Fourier transform of the 2D autocorrelation function of both data sets, that can be used to find the dominant voltage spacings between the fluctuations [95]. The Fourier transform for device B is plotted in Fig. 17c and shows four symmetric hotspots (circled in white) corresponding to a gate voltage spacing $\Delta V_\mathrm{G} = 0.6 \pm 0.1\,\mathrm{V}$ and bias voltage spacing $\Delta V_\mathrm{B} = 20 \pm 14\,\mathrm{mV}$. For device C the same analysis in Fig. 17d shows hotspots with $\Delta V_\mathrm{G} = 1.5 \pm 0.3\,\mathrm{V}$ and $\Delta V_\mathrm{B} = 70 \pm 40\,\mathrm{mV}$. For both devices the spacing on the bias voltage axis is close to or larger than the bias voltage range in the respective measurements in Fig. 17a,b. The position of the hotspots in that dimension is therefore an artefact from the Fourier transform and not analyzed further.

From a simple model based on a particle in a box Biercuk *et al*. [93] have derived the following expression to convert fluctuations on the gate voltage axis to the characteristic length scale of the quantum interference:

$$l_\mathrm{e} = \frac{4e}{c_\mathrm{G} \Delta V_\mathrm{G}} \tag{23}$$

Here e is the electron charge, ΔV_G is the distance in gate voltage between two features and c_G is the capacitance to the gate per unit length. The capacitance per unit length $c_\mathrm{G} = (1.1 \pm 0.2) \times 10^{-10} F/m$

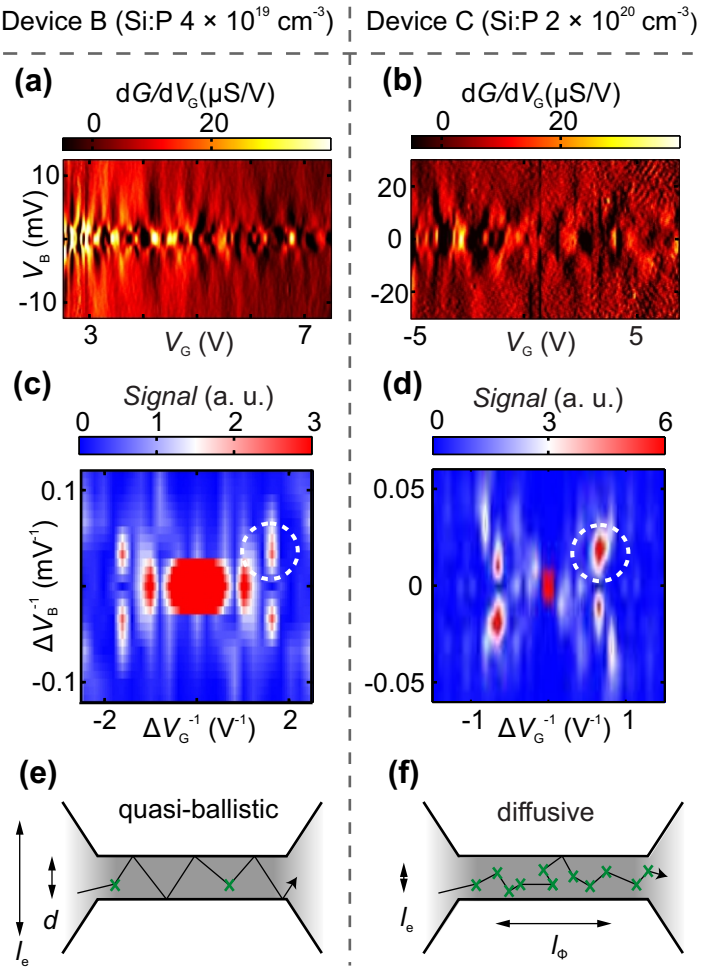

Figure 17: Data from device B with diameter 8 nm and nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ at 12 mK:
a) Transconductance dG/dV_G as a function of gate voltage V_G and bias voltage V_B, c) Fourier transform of the autocorrelation from a) with one of four symmetric hotspot circled in white. e) Illustration of transport in the quasi ballistic regime.
Data from device C with diameter 8 nm and nominal doping Si:P $2 \times 10^{20}\,\mathrm{cm}^{-3}$ at 4 K:
b) Transconductance dG/dV_G as a function of gate voltage V_G and bias voltage V_B, d) Fourier transform of the autocorrelation from c) with one of four hotspots circled in white. f) Illustration of transport in the diffusive regime.

can be taken from the analysis of Fig. 14 where the capacitive coupling to the entire channel of the geometrically identical device A was determined. Following Eq. 23, the dominant gate voltage spacing can be converted to $l_\mathrm{e} = 10 \pm 2\,\mathrm{nm}$ in device B and to $l_\mathrm{e} = 4 \pm 2\,\mathrm{nm}$ in device C.

Based on the extracted l_e, the characteristic transport length scales in device C compare as $l_e < d < L$ as well as $l_\Phi > l_e$. An illustration of a classical transport path in this regime, without taking into account 1D confinement or other quantum effects, is shown in Fig. 17f where the scattering events are marked in green. The majority of scattering events in this regime occur in the channel rather than on the boundaries. In the previous samples, presented in Sec. 2.1.2, the scattering in the channel was associated to unactivated dopants [56]. Assuming that this is also the dominant scattering mechanism in device C, the extracted l_e suggests an unactivated dopant concentration of $(1.5 \pm 0.8) \times 10^{19}\,\mathrm{cm}^{-3}$.

In device B the analysis adds to the results from Sec. 3.3.2 and suggests $d \lesssim l_e < L < l_\phi$. The mean free path is larger than the diameter, such that scattering on the nanowire boundaries is likely to occur. The mean free path is therefore affected by the boundaries and we can only estimate an upper limit for the concentration of unactivated dopants at $(1.0 \pm 0.2) \times 10^{18}\,\mathrm{cm}^{-3}$. The corresponding illustration of a classical transport path in this "quasi-ballistic" regime is shown in Fig. 17e. Since charge carrier waves are not very likely to be scattered when travelling between the radial boundaries of the nanowire, device B supports the formation of transversal quantum interference modes in the radial direction (also called subbands). Given that the mean-free path is only slightly larger than the diameter, however, other scattering is also important and there are additional fluctuations in conductance on top of the ballistic 1D signatures presented in Sec. 3.1.2.

In principle it is possible to gain more insight with respect to coherence length and the origin of the conductance fluctuations from measurements as a function of magnetic field. This has been done in e.g. 50 nm InAs nanowires, where big magnetic fields up to 50 T were used [96]. In the studied samples, this type of measurement would far exceed the capabilities of the vector magnet available in the Triton

200 (up to 6 T).

3.3.4 Conclusion

This section presented low temperature transport data from three highly Si:P doped silicon nanowires with diameter 8 nm, length 150 nm and a wrapped around gate. One nanowire (device A) shows highly periodic Coulomb blockade over a large gate range, that can be attributed to confinement into the channel along the length of the nanowire. Since one charge is added per gate voltage spacing between Coulomb peaks, the device can be used to extract the coupling from the gate to the channel in all of the presented 8 nm nanowire devices.

In a second device (device B) with nominal doping Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ and without dominant tunnel barriers at the ends of the channel, universal conductance fluctuations are measured as a function of temperature. The analysis yields two regimes for the coherence length, that is longer than the channel length ($l_\phi > L$) for temperatures below 1.9 K and shorter than the channel length ($l_\phi < L$) for temperatures above 1.9 K. Additionally the measurement suggests dominant dephasing from electron-electron interactions according to 1D Nyquist-dephasing.

A low temperature measurement of device B at 12 mK shows the zero-bias feature that was attributed to strong localization in Sec. 3.2 as well as oscillations due to quantum interference as a function of gate voltage and bias voltage. This suggests that WL and strong localization are relevant at the same time. The potential fluctuations must therefore allow for strong localization from potential barriers with limited transparency for low energy electrons at low bias, while simultaneously allow for coherent partial scattering in WL.

To find the length of the scattering paths we analyze the periodicity in the WL regime using a Fourier transform. In that way the dominant voltage spacing in gate voltage is extracted in device B, with nominal doping $4 \times 10^{19}\,\mathrm{cm}^{-3}$, as well as in a third device C with nominal doping $2 \times 10^{20}\,\mathrm{cm}^{-3}$. After converting the voltage spacings to a characteristic length scale, the data from the higher doped sample suggests an elastic mean free path of 4 ± 2 nm while the elastic mean free path in device B is $10 \pm 2\,\mathrm{nm}$. The fact that the mean free path increases for lower doping density agrees with previous work, where the dominant scattering mechanism was determined to be neutral impurity scattering [56].

In device C, the elastic mean free path suggests a majority of scattering events occuring in the bulk of the channel, while the elastic mean free path in device C allows for the formation of subbands as described in Sec. 3.1.2. We have therefore demonstrated transport in the "quasi-ballistic" regime where $d \lesssim l_\mathrm{e} < L$ for the first time in top-down fabricated silicon nanowires. The samples therefore represent an important step towards high performance CMOS nanowire transistors and could lead to low temperature ballistic transistors with shorter channel lengths and smaller doping densities. At room temperature, similar transistors will not be ballistic, but could still exhibit improved energy efficiency and therefore be beneficial in any technologies that require low heating or power consumption – for example processors for mobile devices. Additionally, the low temperature operation could enable efficient control electronics for quantum information architectures that require cryogenic temperatures [20, 19]. Finally, the samples could provide a starting point for the development of silicon nanowire based quantum electronic devices such as charge pumps or charge sensors [37].

4 Charge and capacitance sensing

This section introduces a read-out technique for quantum devices called “Radio-Frequency reflectometry”. In reflectometry one measures the reflected radio-frequency signal from a device in a resonant circuit that is a function of inductance, capacitance and conductance of the device.

After introducing the theoretical concepts and limitations of the technique, I will present two ways of improving the sensitivity of the read-out followed by an RF measurement of a silicon nanowire. First I will present circuit simulations and measurements from a collaboration with Natalia Ares, where we show how impedance matching between the source and the resonant circuit can improve the sensitivity of our reflectometry circuit. While my main contribution to this collaboration is the simulation, I was also involved in measurement and data analysis. Next I will present an experiment with a superconducting SQUID amplifier in addition to the previously used amplifiers, that shows reduced noise levels for low input powers and can be beneficial if the input power is limited by measurement back-action. In this experiment I manage to reach unprecedented sensitivities in capacitance sensing that allow for single-shot read-out of singlet-triplet qubits.

Finally I present data from an RF measurement on a silicon nanowire where I achieve charge sensitivities similar to the best reported values from optimized devices. For the experiment with the SQUID amplifier and the experiment with the silicon nanowire I have rewired the dilution refrigerator to allow for an easy implementation of the SQUID amplifier in the puck (see Fig.3a) and have installed an additional line (port 3 in Fig 4) that allows for separate measurement of the amplification chain. I have also carried out the measurements and data analysis for both experiments.

4.1 Theoretical concepts

In this section I will discuss the measurement principle of RF reflectometry in more detail than in Sec. 2.3 and explain the limits of the technique. I will also introduce the SQUID amplifier that I have used in an experiment to improve the signal-to-noise ratio in a capacitance sensing experiment.

4.1.1 Reflectometry

In reflectometry one measures the reflected RF signal from a resonant circuit that consists of an inductor and the sample. The signal path is described in Sec. 2.3 together with the basic concept of the measurement. A signal can be described as a complex wave with a phase φ and an amplitude A such that the voltage can be written as:

$$V_{\text{RF-IN}} = Ae^{i(2\pi ft+\varphi)} \tag{24}$$

where f is the frequency of the signal and t is time. Analogous to optical systems, where reflections occur whenever the refractive index changes, an RF signal gets reflected when the impedance of an electric circuit changes. In most commercially available RF electronics the impedance is standardized at $Z_0 = 50\,\Omega$ to prevent reflections between components. To achieve minimal reflections everywhere but the tank circuit one can therefore use standardized components for wiring, attenuators, directional couplers etc. This sets the reference impedance in the reflectometry measurement, such that there is no reflection when the tank circuit has an impedance of $50\,\Omega$, i.e. “perfect impedance matching”.

Depending on the device and what contact is connected to the reflectometry circuit, its impedance has resistive, capacitive and inductive properties. The device is connected in series with a fixed inductor to form

a resonant tank circuit with frequency dependent reflections similar to an LC-resonator. The reflection coefficient Γ depends on the impedance of the tank circuit Z according to Eq. 1 and produces a reflected signal $V_{\text{RF-IN}}\Gamma$. Due to inductive and capacitive components in Z there can be a phase shift in the reflected signal such that Γ is complex. To measure the phase-shift $\Delta\varphi$ and the change in signal amplitude ΔA one therefore needs to compare the input signal to the reflected signal.

The sensitivity of the technique to a change in tank circuit impedance, and therefore device impedance, depends on the impedance matching to the measurement electronics. According to Eq. 1, if the matching is poor and Z_0 is negligible compared to the tank circuit impedance, the reflection does not change significantly in response to a small impedance change of the tank circuit. The change in reflected signal can therefore not be distinguished from the noise level in a reflectometry setup with a poorly matched tank circuit. Given that even a ballistic quantum device with one conductance channel has an impedance of $h/e^2 = 25.8\,\text{k}\Omega \gg 50\,\Omega$ and might change behaviour significantly as a function of device parameters, engineering a well matched tank circuit requires knowledge of the device impedance and careful design.

A simplified schematic of a reflectometry circuit attached to the source contact of a transistor device is shown in Fig. 4. In this simplified version of the circuit, the inductor and device form a resonant tank circuit with a frequency dependent impedance that is a function of device conductance, capacitance and inductance. In a real circuit the impedance of the tank circuit is also subject to stray capacitances, the self-inductance of the lines, the behaviour of the bondwires and other components in the circuit that are needed for e.g. a voltage bias. The device properties can be manipulated with a gate voltage V_{G} and a source-drain bias voltage V_{B}. To measure DC and RF in parallel, the RF is grounded over a capacitor while the DC component can be measured in a current measurement.

A three terminal transistor-type device can be measured either with an RF signal applied to the leads (source/drain) or with an RF signal on the gate. If the RF signal is reflected from the leads, Z has capacitive and resistive contributions, that are not always trivial to separate, and the reflection changes both amplitude and phase of the signal [50]. In addition there can be a contribution from the device inductance which is often negligible. In case the RF signal is applied to the gate and the tunnel rates to the charge island are comparable to the RF frequency or larger, a change in gate capacitance ΔV_{G} can be related to a phase-shift [44]:

$$\Delta\varphi \propto -Q\Delta C_{\mathrm{G}}/C_{\mathrm{P}} \tag{25}$$

where Q is the quality factor of the resonant circuit and C_{P} is a parasitic capacitance from the gate to the ground.

While DC techniques are only sensitive to the conductance of the device, RF-reflectometry can be used to detect changes in capacitance and inductance as well. Additionally there is no requirement for transport from one lead to the other, which enables detection of e.g. tunnel events between the quantum dots in a double quantum dot system or charging events of single impurities. Given sufficient sensitivity, RF-reflectometry therefore enables the detection of many kinds of tunnelling processes or capacitive effects in a device. On the other hand it is not always clear if a change in amplitude or phase is a capacitive, inductive or conductive effect and careful analysis is required to separate the three. For practical purposes, however, it is often irrelevant how exactly each effect is contributing since one is interested in e.g. detecting tunneling events rather than the implications for the impedance of the device.

4.1.2 Noise and sensitivity

Field or charge sensors based on DC devices are typically built from transistors with a sensitivity that is dominated by the noise in a dissipative channel – mainly thermal Johnson-Nyquist noise and flicker noise [21]. Thermal noise is associated with the random movement of charge carriers in an open channel, increases with temperature and contributes at all measurement frequencies. Flicker noise comes from e.g. charging events in the oxide and scales with the inverse of the frequency. The noise level can therefore be reduced by cooling the sample as well as measuring at higher frequencies where the $1/f$ flicker noise component becomes small. The radio-frequency resonance of a tank circuit with a transistor then acts as a bandpass filter for noise because the oscillation is only sensitive to noise close to the resonance frequency. The noise in an RF-FET is then limited by the low temperature Johnson-Nyquist noise, that is independent of the average current through the device [82]. In cold RF-SETs on the other hand, the dominant noise on the leads is shot noise which arises from tunnelling through the barriers at a random time [21, 82]. For the simplest case of two symmetrical tunnel barriers the shot noise power per bandwidth is [21]:

$$S_{\mathrm{N}} = 2e < I > \tag{26}$$

where e is the electron charge and $< I >$ is the average current. Since currents in SETs are typically very small, the associated shot noise is also small. In FETs, on the other hand, the Johnson-Nyquist noise does not depend on the overall current in the device and cannot be reduced by using smaller signals. The noise limit in conventional RF-FETs at cryogenic temperatures therefore compares disadvantageously to RF-SETs [82]. For RF reflectometry techniques on the gate of an SET, the randomness of tunneling

events also dominates the noise in the device, but couples into the RF-circuit in a different way. Since this thesis does not include the analysis of a reflectometry experiment on a gate contact, I want to refer the interested reader to Ref. [44] for more information about the associated "Sisyphus Noise".

Furthermore any device specific noise limit can only be reached if the noise from the device dominates over the noise that is produced in the read-out circuit. Typically this noise comes from the active components, such that low noise amplifiers are used in reflectometry circuits. Often these amplifiers are high electron mobility transistor (HEMT) amplifiers or bipolar junction transistor (BJT) amplifiers, that produce little noise at low temperatures but can still dominate the sensitivity of the circuit – especially when currents are low and shot noise is small [50]. In this thesis I will therefore introduce a reflectometry circuit with a SQUID amplifier that operates at lower noise levels than the BJT. This setup is particularly interesting in sensing experiments where measurement back action limits the input power to the device such that the resulting RF current and shot noise are small. In the context of amplifier noise, which is typically a form of Johnson-Nyquist noise and therefore does not depend on frequency, the noise power P_{N} is often converted to a noise temperature for better comparison to resistive components with temperature dependent noise:

$$T_{\mathrm{N}} = \frac{P_{\mathrm{N}}}{k_{\mathrm{B}}\Delta f} \tag{27}$$

where k_{B} is Boltzmann's constant and Δf is the resolution bandwidth of the measurement. The noise temperature of an amplifier refers to the noise level that it creates at the input rather than the output. This is convenient since it does not depend on amplifier gain.

To measure the charge sensitivity of a circuit, the charge on the gate of an SET is modulated with an

amplitude δQ and a frequency f_{M} around a point that corresponds to a flank of a Coulomb peak. The resulting modulation in device impedance is translated to an amplitude modulation in the reflected signal. When this signal is mixed in a spectrum analyzer, the frequency spectrum contains a peak from the input carrier frequency f_{C} as well as sidebands around the carrier frequency at $f_{\mathrm{C}} \pm f_{\mathrm{M}}$. The charge sensitivity is then calculated from the signal-to-noise ratio *SNR* of the sidebands according to [50, 6]:

$$S_{\mathrm{Q}} = \frac{1}{\sqrt{2}} \delta Q (\Delta f)^{-0.5} 10^{-SNR/20} \tag{28}$$

where the *SNR* is given in dB.

The same concept can be used to determine the sensitivity to conductance or capacitance, if it is possible to modulate those quantities independently of the other parameters in the circuit. For many devices it is not trivial to find a real control parameter that can be used to modulate the device capacitance only. In the presented experiments a variable capacitor is therefore introduced in parallel to the device. This capacitor can be modulated with a bias voltage to produce the same effect in the circuit as a purely capacitive change of the device impedance, assuming the dielectric losses in the capacitor are independent of the bias voltage.

In a measurement of the capacitance-, conductance or charge sensitivity using the sidebands arising from the modulation of a parameter X, the sensitivity is generally given by [58]:

$$S_X = \frac{\sqrt{2 T_{\mathrm{N}} k_{\mathrm{B}}}}{V_{\mathrm{IN}}^0 \left| \frac{d\Gamma}{dX} \right|} \propto \left| \frac{d\Gamma}{dX} \right|^{-1} \tag{29}$$

where V_{IN}^0 corresponds to the RF-voltage amplitude of the incident signal to the resonant circuit. The sensitivity can therefore be improved if $\left|\frac{d\Gamma}{dX}\right|$ is maximized. For example in a series *LRC* circuit where capacitance is modulated and the circuit is probed at the resonance angular frequency $\omega_0 = 1/\sqrt{LC_{\mathrm{G}}}$:

$$\left|\frac{d\Gamma}{dC_{\mathrm{G}}}\right| = \frac{2Z_0}{\omega_0 C_{\mathrm{G}}^2 R^2 (1+\frac{Z_0}{R})^2} = \frac{2Z_0\omega_0 Q_Z^2}{\left(1+\frac{Z_0}{R}\right)^2} \tag{30}$$

with $Q_{\mathrm{Z}} = 1/(RC_{\mathrm{G}}\omega_0)$ being the Q-factor of the circuit [97]. In this case the parameter R would correspond to a frequency independent dissipation due to e.g. line resistance and is likely on the order of Z_0 – the model neglects dissipation in the device via e.g. Sisyphus resistance. In case $R \approx Z_0$ the expression simplifies to $\left|\frac{d\Gamma}{dC_{\mathrm{G}}}\right| = 0.5LQ_{\mathrm{Z}}/C_{\mathrm{G}}$ indicating that the capacitance sensitivity benefits from a high Q-factor. To obtain the charge sensitivity one needs to multiply the derivative of the gate capacitance with respect to charge $\frac{dC_{\mathrm{G}}}{dq}$ that depends on the physics of the sample and will not be discussed in detail here – for a more detailed analysis see Ref. [44].

For the RF circuit attached to the source electrode in the simple model of a series *LCR* circuit at resonance, the circuit impedance changes via R such that:

$$\left|\frac{d\Gamma}{dR}\right| = \frac{2Z_0}{R^2(1+\frac{Z_0}{R})^2} \approx \frac{2Z_0}{R^2} \tag{31}$$

In contrast to Eq. 30, the parameter R is the resistance of the quantum device from source to drain and therefore larger than the resistance quantum – this implies $R \gg Z_0$ such that the approximation can be made in Eq. 31. To obtain the charge sensitivity there are again device dependent terms that need to be

multiplied.

A more elaborate model by Devoret and Schoelkopf includes the device behaviour of an RF SET with typical parameters and yields the shot noise limited charge sensitivity $2.7\mu e/\sqrt{\text{Hz}}$ [82]. The dependence on the SET and measurement parameters has been calculated by Korotkov and Paalanen [39] as a function of the charging energy E_c and the resistance from both tunnel barriers R_Σ. For a device with identical tunnel barriers at low temperature, zero source-drain voltage and optimal RF-power they find:

$$S_Q \propto R_\Sigma^{1/2} E_c^{-1} T^{1/2} \tag{32}$$

This proportionality is valid in the Coulomb blockade regime without co-tunnelling such that the tunnel barriers cannot be too transparent and the corresponding resistance is limited. While a high input power is beneficial for the signal-to-noise ratio and therefore the sensitivity, it is limited by the backaction of the RF signal – increased power is not beneficial when the capacitive coupling of the RF signal into the charge island causes broadening larger than the linewidth of a charge transition.

Until recently, the best reported charge sensitivity in a semiconductor RF-SET of $7.2\mu e/\sqrt{\text{Hz}}$ was achieved in a silicon quantum dot defined by multiple top-gates on a 2DEG [40]. There is also a recent preprint from 2018 by Ahmed *et al*. [41] that reports a charge sensitivity of $1.3\mu e/\sqrt{\text{Hz}}$ using a superconducting spiral inductor and gate-based charge sensing.

4.1.3 SQUID amplifiers

Amplifiers with low noise are crucial for reflectometry because they represent the active component in the circuit and therefore the dominant noise source next to the device. In sensing experiments with relatively strong signals there can be sufficiently high noise from the device, such that the noise from a semiconductor amplifier becomes insignificant for the sensitivity. In other applications, e.g. when signals and currents need to be small due to measurement back action, it is useful to consider lower noise amplifiers. There are a number of low noise superconducting amplifiers including Josephson parametric amplifiers [98, 99], travelling wave parametric amplifiers [100] and SQUID amplifiers [101]. All of these amplifiers use superconducting quantum interference devices (SQUIDs) and generate much lower noise powers than a semiconductor amplifier. However, only the SQUID amplifier has been demonstrated in the required frequency regime of few 100s of MHz to date [102].

A DC-SQUID consists of a superconducting ring that is broken at two points by Josephson junctions (JJ). An ideal JJ can carry a supercurrent up to the critical current I_c that depends on the difference in phase $\Delta\theta$ between the macroscopic superconducting wavefunctions in the superconductors on each side of the junction [103, 104]:

$$I_J = I_c \sin\Delta\theta \tag{33}$$

Any additional current causes dissipation across the junction. A more realistic representation of a real JJ, that also takes into account AC signals, is therefore given by an ideal JJ, that carries all the current up to I_J, in parallel to a capacitor and a resistor [105].

In a SQUID at non-zero magnetic field the maximal supercurrent is not simply $2I_J$ from both JJ, because

the flux through the SQUID loop Φ shifts the phase in the superconductors due to the Aharonov-Bohm effect [21]. When neglecting self-inductance in a SQUID with ideal JJs, the supercurrent can be approximated around the maximum supercurrent as [105]:

$$I = 2I_c \left| \cos\left(\frac{\Phi\pi}{\Phi_0}\right) \right| \tag{34}$$

where Φ_0 is the magnetic flux quantum. While the "current-phase relation" can be much more complicated in real SQUIDs, the concepts required in this thesis can be discussed in the framework of this approximation.

RF SQUID amplifiers exploit the current-phase relation to amplify an RF signal. For that purpose, the input signal V_{IN} is converted to a flux using a coil or stripline resonator. This flux is coupled into the SQUID and therefore alters the maximum supercurrent according to Eq. 34. The SQUID is current biased with a current I_{SQ} above the critical current ($> 2I_c$), which leads to a voltage drop across the SQUID that constitutes the output voltage of the amplifier V_{OUT}. In case $I_{SQ} > 2I_c$ there is a constant DC component in V_{OUT} that can be removed with a high pass filter.

The SQUID amplifier used in this thesis has a 20 turn input coil made from superconducting Nb with a length just below half of the wavelength of the input signal at the specified operation frequency of the amplifier (200 MHz). This superconducting resonator is processed on top of the SQUID and separated by a 400 nm SiO_2 layer. While this geometry ensures an inductive coupling $M \lesssim 1$, it also gives rise to a capacitive coupling from the SQUID to the input coil. Figure 18 shows a schematic of the SQUID amplifier with an input coil (green) where the capacitive coupling is indicated by a red dashed capacitor.

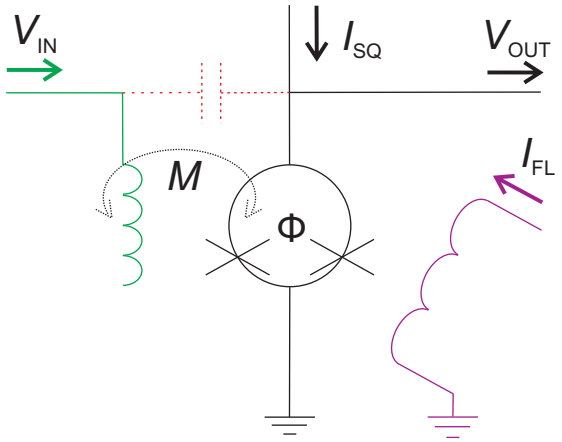

Figure 18: Schematic of the SQUID amplifier with input coil (green) made from a 20 turn Niobium superconducting resonator that is coupled to the SQUID with coupling M. The SQUID loop with two JJs (denoted by crosses) is biased with a current I_{SQ} and separated from the input coil with a 400 nm silicon oxide layer. The resulting capacitance from this geometry is indicated by a capacitor (red). An offset flux can be introduced to the SQUID with a current I_{FL} through a nearby coil (purple) to optimize gain and noise in the amplifier. The RF part of the voltage V_{OUT}, that drops over the SQUID when it is biased with a current above the critical current, constitutes the amplified RF output voltage of the SQUID.

A current I_{FL} through a flux bias coil (purple) can be used to induce a flux-offset into the SQUID and optimize the amplifier performance. The output voltage is given by the flux-voltage transfer function $V_{OUT}(\Phi)$ that follows from the SQUID impedance, I_{SQ} and Eq. 34. Given a SQUID impedance that is mostly resistive V_{OUT} roughly follows a cosine function in the approximation of Eq. 34. For the non-ideal case there can be two slightly different JJs that do not follow Eq. 33, thermal and capacitive effects as well as self-inductance, such that a simple cosine is not sufficient.

The dominant noise in SQUID amplifiers is related to the resistive transport through the JJs and can be described as thermal Johnson-Nyquist noise. A coarse estimate of the noise temperature can be made by assuming that all the noise is produced at the output of the amplifier [106, 101]. Since the noise temperature refers to the noise at the amplifier input, it can be calculated by dividing the constant Johnson-Nyquist

noise at the output by the gain. In that way the noise temperature is proportional to the inverse of the gain, which describes the noise as a function of I_{SQ} and I_{FL} relatively well in a large fraction of the parameter space. At high gains of the amplifier, however, currents in the SQUID cause additional noise that does not result in a noise temperature contribution inversely proportional to the gain [101].

4.2 Radio frequency read-out for charge and capacitance

As discussed in Sec. 4.1.2, the signal-to-noise ratio and therefore the sensitivity of an RF-reflectometry measurement is affected by impedance mismatches in the circuit. If reflections in the lines are avoided by using standardized 50 Ω components, the only impedance mismatch can appear at the tank circuit. In this section I will present a tank circuit with tunable components, such that the tank circuit impedance can be tuned through 50 Ω and the sensitivity can be measured as a function of impedance matching.
With optimized impedance matching between tank circuit and lines, the sensitivity is fundamentally limited by device noise – e.g. shot noise in SET charge sensors. However, this limit cannot be reached if the amplifiers dominate the noise in the circuit. I will therefore present measurements with a low-noise amplifier based on a SQUID that can be used to improve the noise level in the RF circuit.
The final section of this chapter covers an experiment where I have combined the single electron transistor in the silicon nanowire device from Sec. 3.3.1 with RF reflectometry to create an RF charge sensor.

4.2.1 Matching circuit and simulation

Ideally all parts of the reflectometry circuit down to the tank circuit have an impedance of 50 Ω to avoid undesired reflections in addition to the reflections from the tank circuit. In this section I will show that the sensitivity of the circuit can be improved when the tank circuit also has an impedance close to 50 Ω, such that the change in reflected signal due to changes in the sample impedance is maximized following Eq. 1. This corresponds to the point of maximal coupling between the input signal and the resonating tank circuit.

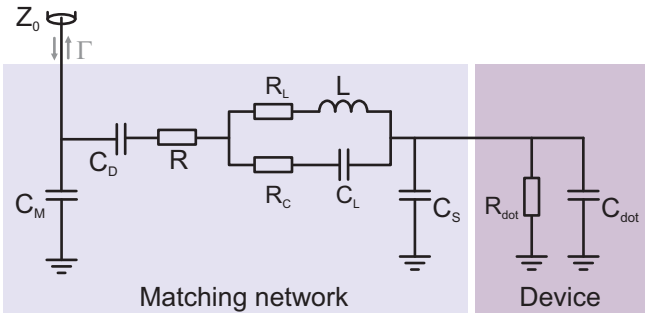

Figure 19: Circuit in the simulation where C_M and C_S were varied. The replacement circuit for the inductor was taken from the manufacturer with $R_\mathrm{L} = 3.15 \times 10^{-4}\,\Omega \times \sqrt{f_\mathrm{C}\,[\mathrm{Hz}]}$, $C_\mathrm{L} = 0.082\,\mathrm{pF}$ and $R_\mathrm{C} = 25\,\Omega$. The other parameters are $C_\mathrm{D} = 87\,\mathrm{pF}$, $L = 223\,\mathrm{nH}$, $R_\mathrm{dot} = 1\,\mathrm{G}\Omega$ and $C_\mathrm{dot} = 1\,\mathrm{aF}$. [50]

To match the impedance of the tank circuit to $50\,\Omega$ its components need to be chosen accordingly. While the parameters of these components can be calculated precisely in theory, there are some uncertainties that cannot always be accounted for in a real system. One source of impedance variability is the sample itself that likely changes impedance drastically depending on parameters like gate-voltages, bias-voltages and temperature. Additionally the tank circuit is likely to contain stray capacitances from e.g. bond wires that cannot necessarily be taken into account precisely when designing the experiment. For that reason I will present a tank circuit with variable capacitors that can be tuned to adjust the tank circuit impedance and thus compensate for impedance variability.

Figure 21 shows the measurement circuit with a GaAs gate-defined quantum dot device as a test object. As described in Sec. 2, the sample is mounted on a circuit board (pink rectangle) and measured in the dilution refrigerator. The reflected signal is measured either directly with a spectrum/vector-network analyzer or demodulated to produce a DC voltage V_S that is proportional to the amplitude of the reflected wave and a phase factor. In contrast to the simpler circuit from Fig. 4, the circuit board contains variable capacitors C_M and C_S (Macom MA46H204-1056) as well as several other mounted capacitors in addition

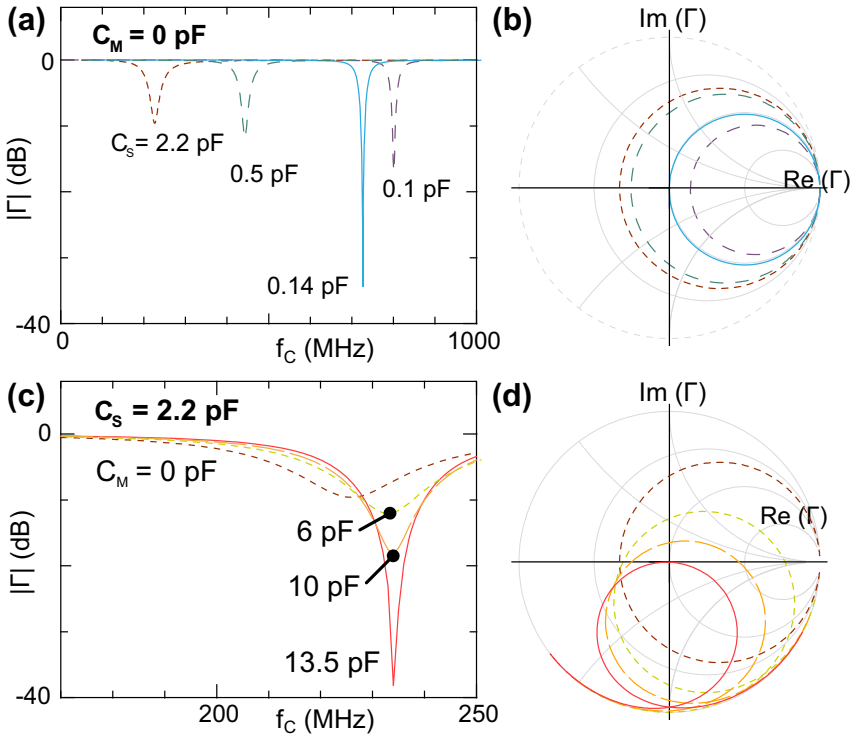

Figure 20: Simulations of the reflection coefficient Γ according to the circuit in Fig. 19 with $R = 20\,\Omega$. Simulations without matching capacitor ($C_M = 0$): a) $|\Gamma|$ as a function of frequency for different values of C_S. b) Smith chart for Γ corresponding to the simulation in a). Simulations with $C_S = 2.2\,\text{pF}$: c) Simulated $|\Gamma|$ for varying C_M. d) Smith chart from the simulations in c). [50]

to the inductor and bias voltage connection. The schematic in Fig. 21 also shows a resistor R that does not correspond to an individual component in the real circuit, but is used in modelling to represent dissipative processes and their effect on the impedance of the circuit. The impedance of the tank circuit can be tuned through the bias voltage across the device V_B, the gate-voltage V_L as well as the capacitances of the variable capacitors through the DC voltages V_M and V_S (see inset in Fig. 21). The reflectometry circuit is attached to one of the leads of the device and the DC current I can be measured in parallel to the RF measurement.

Before any measurements were carried-out, the reflection coefficient of the circuit was simulated for

an input signal from an RF source with $50\,\Omega$ impedance and a tank circuit with a highly resistive device represented by a 1 $G\Omega$ resistor in parallel to a negligible capacitance of 1 aF (the simulated circuit is shown in Fig. 19). The simulated circuit also contains a resistor R that does not correspond to a component in the real circuit and accounts for dissipative processes in the circuitry. Figure 20 shows the results of the simulations using $R = 20\,\Omega$ which was determined by fitting the resonances of the tank circuit in the experiment (see next section). The simulated reflection coefficient Γ is presented in two ways: the absolute value $|\Gamma|$ as a function of frequency and the full complex representation of Γ in a "Smith chart". A Smith chart is a representation on the complex plane with a scale that denotes the impedance of the tank circuit according to Eq. 1 assuming a line impedance $Z_0 = 50\,\Omega$ [97]. The frequency dependence cannot be observed in a Smith chart.

Figure 20a shows $|\Gamma|$ as a function of frequency at $C_M = 0$ for 4 different values of C_S. While the resonances are less pronounced in 3 traces (for $C_S = 2.2\,$pF, $0.5\,$pF and $0.1\,$pF), there is a one strong resonance at $0.14\,$pF. Figure 20b is the corresponding Smith chart showing Γ as the frequency is swept from 0 to 1 GHz. Perfect matching in this representation corresponds to zero reflection coefficient in the centre of the Smith chart and is only reached for $C_S = 0.14\,$pF (blue) as expected from Fig. 20a. In the real circuit, however, $C_S = 0.14\,$pF and $C_M = 0\,$pF cannot be reached due to a limited tuning range of the varactors.

Figure 20c shows the simulations of $|\Gamma|$ as a function of frequency at fixed $C_S = 2.2\,$pF while Fig. 20d shows the corresponding Γ in a Smith chart. Here perfect matching is reached at $C_M = 13.5\,$pF, which is within the tunable range of our circuit and larger than stray capacitances. The simulations therefore show how the circuit can be tuned into perfect matching using C_M and C_S even when there are parasitics that

were not accounted for in the design of the circuit.

4.2.2 Impedance matching in the experiment

At 12 mK the tuning range of the variable capacitors is lower than specified for higher temperatures by the manufacturer – most likely because less charge carriers are available without thermal activation. To increase the tunability and demonstrate the behaviour well out of matching as well as in perfect matching, the dilution refrigerator is heated to 1 K. Nevertheless the attempts to tune the tank circuit impedance through the capacitance C_M were unsuccessful with hardly any effect on the matching. On the other hand, the capacitance C_S of the varactor connected in parallel to the sample can be tuned to adjust the impedance matching.

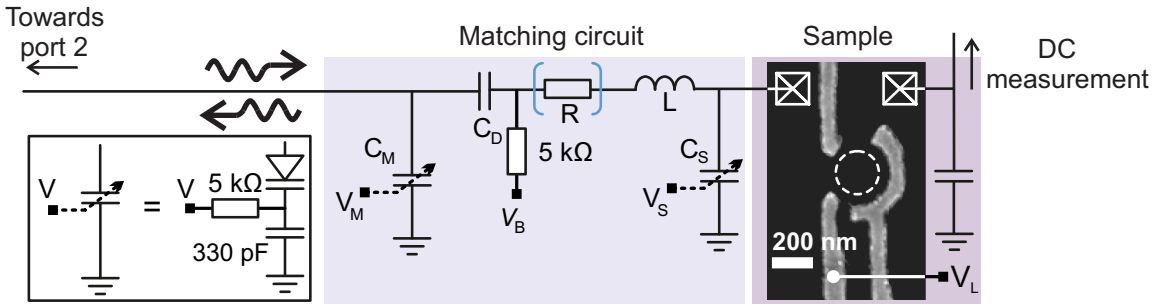

Figure 21: Experimental setup: A gate defined quantum dot on the surface of GaAs (electron micrograph right, with Ohmic contacts denoted by boxes) is coupled to an impedance-matching network formed from an inductor L (223 nH), variable capacitors C_S and C_M (tuned through the circuit in inset on the left) as well as a fixed capacitor C_D (87 pF). Parasitic losses in the circuit are parametrized by an effective resistance R, that is used in the simulation. The matching network is attached to the lines shown in Fig. 4 without the SQUID amplifier. A bias-T with a 5 kΩ resistor can be used to voltage bias the device with V_B. [50]

The symbols in Fig. 22a correspond to the amplitude of the measured reflection coefficient $|S_{21}| = A|\Gamma|$ from port 1 to port 2 in the experiment. The factor A accounts for constant attenuation and gain in the

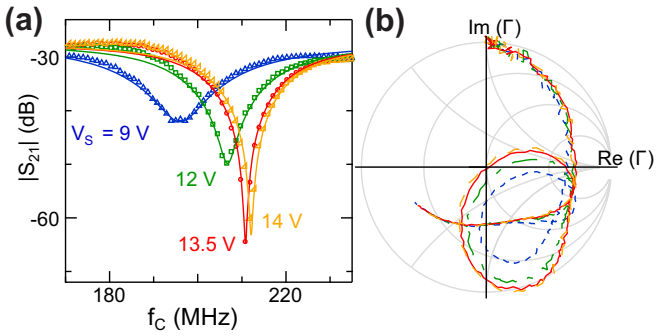

Figure 22: S_{21} parameter between port 1 and port 2 measured as a function of frequency for different V_S settings. The data are taken at a temperature of 1 K with $V_M = 0$. a) $|S_{21}|$ data points fitted with a circuit model (lines). b) Corresponding S_{21} plotted on a Smith chart with perfect matching achieved at $V_S = 13.5\,\mathrm{V}$. [50]

lines and therefore depends on the used attenuators, other losses as well as the gain of the low temperature amplifiers. As expected from the simulation in Fig. 20, tuning C_S affects the resonance frequency and the value of $|S_{21}|$ in resonance. The best matching is achieved at a frequency of 211 MHz for the curve that corresponds to a voltage $V_S = 13.5\,\mathrm{V}$ across the varactor. In the model from the previous section, that was fitted to the resonances as described in the next paragraph, this resonance frequency can be associated to a capacitance of $C_S = 2.78\,\mathrm{pF}$. Figure 22b shows the corresponding S_{21} on the complex plane in a Smith chart with the curve for $V_S = 13.5\,\mathrm{V}$ going through the origin and therefore indicating perfect matching.

The lines Fig. 22a correspond to a fit of the model from the last section to the data points. The good agreement was found by fitting the unknown circuit parameters R, C_S, C_M and A in a least square fit. This process required repeated simulation of the circuit in Fig. 19, where the ideal inductor was replaced with a more realistic effective circuit recommended by the manufacturer. The components of the replacement circuit as well as the other components in Fig. 19 are modeled according to the specifications from the respective manufactures as: $C_D = 87\,\mathrm{pF}$, $L = 223\,\mathrm{nH}$, $R_L = 3.15 \times 10^{-4}\,\Omega \times \sqrt{f_C}$, $R_C = 25\,\Omega$ and

$C_L = 0.082\,\text{pF}$. The sample was pinched off in the experiment such that it had a high resistivity and small capacitance compared to the rest of the circuit. It was confirmed that a variation of this high sample resistance does not affect the outcome of the simulation. Similarly a device capacitance that is much smaller than C_S is irrelevant such that the device parameters in the simulation can be arbitrarily chosen as $R_{dot} = 1\,\text{G}\Omega$ and $C_{dot} = 1\,\text{aF}$ without knowing the exact values.

For the resonance in perfect matching at $V_S = 13.5\,\text{V}$, the fit yields $A = -27.6 \pm 0.3$ dB and $C_M = 14.5 \pm 0.9\,\text{pF}$. While the value for C_M is in good agreement with the expected capacitance at zero bias voltage across the capacitor from the specifications of the manufacturer, the value for A is much smaller than expected. The expected value for A due to the attenuators, the directional coupler and the BJT amplifier without additional losses is $-19\,\text{dB}$ (BJT amplifier +32 dB, input line attenuation -31 dB, directional coupler -20 dB). The fit therefore indicates a loss of $-8.6\,\text{dB}$ in the lines or, alternatively, a smaller gain of the BJT amplifier than expected.

To obtain the circuit parameters for different matching conditions A and C_M were held constant and the resonances were fitted using the parameters C_S and R. The extracted values are shown in Fig. 23 as a function of V_S. For comparison Fig. 23 also shows the behaviour of C_S at room temperature according to the data sheet (assuming a parallel parasitic capacitance of $0.7\,\text{pF}$). The figure confirms, that the tunable range is significantly reduced at low temperatures.

4.2.3 Capacitance sensitivity

As mentioned earlier in Sec. 4.1.2, the used device can have a significant impact on the sensitivity in a sensing experiment. To demonstrate the improved sensitivity due to impedance matching independently

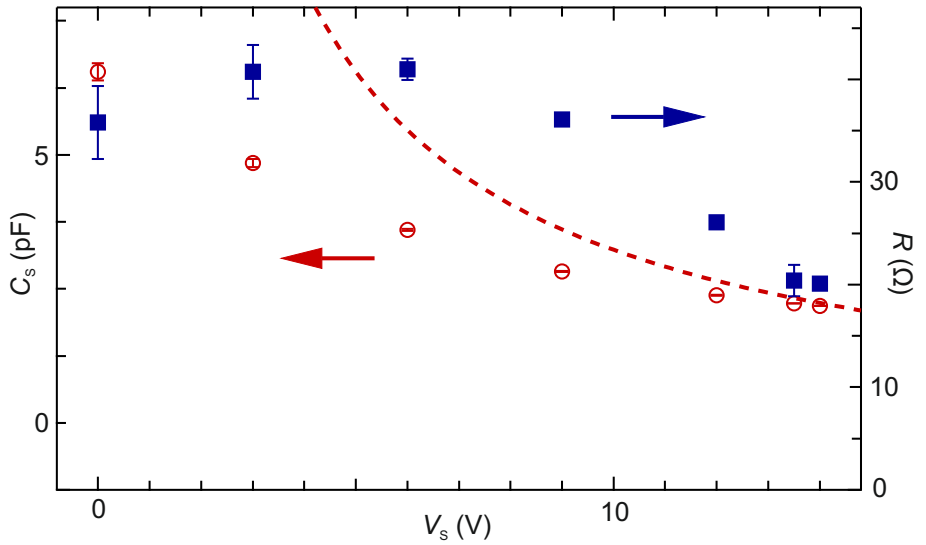

Figure 23: Fit parameters C_S (red) and R (blue) for the fits in Fig 22a as a function of V_S. The red dashed line shows C_S at room temperature according to the data sheet assuming a parallel parasitic capacitance of 0.7 pF. The error bars are calculated from the confidence bounds of the fits. [50]

of the measured device, I will therefore present measurements of the capacitance sensitivity using varactor capacitance modulation. Since the varactor is connected in parallel to the device, a modulation of the varactor capacitance is equivalent to a modulation of the device capacitance but can be done without changing the device inductance or conductance.

The capacitance sensitivity is measured using a sideband experiment similar to the measurement scheme for charge sensitivity presented in Sec. 2.3. Unlike in Sec. 2.3, however, the sidebands arise from an AC component to the voltage across the variable capacitor V_S with frequency f_M and root-mean square amplitude V_M.

The resulting capacitance modulation amplitude can be determined from the voltage modulation via $\delta C_S = \left|\frac{dC_S}{dV_S}\right| V_M$. Since the derivative cannot be measured directly, the calculation of δC_S requires a measurement of the derivative of the resonance frequency f_0 with respect to the varactor voltage $\left|\frac{df_0}{dV_S}\right|$ and a

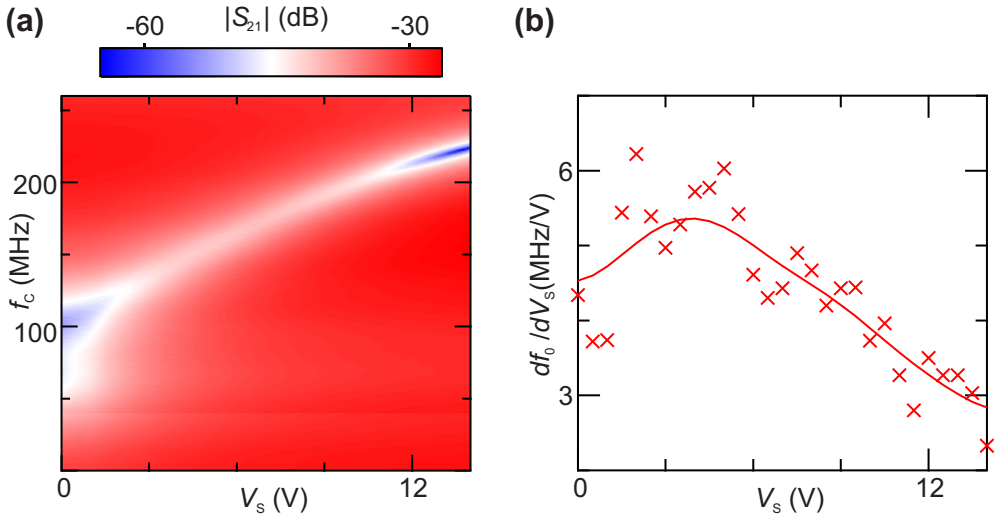

Figure 24: a) $|S_{21}|$ as a function of carrier frequency f_C and voltage across the variable capacitor V_S. b) Frequency f_0 at the minimum of every $|S_{21}|(f_C)$ trace derived with respect to V_S. The red line is the smoothed data used to determine $|\mathrm{d}f_0/\mathrm{d}V_S|$ in Eq. 36. [50]

local approximation of the resonance frequency as a function of capacitance given by an LC-circuit:

$$f_0 = \frac{1}{2\pi\sqrt{LC_S(V_S)}} \tag{35}$$

While the LC-circuit model is not sufficient for the prediction of the phase and amplitude of S_{21} or the exact resonance frequency in a large C_S range, comparison with the simulation and measured resonances confirms that it is a good local approximation for the resonance frequencies. Equation 35 can therefore be used to estimate the derivative $\left|\frac{\mathrm{d}C_S}{\mathrm{d}f_0}\right|$ around a frequency f_0 and the capacitance variation is:

$$\delta C_S = \left|\frac{\mathrm{d}C_S}{\mathrm{d}V_S}\right| V_M = \left|\frac{\mathrm{d}C_S}{\mathrm{d}f_0}\right| \left|\frac{\mathrm{d}f_0}{\mathrm{d}V_S}\right| V_M = \frac{V_M}{2\pi^2 L f_0^3} \left|\frac{\mathrm{d}f_0}{\mathrm{d}V_S}\right| \tag{36}$$

The factor $\left|\frac{df_0}{dV_S}\right|$ is obtained from a measurement of $|S_{21}|$ as a function of V_S and carrier frequency f_C that is shown in Fig. 24a. To obtain f_0 and $\left|\frac{df_0}{dV_S}\right|$, the resonance frequencies f_0 are extracted and numerically derived with respect to V_S. The result is plotted in Fig. 24b as a function of V_S together with the smoothed curve through the data points that can be used to obtain $\left|\frac{df_0}{dV_S}\right|$ for any V_S in the measurement range.

Knowing the relationship of δV_M and δC_S it is then possible to obtain the capacitance sensitivity in a

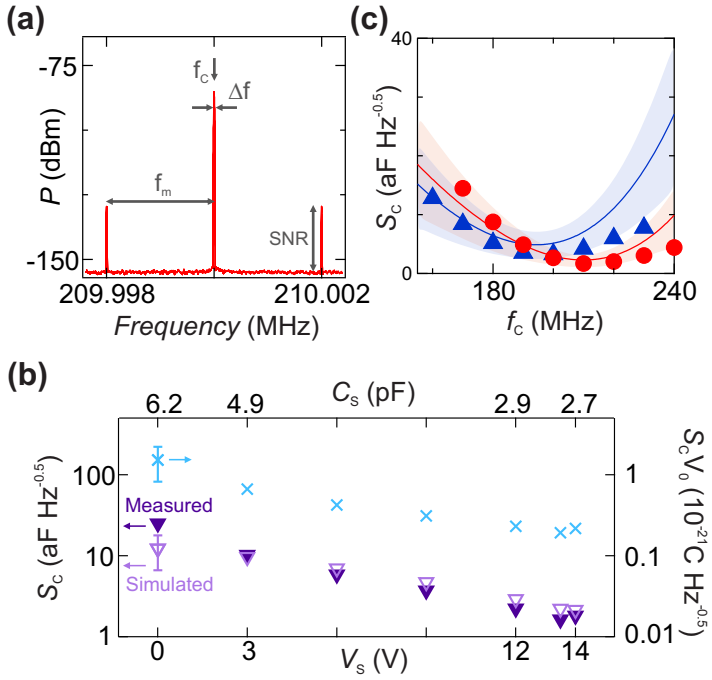

Figure 25: a) Power spectrum of the reflected signal near perfect matching (V_S = 13.5 V) with variable capacitor modulation $V_M = 2\,\mathrm{mV_{rms}}$ showing the carrier peak and modulation sidebands. The *SNR* and resolution bandwidth (Δf) are indicated. b) Capacitance sensitivity S_C (left axis) as a function of V_S (bottom) and the corresponding C_S (top) obtained from the simulation. The filled triangles indicate measured S_C while the empty triangles denote the corresponding simulated values. The crosses denote the figure of merit $S_C V_0$ (right axis) for the respective S_C. All data were measured using $\Delta f = 10\,\mathrm{Hz}$, $V_M = 2\,\mathrm{mV_{rms}}$ and $f_M = 1.75\,\mathrm{kHz}$. f_C was adjusted for best matching at every V_S. The error bars on the measured S_C data are smaller than the symbols. The error bars for $S_C V_0$ and simulated S_C (only marked for the first data point) reflect systematic uncertainty in the power delivered to the matching network. c) Symbols: Measured S_C as a function of f_C for $V_S = 13.5\,\mathrm{V}$ (circles) and $V_S = 9\,\mathrm{V}$ (triangles). Curves: Simulated S_C with shaded bands indicating systematic uncertainty in the simulation of the same origin as in b). [50]

sideband experiment similar to the charge sensitivity as discussed in Sec. 4.1.2. Figure 25a shows the reflected power as a function of frequency with the sidebands at $f_C \pm f_m$ next to the carrier frequency peak at f_C. Like the charge sensitivity, the capacitance sensitivity S_C can be extracted from the the height of the sidebands over the noise level (*SNR*) via [50, 107]:

$$S_C = \frac{1}{\sqrt{2}} \delta C_S (\Delta f)^{-0.5} 10^{-SNR/20} \tag{37}$$

where Δf is the bandwidth of the measurement.

Figure 25b shows the extracted sensitivity S_C as a function of V_S (dark purple triangles) using a modulation with $V_M = 2\,\mathrm{mV_{rms}}$ and $f_M = 1.75\,\mathrm{kHz}$ while adjusting f_C to the best matching point for every V_S. The input power $P_{IN} = -29\,\mathrm{dBm}$ was chosen below the threshold for Coulomb peak broadening in the device, such that later charge sensing experiments can be done at the same power. The error bars in the figure are smaller than the symbols and reflect the uncertainty in the calculation of δC_S from losses in the modulation signal. The y-axis on top of Fig. 25b shows the capacitance that is associated with the voltage V_S according to the simulation with the circuit parameters obtained in the previous section. The best sensitivity $S_C = 1.6\,\mathrm{aF\ Hz^{-0.5}}$ is measured for perfect matching at $V_S = 13.5\,\mathrm{V}$.

The figure also shows the simulated capacitance sensitivity (light purple triangles) for the C_S values that are associated with the measurement points. The errors in the simulated capacitance sensitivity, shown only for the first point, reflect uncertainties in the attenuation of the input line due to possible losses. While the behaviour of S_C as a function of V_S agrees well with the simulation for $C_S > 3\,\mathrm{V}$, the simulation deviates from the data at $C_S < 3\,\mathrm{V}$ due to a cable resonance at higher frequencies that lowers the effective

input power and increases S_C in the experiment.

To confirm that the best matching leads to the best sensitivity, Fig. 25c shows the sensitivity S_C as a function of carrier frequency f_C when the system is fixed at $V_S = 9\,\mathrm{V}$ (blue) and $V_S = 13.5\,\mathrm{V}$ (red). The experimental data is shown as points/triangles and the associated simulations are shown as lines in a shaded region that corresponds to the errors in the simulation given the uncertainties in the power delivered to the network. Although simulation and experiment only agree in a certain frequency range, they both show that the best sensitivity of the circuit can be achieved at perfect matching. The discrepancies as a function of frequency are due to insufficient detail in the simulation, such as a simple resistor that was included to account for parasitic losses as opposed to a parasitic capacitance to other parts of the sample board. A more involved simulation would, however, increase the number of free parameters in the fit and is not adding to the explanatory power of the model.

In addition to S_C, Fig. 25b shows the quantity $S_C V_0$ (blue), where V_0 is the peak-to-peak voltage of the carrier wave across the sample. This quantity depends on the attenuation in the input lines as well as the impedances in the tank circuit that can be obtained from the simulation as described earlier. Close to perfect matching, where the impedance is $50\,\Omega$, the RF-voltage across the sample is $V_0 = 117 \pm 54\,\mu\mathrm{V_{rms}}$ given an input power to the circuit of $P_{IN} = -29\,\mathrm{dBm}$. Since the sensitivity improves with power as long as the capacitance is linear with varactor voltage, it is more meaningful to consider $S_C V_0$, especially for quantum systems where input power is limited by e.g. measurement back-action.

4.2.4 Charge sensitivity, bandwidth and device read-out

In the last section I have presented a capacitance sensing experiment, that was used to characterize the sensitivity of the circuit as a function of the matching condition. To isolate that effect from the quantum dot behaviour the quantum dot was pinched off in this experiment. In this section I will present measurements with the quantum dot in the Coulomb blockade regime, where the impedance changes as a function of bias voltage V_B and gate voltage V_L.

The sensitivity of the circuit to charging of the gate electrode can be determined in a sideband experiment with gate voltage modulation as described in Sec. 4.1.2. To get a large conductance change in the sample when modulating the gate voltage, the quantum dot is tuned to the flank of a Coulomb peak at $V_L = -438.8\,\mathrm{mV}$ (marked in Fig. 27a). Figure 26a shows the SNR of the sidebands as a function of carrier frequency f_C for $V_S = 9\,\mathrm{V}$ (blue) and $V_S = 13.5\,\mathrm{V}$ (red). To maximize the SNR without broadening the Coulomb peak, the input power has been adjusted at every point to just below the threshold for broadening. In that way the voltage across the device is the same independent of the matching condition. As in the capacitance sensing experiment, perfect matching is reached at $V_S = 13.5\,\mathrm{V}$ and the SNR is highest at this point. This suggests that the impedance matching is hardly affected by the device reaching the, still highly resistive, Coulomb blockade regime. The charge sensitivity S_Q is shown in Fig. 26c and reaches $1810\,\mu\mathrm{e\ Hz}^{-0.5}$ at $V_S = 9\,\mathrm{V}$, while it reaches the best measured sensitivity $1650\,\mu\mathrm{e\ Hz}^{-0.5}$ at $V_S = 13.5\,\mathrm{V}$ with better impedance matching. The best sensitivity in this experiment is still over $200\times$ worse than the best reported value in a comparable semiconductor quantum dot system $7.2\,\mu\mathrm{e\ Hz}^{-0.5}$[40]. This is a result of the unfavourable tunnel barriers in the device, that cannot be tuned to higher transparencies causing

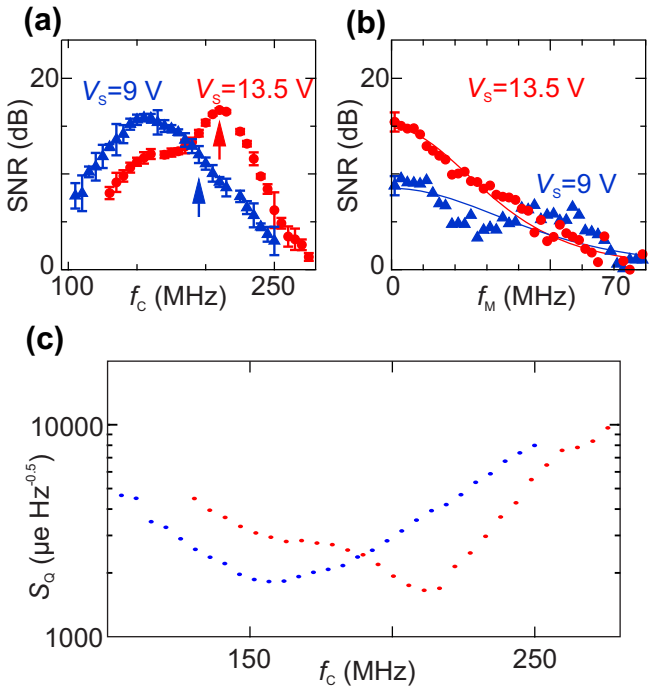

Figure 26: a) SNR as a function of carrier frequency f_C in a frequency trace that includes the perfect matching point ($V_S = 13.5$ V, red) and a frequency trace that does not ($V_S = 9$ V, blue). The used modulation frequency is $f_M = 1.1$ MHz and the input power was adjusted just below the threshold for Coulomb-peak broadening for every data point. The error bars reflect the errors related to different input powers in different data sets. b) SNR as a function of modulation frequency f_M measured using the f_C marked with arrows in a) and an input power of $P_{IN} = -31$ dBm. The error bars (only shown for the first data point) correspond to the uncertainty in the noise level of the data. From Lorentzian fits (lines), the 3-dB readout bandwidth can be extracted. c) Charge sensitivity S_Q calculated from the SNR in a). The data in all three subfigures was taken with a measurement bandwidth of $\Delta f = 10$ Hz, a modulation amplitude of 0.48 mV_{rms} and at a temperature of 1 K. [50]

high resistance and poor sensitivity according to Eq. 32. In Sec. 4.4 I will show that the sensitivity is significantly improved for a sample with more transparent tunnel barriers.

The bandwidth of this charge sensor can be determined by measuring the SNR as a function of modulation frequency f_M (Fig. 26b). The bandwidth is determined for two different matching conditions at $V_S = 9$ V and $V_S = 13.5$ V as shown in Fig. 26a where the SNR is plotted as a function of carrier frequency. Since the RF voltage across the device changes with the matching condition, the input power was adjusted for

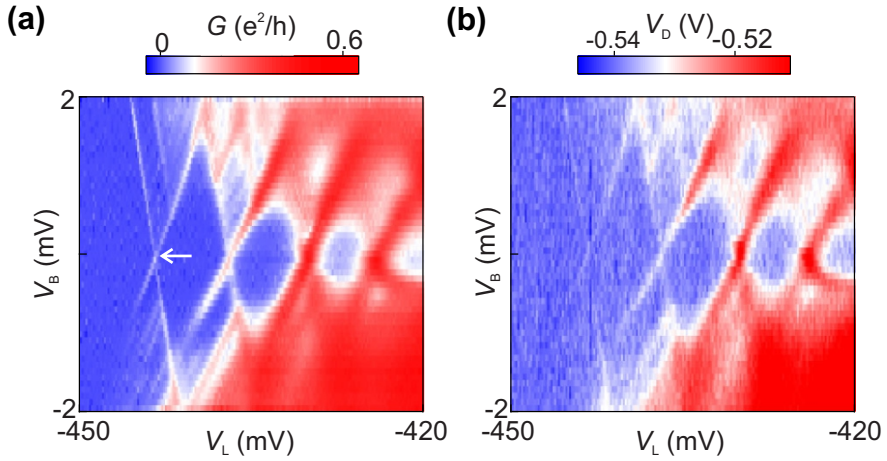

Figure 27: a) DC Conductance G through the quantum dot as a function of V_B and V_L measured at $T = 12$ mK. The white arrow marks the Coulomb peak that was used in the charge sensing experiment. b) Demodulated voltage V_D measured simultaneously at $V_S = 13.5$ V and $f_C = 210.75$ MHz. The applied power $P_{IN} = -40$ dBm does not broaden the Coulomb peaks.[50]

every data point to ensure an optimal SNR according to Eq. 32. To further contrast the behaviour in perfect matching against poor matching, the bandwidth was determined at different carrier frequencies that correspond to the best matching for the measurement at $V_S = 13.5\,\mathrm{V}$ (red arrow in Fig. 26a) and a frequency outside of the best matching for the measurement at $V_S = 9\,\mathrm{V}$ (blue arrow in Fig. 26a). The bandwidth, measured in Fig. 26b, is defined as the point in f_M where the SNR has fallen by 3 dB (factor 0.5). This point is determined by fitting the data in Fig. 26b with a Lorentzian, which yields a bandwidth of 34 MHz for $V_S = 9\,\mathrm{V}$ and a bandwidth of 18 MHz for $V_S = 13.5\,\mathrm{V}$. Note that, while the bandwidth is larger at $V_S = 9\,\mathrm{V}$, the sensitivity of the circuit is better at $V_S = 13.5\,\mathrm{V}$. This indicates a trade-off between good sensitivity and large bandwidth.

Finally the quantum dot was measured as a function of gate voltage V_L and bias voltage V_B using the demodulation circuit. Figure 27a shows the differential conductance G at 12 mK obtained from a numerical

derivative of the measured DC current. The measurement shows the characteristic Coulomb diamonds as expected for a quantum dot device. Figure 27b shows the voltage from the demodulated RF-signal V_{D} that was measured in parallel to the DC conductance with the optimized matching parameters from charge sensing $V_{\mathrm{S}} = 13.5\,\mathrm{V}$ and $f_{\mathrm{C}} = 210.75\,\mathrm{MHz}$. The power $P_{\mathrm{IN}} = -40\,\mathrm{dBm}$ does not broaden the Coulomb peaks, that are also clearly visible in the reflectometry. Note that the impedance matching could be slightly different from the previous measurements due to the colder temperature – the previous measurements were carried out at 1 K for an increased tuning range of the variable capacitor and to test a larger range of impedances.

4.2.5 Conclusion

In this section I have demonstrated the effect of impedance matching on charge and capacitance sensitivities in RF reflectometry. For this purpose, tunable capacitors were added to the tank circuit such that parasitic capacitances, bondwires or changing sample impedance can be compensated for and the tank circuit impedance is tunable to $50\,\Omega$.

A circuit model was developed to simulate the effect of tunable capacitances and the unknown parameters of the real circuit were obtained by fitting the model to the resonances from the experiment. Notably there is an unaccounted loss of 8.6 dB in the circuit between port 1 and port 2 that is either due to an underperforming BJT amplifier or losses in the cables. Further measurements of the lines have confirmed that the majority of this signal loss ($\sim 6.8\,\mathrm{dB}$) can be attributed to a faulty connector in the lines just before the BJT amplifier – the connector was replaced for the remaining experiments presented in this thesis.

Next the capacitance sensitivity was measured at different matching conditions with the optimal capac-

itance sensitivity of $1.6\,\mathrm{aF\,Hz^{-0.5}}$ recorded in perfect matching. The figure of merit in the experiment was identified as the capacitance sensitivity scaled by the voltage across the device, since the capacitance sensitivity scales with the input power as long as the varactor response is linear with the bias voltage and becomes meaningless for the evaluation of the circuit performance. The figure of merit is particularly important to estimate the read-out performance for quantum devices if the input power is limited by measurement back-action such that high input powers cannot be used to improve sensitivities.

Apart from capacitance sensing, I have presented measurements of the charge sensitivity using a GaAs quantum dot device. The best measured charge sensitivity of $1650\,\mu\mathrm{e\,Hz^{-0.5}}$ was found at the varactor bias that also produced the best capacitance sensitivity. In both experiments this corresponds to the best matching condition in the tuning range of the varactor, which indicates that the increased conductivity of the quantum dot tuned to the flank of a Coulomb peak does not significantly alter the resonance of the circuit. There is, however, a trade-off between bandwidth and sensitivity depending on the quality of the impedance matching – the bandwidth is higher for poorer matching while the sensitivity improves for better matching. Even in perfect matching, the charge sensitivity is much worse than in other measurements due to the high impedance of the sample (see Eq. 32). Despite the low charge sensitivity, it is possible to resolve Coulomb diamonds in RF with a similar contrast to a DC current measurement that was carried out in parallel.

In this chapter I have demonstrated a method that employs tunable varactors to tackle reduced sensitivities in RF read-out due to unpredictable impedance mismatches from bondwires or changes in the sample impedance. Additionally I have shown how the capacitance sensitivity of a reflectometry circuit can be measured independent from conductance or inductance changes in a device. I will use this method again

in the next chapter to further optimize a circuit with respect to the read-out of quantum capacitance in e.g. a singlet-triplet qubit.

4.3 Capacitance sensing using a SQUID amplifier

In the previous section I have demonstrated how impedance matching can lead to improved sensitivities in reflectometry circuits. Given a limited input power in perfect matching, the remaining limitation for the sensitivity is the noise in the circuit. In quantum dots and other SETs, the noise from the device is typically dominated by shot noise and increases with current. For high signal powers in highly conductive devices the noise is therefore fundamentally limited by the device, while noise from the RF-amplifiers dominates for low conductance and signal powers [50, 82]. In this section I will present measurements on the tank circuit with the GaAs quantum dot from the last section, where the tunnel barriers do not allow for high currents through the device. Since the system is dominated by noise from the RF-amplifiers I will introduce a low noise amplifier based on a SQUID to improve sensitivities.

4.3.1 SQUID amplifier optimization

As discussed in Sec. 2.3, the amplifier noise in a reflectometry circuit is dominated by the noise from the first amplifier given sufficient gain in all parts of the amplifier chain. Consequently, if the input power is fixed in a circuit with negligible device noise, the signal-to-noise ratio of the reflected signal, and therefore the sensitivity, is limited by that noise. An improvement in sensitivity due to a low noise SQUID amplifier therefore requires optimization of the SQUID amplifier gain and noise temperature.
The used SQUID amplifier was described in Sec. 4.1.3 and is implemented in the circuit as shown in Fig. 4. The green line ending in port 3 is used to test the amplifier chain independent of the reflection on the tank circuit and is coupled directly into the RF output line at the base temperature stage of the

dilution refrigerator. The SQUID amplifier is characterized using a single frequency tone at the optimized matching frequency of the tank circuit $f_C = 196\,\text{MHz}$ (see next Section) and with a power of -124 dBm at the SQUID input. While this power is well below the specified maximum input power of -100 dBm, it turns out to be larger than desirable for the best noise performance.

The gain of the SQUID amplifier was determined by comparing the total gain from port 3 to port 2 between a measurement with the SQUID amplifier in the circuit and a measurement without the SQUID amplifier in the circuit. The noise temperature at the SQUID input is determined from a measurement of the output power at port 2 after a single probe tone is applied to port 3. The power vs frequency spectrum contains a peak at the frequency of the tone with power P_P as well as the noise power after amplification P_B that can be taken from the power level away from the tone frequency. The gain in the RF output line with SQUID amplifier and BJT can be determined by comparing the power at the SQUID input to P_P. The noise level at the input of the SQUID can then be calculated from P_B via $P_\text{N} = P_\text{B} - P_\text{P} - 124\,\text{dBm}$ and the noise temperature follows from Eq. 27. All measurements were adjusted for cable and line resonances that were measured separately, thus avoiding uncertainties that could arise from the sample board or the uncharacterized SQUID amplifier.

To find the optimal noise temperature and gain, the amplifier was characterized with respect to I_SQ and I_FL as shown in Fig. 28. The amplifier was switched on with a bias current I_SQ above the critical current resulting in a voltage drop across the SQUID. To optimize the performance, the voltage drop was tuned for optimal sensitivity to the flux oscillations from the input signal $\delta\Phi$. This can be achieved by optimizing the flux offset Φ_0 using I_FL such that the flux-offset tunes the amplifier to a steep point in $V_\text{OUT}(\Phi_0 + \delta\Phi)$ – remember that that the gain is proportional to $dV_\text{OUT}/d\Phi$.

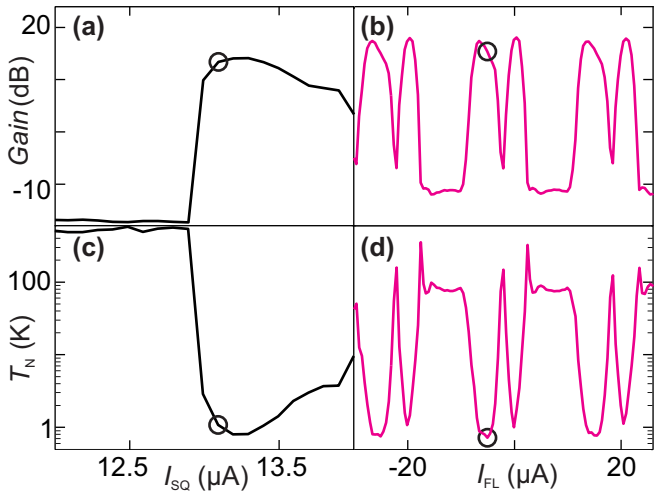

Figure 28: Characterization of the SQUID amplifier as a function of the current bias I_{SQ} (black) and the flux coil bias I_{FL} (purple) at frequency 196 MHz and SQUID input power -124 dBm. The black markers indicate the chosen values for the measurements in the remainder of this section $I_{SQ} = 13.1\,\mu$A and $I_{FL} = -5\,\mu$A. a) Amplifier power gain at $I_{FL} = 0$ as a function of I_{SQ}. b) Gain as a function of I_{FL} at $I_{SQ} = 13.1\,\mu$A. c) Noise temperature T_N as a function of I_{SQ} determined from a power vs frequency spectrum at every point in a). d) Noise temperature as a function of I_{FL}. The minimal noise temperature $T_{N,\,min} = 730 \pm 60$ mK was measured at $I_{FL} = -5\,\mu$A and this point was chosen for the measurements in the remainder of this section. The gain at this point is 15.5 ± 0.7 dB, while the maximum gain at $I_{FL} = -6.5\,\mu$A is 17.4 ± 0.7 dB ($T_N = 890 \pm 45$ mK).

Figure 28 shows the performance of the SQUID amplifier as a function of the bias current I_{SQ} (Fig. 28a,c) and I_{FL} (Fig. 28b,d). For low I_{SQ} the SQUID junctions are biased below their critical current and the output voltage is close to zero which leads to a gain below unity (less than 0 dB). As I_{SQ} is increased above the critical current (12.9 μA in Fig. 28a), a voltage drops across the SQUID and the gain increases abruptly. When the amplifier is on, the gain varies with the bias current due to the self-inductance of the system. This effect can be accounted for with the flux current, such that the gain can be optimized for all measured bias currents larger than the critical current. As indicated by the black marker in Fig. 28a, a bias current of $I_{SQ} = 13.1\,\mu$A was chosen to minimize heating from the current bias while being above the critical current.

Figure 28b shows the power gain of the amplifier at $I_{SQ} = 13.1\,\mu A$ as a function of current through the nearby coil I_{FL}. The gain varies periodically with I_{FL} reflecting the periodicity of the maximum supercurrent as a function of flux through the SQUID as approximated by Eq. 34. This periodical variation does not follow the square of a cosine, like it would for the simplified ideal case presented in Sec. 4.1.3, because thermal effects, self-inductance and capacitances cannot be neglected [105]. The black marker in Fig. 28b indicates $I_{FL} = -5\,\mu A$ that was chosen for the remaining measurements with the SQUID amplifier producing a gain of 15.5 ± 0.7 dB. Note that the gain for this value of I_{FL} is not at its maximum of 17.4 ± 0.7 dB, that is reached for $I_{FL} = -6.5\,\mu A$, because the amplifier was tuned for minimum noise rather than maximum gain. The error in the measurement of the gain is accumulated over multiple measurements that are needed to determine the losses in lines, cables and the gain of the BJT amplifier.

Figures 28c,d show the noise from the SQUID amplifier parameterized by the noise temperature T_N as a function of bias current and flux current. Figure 28c shows the noise temperature as a function of bias current at $I_{FL} = 0\,\mu A$. Before the amplifier switches on at $I_{SQ} = 12.9\,\mu A$ the dominant noise power in the measurement stems from the low noise BJT amplifier, such that T_N in that regime is not representative for the noise from the SQUID. For $I_{SQ} > 12.9\,\mu A$ the amplifier is on and the noise temperature follows the inverse of the gain as expected from Sec. 4.1.3. Figure 28d shows the noise temperature at $I_{SQ} = 13.1\,\mu A$ as a function of I_{FL}. Again the noise temperature follows the inverse of the gain except for some discrepancies around the points of highest gain/lowest noise temperature. The minimum noise temperature at $I_{FL} = -5\,\mu A$ is $T_N = 730 \pm 60\,mK$ and was chosen for the remaining measurements to optimize the sensitivities of the circuit, not maximize gain (black marker in Fig. 28d). The highest gain of 17.4 ± 0.7 dB is recorded at $I_{FL} = -6.5\,\mu A$ where the noise temperature is $890 \pm 45\,mK$. A shift in

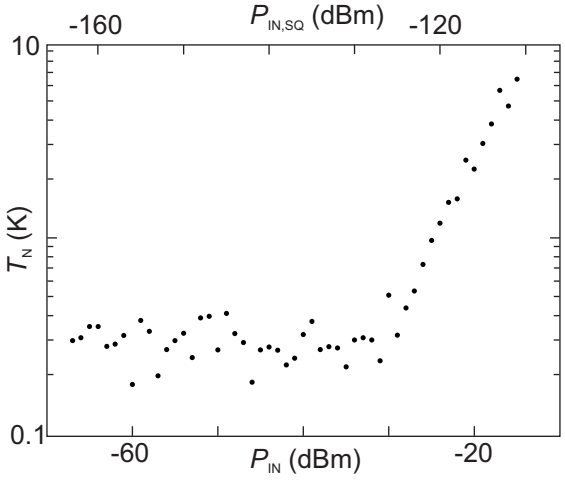

Figure 29: Noise temperature T_N as a function of input power into port 1 P_{IN} (bottom axis) as well as the power on the SQUID amplifier input $P_{IN,SQ}$ (top axis). The average $T_N = 286\,\text{mK}$ below $P_{IN} < -31\,\text{dBm}$.

I_{FL} between optimal power gain and optimal noise temperature has been observed before by Schmidt *et al*. [108] and linked to current noise from induced currents close to the highest gain.

The minimum noise temperature $T_N = 730 \pm 60\,\text{mK}$ is about a factor of 5 better than the noise temperature from the BJT (3.7 K), but far away from the best reported value of 47 mK for a SQUID amplifier at 519 MHz in a dilution refrigerator with a bath temperature below 100 mK [109]. It can be reduced by applying less input power to the SQUID as shown in Fig. 29. In this figure the noise temperature is plotted against the input power into port 1 in a reflectometry experiment that is discussed in the next section. To estimate the input power to the SQUID from the input power into port 1, the reflection coefficient and the attenuation in the input line need to be considered – a rough estimate, using the circuit specifications and the resonance for the best impedance matching, yields $P_{IN,SQ} = P_{IN} - 96$ dB. The average noise temperature in Fig. 29 for $P_{IN} < -31$ dBm ($P_{IN,SQ} < -127\,\text{dBm}$) is $T_N = 286\,\text{mK}$ and therefore still larger than the 47 mK reported in Ref. [109]. Possible reasons for the low input power tolerance and increased

noise temperature are poor matching to the impedance of 50 Ω on the input side of the amplifier, radiation from outside of the dilution refrigerator and/or poor thermalization [101].

4.3.2 Impedance matching and capacitance sensitivity

In this section I will follow the impedance matching procedure that is required to optimize sensitivities as previously shown in Sec. 4.2.2. Although the SQUID amplifier should have an input impedance close to 50 Ω and therefore not affect the matching condition, the best matching in this experiment is at a different frequency and varactor voltage. This could be related to the measurement temperature that is reduced from 1 K to 12 mK and could alter the properties of the surface mount components on the sample board (e.g. from less free charge carriers in the varactors).

To optimize the impedance matching between the tank circuit and the input network, the varactor is tuned using V_S. Figure 30a shows the transmission from port 1 to port 2 $|S_{21}|$ for different settings of V_S. The lowest reflection coefficient and therefore the best matching is achieved at $f_C = 196\,\text{MHz}$ when $V_S = 6.8\,\text{V}$.

Figure 30b shows the associated capacitance sensitivity S_C that was determined in a sideband experiment similar to Sec. 4.2.3. For each value of V_S the frequency was adjusted to the point of minimal reflection since the sensitivity is optimized at the best matching frequency. As expected, the best sensitivity of $S_C = 0.9 \pm 0.2\,\text{aF Hz}^{-0.5}$ is measured closest to perfect matching at $f_C = 196\,\text{MHz}$ and $V_S = 6.8\,\text{V}$ [50]. The sensitivities in Fig. 30b were measured with an input power of $P_{IN} = -60\,\text{dBm}$ into port 1 which approximately corresponds to $-156\,\text{dBm}$ on the SQUID input after attenuation and reflection on the circuit board. This power should be well below the maximum input power of the SQUID and not cause non-

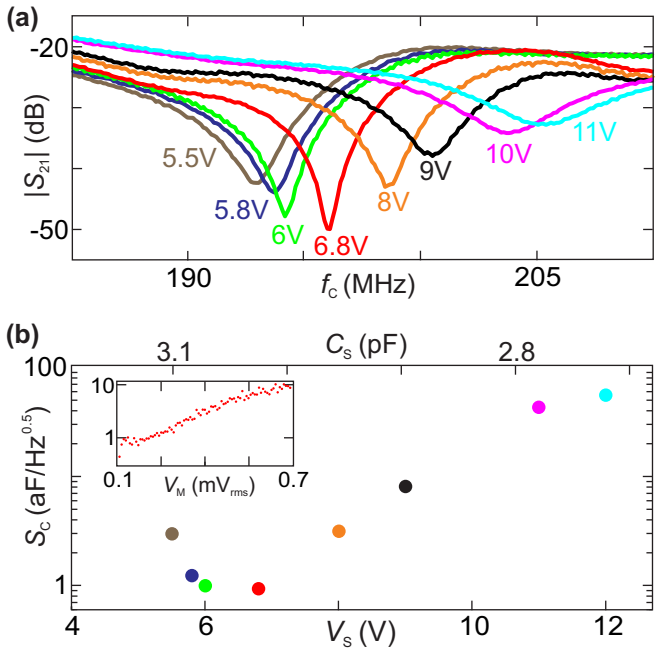

Figure 30: a) Transmission between port 1 and port 2 $|S_{21}|$ as a function of carrier frequency f_C at the varactor voltages indicated. b) Capacitance sensitivity S_C at modulation frequency $f_M = 3\,\text{kHz}$, modulation amplitude $V_M = 99\,\mu\text{V}_{\text{rms}}$ and input power $P_{IN} = -60\,\text{dBm}$ as a function of varactor voltage V_S. The carrier frequency was adjusted to the best matching point for each value. Inset: Capacitance sensitivity S_C as a function of V_M at $f_M = 3\,\text{kHz}$, $P_{IN} = -60\,\text{dBm}$, $V_S = 6.8\,\text{V}$ and $f_C = 196\,\text{MHz}$.

linearities or increased noise. The sideband experiment was carried out using a modulation amplitude of $V_M = 99\,\mu\text{V}_{\text{rms}}$, where the sidebands were clearly visible and no harmonics could be observed above the noise level. The frequency of the capacitance modulation was chosen as $f_M = 3\,\text{kHz}$ which is large enough for good separation from the main carrier peak and well below the cutoff from the filtering of the lines.

The inset of Fig. 30b shows the sensitivity for the optimized matching parameters as a function of modulation amplitude V_M. The sensitivity is worsening for higher amplitudes because power at the sideband frequencies is lost to harmonics in the spectrum that arise from a non-linear response of the varactor.

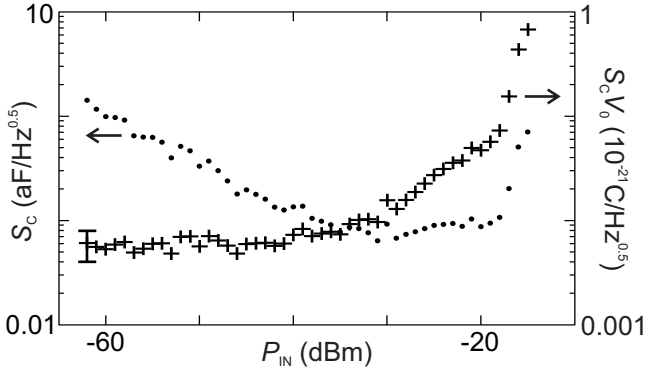

Figure 31: Capacitance sensitivity S_C (left axis, points) and the product of the capacitance sensitivity with the applied voltage across the varactor $V_0 S_C$ (right axis, crosses) as a function of the input power at port 1 P_{IN}. The errors in S_C are smaller than the symbols and due to uncertainties in determining the noise level. The errors in $V_0 S_C$ are due to uncertainties from the noise level as well as the measurement of the input lines/cables. For clarity one single error bar is marked. Other parameters: $f_M = 3\,\text{kHz}$, $V_M = 80\,\mu\text{V}_{\text{rms}}$, $f_C = 196\,\text{MHz}$ and $V_S = 6.8\,\text{V}$.

For further measurements the amplitude is chosen slightly smaller than in Fig. 30b to be $V_M = 80\,\mu\text{V}_{\text{rms}}$, which ensures that there is no non-linear effect from the varactor, but still sufficient modulation to clearly distinguish the sidebands from the noise level in the measurement.

While the low input power yields the full benefit of the reduced noise from the SQUID amplifier, the capacitance sensitivity can be improved with higher input power due to increased signal strength compared to the noise. For input powers $> -31\,\text{dBm}$ this benefit can disappear due to increased SQUID amplifier noise. I will therefore present a measurement as a function of the input power P_{IN} into port 1 and study the capacitance sensitivity as well as the figure of merit $S_C V_0$. This measurement is shown in Fig. 31 where the capacitance sensitivity improves with increasing power until an optimal power of $P_{IN} = -31\,\text{dBm}$. At this power the sensitivity reaches $S_C = 0.07 \pm 0.02\,\text{aF Hz}^{-0.5}$, which represents an improvement to the measurement without the SQUID amplifier of x26. The optimized power corresponds to approximately $-127\,\text{dBm}$ on the SQUID input after attenuation in the input line and reflection on the circuit board. From

$-31\,\mathrm{dBm}$ to around $-18\,\mathrm{dBm}$ (-127 to $-114\,\mathrm{dBm}$ on the SQUID input) the sensitivity stays relatively constant before worsening at higher input power. The noise level in this measurement was extracted and analyzed previously in Fig. 29.

The behaviour of S_C as a function of input power can be explained with the increasing noise in the SQUID amplifier. The different regions in Fig. 31 could then be associated to the flux through the SQUID with respect to the flux-voltage transfer function $V_\mathrm{OUT}(\Phi_0)$. The constant region between -31 and -18 dBm could be interpreted as the regime where the induced flux from the input signal $\delta\Phi$ is exceeding the linear range of $V_\mathrm{OUT}(\Phi_0+\delta\Phi)$ (compression). This results in additional frequency components in the spectrum, such that there is less gain at the relevant sideband frequency while the noise increases – an increasing power is therefore less beneficial. For $P_\mathrm{IN} > -18\,\mathrm{dBm}$, when the flux exceeds a quarter of the period of $V_\mathrm{OUT}(\Phi_0)$, the flux oscillation is reaching beyond the maxima and minima of $V_\mathrm{OUT}(\Phi_0)$ causing the amplification to break down and the sensitivity to worsen rapidly (above saturation).

For many applications, including direct read-out of spin-qubits, the measurement back action cannot be neglected if e.g. quantum states are close enough in energy such that a bias from the RF signal could cause a transition. As discussed before, it is therefore useful to optimize a circuit with respect to the figure of merit $S_\mathrm{C}V_0$ – especially since it is not meaningful to optimize S_C when the SNR can be improved with higher input powers in case there is no power limited amplifier. $S_\mathrm{C}V_0$ is shown in Fig. 31 on the right y-axis as a function of input power into port 1. Until $-41\,\mathrm{dBm}$ (or -137 dBm on the SQUID) $S_\mathrm{C}V_0$ is constant before it increases for higher powers. While this behaviour can be attributed to the increasing noise shown in Fig. 29 for input powers $P_\mathrm{IN} > -31\,\mathrm{dBm}$, $S_\mathrm{C}V_0$ seems to increase already at lower input powers $P_\mathrm{IN} > -41\,\mathrm{dBm}$. Given the relatively large fluctuation of the extracted noise temperature in Fig. 29, it is

possible that the increasing noise temperature between -41 dBm and -31 dBm was not observable.

4.3.3 Estimated read-out time for a spin singlet-triplet qubit

As mentioned previously, reflectometry with a low noise amplifier is beneficial for the read-out of devices that produce a negligible noise power. If additionally the input power into the reflectometry circuit is limited by the requirements of the device rather than the input power limitations of the amplifier, it is possible to achieve highly improved read-out sensitivities with a SQUID amplifier. One example for such a system is a singlet-triplet spin qubit in a double quantum dot. In this section I will estimate the time it would take to read out a singlet-triplet qubit in a GaAs double quantum dot measured by Petersson *et al*. [47] based on the sensitivities from the experiments presented in Sec. 4.2 and 4.3 that are summarized in Table 1.

This type of qubit is made from two electrons trapped in a double quantum dot. The spins of the electrons can be aligned such that hybridization is not allowed due to Pauli's principle and the electrons remain in two separate electron states (triplet-state) even if there is a finite tunnel coupling. If the spins are antiparallel, the Pauli exclusion principle does not apply and the spins hybridize (singlet-state). The distribution of the wave function over two quantum dots in the singlet-state can thus be locally manipulated resulting in a quantum capacitance. An applied RF signal can therefore change the charge distribution, which alters the impedance and therefore the reflected signal in reflectometry compared to a qubit in the triplet state. In that way reflectometry can be used to read-out the qubit state via its quantum capacitance. Since the qubit itself is not investigated in this thesis, I want to refer the reader to e.g. Ref. [80] for more details about singlet-triplet qubits.

The maximum quantum capacitance in the qubit from Petersson *et al*. is around $C_{\mathrm{Q}} = 19$ fF (assuming

$\lambda = 1$ and $V_0 = 0$ in Eq. 39), such that one could naively estimate the read-out time using Eq. 37 and conclude that read-out should be possible with unity SNR in a bandwidth:

$$\sqrt{\Delta f} = \frac{C_\mathrm{Q}}{S_\mathrm{C}} \tag{38}$$

This would convert to a read-out time of $\tau = (S_\mathrm{C}/C_\mathrm{Q})^2$ which yields 7 ns without the SQUID amplifier and 14 ps with the SQUID amplifier. This naive calculation does not take into account the behaviour of the quantum capacitance as a function of detuning between the quantum dot chemical potentials, which can be derived following Ref. [47]:

$$C_\mathrm{Q} = (e\lambda)^2 \frac{(2t)^2}{2\left((\lambda e V_0)^2 + (2t)^2\right)^{3/2}} \tag{39}$$

Here $\lambda e V_0$ is the detuning between the chemical potentials of the two quantum dots from the applied RF signal, $\lambda = 0.3$ is the gate coupling, $t = h \times 500\,\mathrm{MHz}$ is the coupling energy between the two quantum dots and I have considered the limit $k_\mathrm{B}T \ll 2t$.

The naive calculation according to Eq. 38 assumes that the quantum capacitance remains constant over the entire cycle of the RF oscillation – this is only valid for $eV_0 \ll 2t$. I will therefore estimate the read-out time for larger amplitudes using the average capacitance over the RF cycle:

$$\overline{C_\mathrm{Q}} = \frac{1}{2V_0}\int_{-V_0}^{V_0} C_\mathrm{Q}(x)\mathrm{d}x \tag{40}$$

The read-out bandwidth can then be calculated via [58]:

$$\sqrt{\Delta f} = \frac{\overline{C_{\mathrm{Q}}}}{S_{\mathrm{C}}} \tag{41}$$

At an input power of $-29\,\mathrm{dBm}$ this yields $\tau = 62\,\mu\mathrm{s}$ given the best capacitance sensitivity without the SQUID amplifier and $\lambda = 0.3$. Figure 32 shows the read-out time τ as a function of input power in the experiment with the SQUID amplifier. At higher powers the average quantum capacitance is low and the noise temperature increases such that the SNR drops and the read-out takes longer. At low powers the average quantum capacitance is high, but the signal level is small such that the SNR is low. A sweet spot is found at $P_{\mathrm{IN}} = -46\,\mathrm{dBm}$ where the predicted read-out time is 26 ns.

The result of a quantum computation needs to be read-out before the qubit state decays and the information is lost. For a state-of-the-art decay time of $34\,\mu\mathrm{s}$ [110] this means that read-out without a SQUID

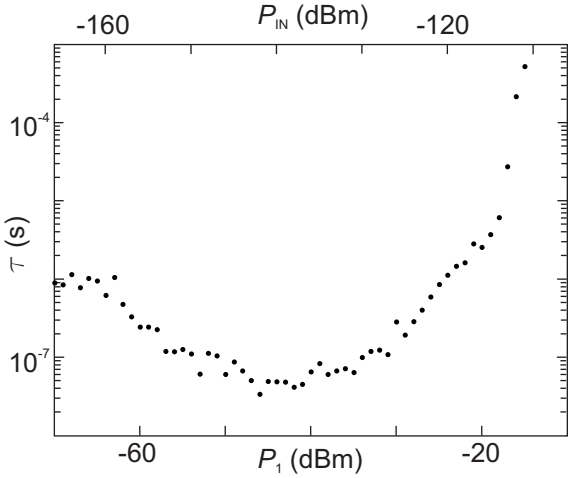

Figure 32: Predicted read-out time τ as a function of input power at port 1 P_{IN} (bottom axis) and the corresponding power at the SQUID amplifier input $P_{\mathrm{IN,SQ}}$ (top axis).

	S_C (aF Hz$^{-0.5}$)	$S_C V_0$ (10^{-21} CHz$^{-0.5}$)	τ (μs)
No SQUID amplifier	1.6	0.2	61
With SQUID amplifier	0.07	0.006	0.026

Table 1: Overview of the capacitance sensitivity S_C, figure of merit $S_C V_0$ and predicted read-out time τ for the measurements with and without the SQUID amplifier.

would require averaging over multiple cycles of the computation, while the read-out with the SQUID amplifier could be done in a "single-shot".

4.3.4 Charge sensitivity

In this section I will optimize the charge sensitivity of the reflectometry circuit with the SQUID amplifier and the GaAs quantum dot. The noise in this circuit is dominated by the amplifier chain such that employing a SQUID amplifier can improve the sensitivity if the input power limitations of the SQUID are not exceeded. This is the case since the charging energy of the device limits the input power at port 1 and the reflected power that reaches the SQUID input is further reduced by good impedance matching. I will therefore demonstrate the same factor of improvement in charge sensitivity as in capacitance sensitivity (x26).

The charge sensitivity can be calculated from the SNR of the sidebands that arise when the charge on the gate is modulated (see Eq. 28). To calculate the charge modulation one needs to compare the voltage modulation δV_L to the distance between Coulomb peaks ΔV_{CB} that corresponds to the addition of one electron. The ratio $\delta V_L / \Delta V_{CB}$ was determined by measuring the Coulomb peaks in DC-current as a function of V_L and applied modulation voltage (see Fig. 53 in the Appendix). The distance between the Coulomb peaks can be taken from the current-V_L trace at zero modulation amplitude, while the broaden-

ing at higher modulation voltage is used to determine δV_L in units of ΔV_{CB}.

Figure 33 shows the charge sensitivity as a function of gate voltage. The parameters used in this measurement were chosen without optimization to be $f_C = 197\,\mathrm{MHz}$, $V_S = 7\,\mathrm{V}$, $P_{IN} = -38\,\mathrm{dBm}$, $f_M = 6\,\mathrm{kHz}$ and $\delta V_L = 117.8\,\mu\mathrm{V_{rms}}$. The charge sensitivities were determined considering the different values for δQ corresponding to the different distances between Coulomb peaks. In comparison with the DC conductivity, that is plotted as a function of gate voltage V_L and bias voltage V_B in Fig. 37a, Fig. 33 confirms that the sensitivity reaches a minimum at the flanks of the Coulomb peaks. The best sensitivity $S_Q = 295\,\mu e\mathrm{Hz}^{-0.5}$ is measured at $V_L = -315.6\,\mathrm{mV}$ (green marker in Fig. 33), such that the next optimization steps are carried out at that gate voltage. Note that the optimal gate voltage after the optimization of the other parameters might be slightly different, because the optimized modulation voltage and RF power might cover a slightly different parameter space in V_L and V_B. For example a large RF-power might cause fluctuations in the quantum dot potential via capacitive coupling to the source that encompasses more non-linear features of the Coulomb peak, causes additional sidepaks and therefore reduced SNR at the measured sideband frequency.

Figure 34a shows the optimization of S_Q with respect to varactor voltage V_S. Since the sensitivity is best close to perfect matching, as demonstrated in Sec. 4.2, the carrier frequency is adjusted to the best matching point for every voltage. The best sensitivity of $S_Q = 182\,\mu e\mathrm{Hz}^{-0.5}$ is found at $V_S = 6.1\,\mathrm{V}$ and $f_C = 194.56\,\mathrm{MHz}$ (green marker in Fig. 34a). This is slightly different from the ideal matching condition in the capacitance sensitivity optimization, since the quantum dot is contributing to the tank circuit impedance differently when it is more conductive.

Figure 34b shows S_Q as a function of the input power P_{IN} applied to port 1. The input power is lim-

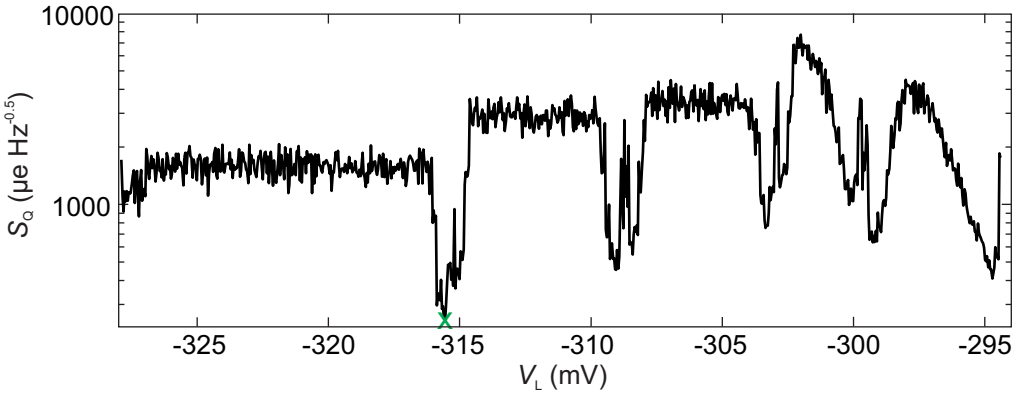

Figure 33: Charge sensitivity S_Q as a function of gate voltage V_L at $f_C = 197\,\text{MHz}$, $V_S = 7\,\text{V}$, $f_M = 6\,\text{kHz}$, $\delta V_L = 117.8\,\mu\text{V}_{\text{rms}}$ and $P_{IN} = -38\,\text{dBm}$. The chosen gate voltage for further optimization $V_L = -315.6\,\text{mV}$ is indicated by the green marker.

ited by the SQUID amplifier such that $S_Q(P_{IN})$ shows similar behaviour to $S_C(P_{IN})$ shown in Fig. 29. Small differences could be caused by a changed matching condition due to a more conductive sample, which causes a slight difference in the powers on the SQUID input as a function of P_{IN}. Additionally the trade-off between larger input power to the device and increased noise in the SQUID amplifier can result in a sweet spot at a different P_{IN}. The best charge sensitivity $S_Q = 93\,\mu e\text{Hz}^{-0.5}$ was measured at $P_{IN} = -26\,\text{dBm}$ (green marker in Fig. 34b).

Figure 35 shows the optimization of the sensitivity with respect to the modulation amplitude δV_L. Similar to the capacitance sensitivity as a function of the modulation amplitude of the varactor, the sensitivity worsens for increasing gate modulation amplitude due to non-linearities that lead to additional sidebands and less power at $f_C \pm f_M$ – here the non-linearities are inherent to the flank of the Coulomb peak. The best sensitivity in Fig. 35 $S_Q = 80\,\mu e\text{Hz}^{-0.5}$ is measured at the lowest modulation amplitude $\delta V_L = 12\,\mu\text{V}_{\text{rms}}$. At smaller modulation amplitudes other peaks become larger than the sideband at $f_C \pm f_M$.

Finally, the charge sensitivity is measured again as a function of gate voltage using the optimized parame-

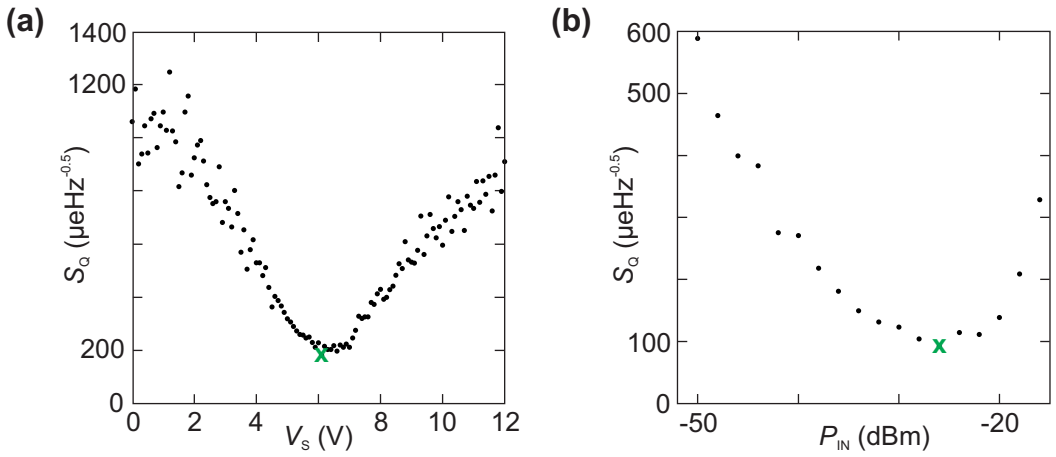

Figure 34: a) Charge sensitivity S_Q as a function of varactor voltage V_S at $V_L = -315.6\,\text{mV}$, $f_M = 6\,\text{kHz}$, $\delta V_L = 117.8\,\mu\text{V}_{\text{rms}}$ and $P_{IN} = -38\,\text{dBm}$. The chosen varactor voltage for further measurements $V_S = 6.1\,\text{V}$ is indicated with the green marker. The associated carrier frequency is $f_C = 194.56\,\text{MHz}$. b) Charge sensitivity S_Q as a function of P_{IN} at $V_L = -315.6\,\text{mV}$, $f_C = 194.56\,\text{MHz}$, $V_S = 6.1\,\text{V}$, $f_M = 6\,\text{kHz}$ and $\delta V_L = 117.8\,\mu\text{V}_{\text{rms}}$. The optimal $P_{IN} = -26\,\text{dBm}$ is indicated with a green marker.

ters and a modulation frequency of $f_M = 3\,\text{kHz}$. The best charge sensitivity improves to $S_Q = 58\,\mu e\text{Hz}^{-0.5}$ at $V_L = -315.556\,\text{mV}$ (shown in Fig. 36a). The frequency trace associated with the best measured sensitivity is shown in Fig. 36b. While the most dominant sideband is at $f_C + f_M$ there are many other peaks in the spectrum above the noise level. It is unclear where the other peaks come from but a link to the low power tolerance of the SQUID is likely – careful filtering and shielding might improve the performance. In this experiment, the best charge sensitivity is far way from the best reported values in a semiconductor device $S_Q = 7.2\,\mu e\text{Hz}^{-0.5}$ [40] (or $1.3\,\mu e\text{Hz}^{-0.5}$ with a superconducting spiral inductor [41]). I can, however, report a $\times 26$ improved charge sensitivity compared to the measurement without the SQUID amplifier in agreement with the improvement in capacitance sensitivity [50]. The poor charge sensitivity can be explained with the theory from Eq. 32 that predicts good sensitivity for high charging energy and low resistivity: the charging energy in the GaAs sample is comparable to the silicon quantum dot in

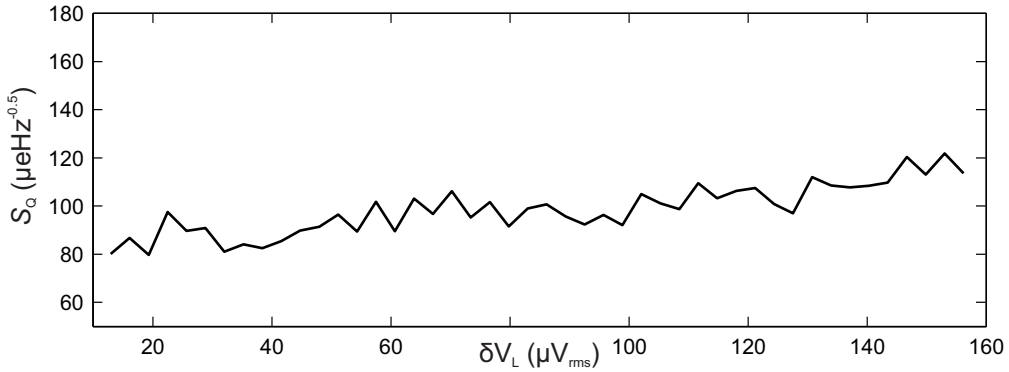

Figure 35: Charge sensitivity S_Q as a function of gate modulation amplitude δV_L at $V_L = -315.6\,\mathrm{mV}$, $f_C = 194.56\,\mathrm{MHz}$, $V_S = 6.1\,\mathrm{V}$, $f_M = 6\,\mathrm{kHz}$ and $P_{IN} = -26\,\mathrm{dBm}$. The best sensitivity is $S_Q = 80\,\mu e\mathrm{Hz}^{-0.5}$.

Ref. [40], but the resistance on the Coulomb peak is much higher (55 kΩ in Ref. [40] to 6.7 MΩ in the GaAs quantum dot) [39]. I therefore conclude that the charge sensitivity in the presented setup is limited by the device resistance and could be improved with an optimized device.

Finally the GaAs quantum dot was measured in RF-reflectometry as a function of gate voltage V_L and

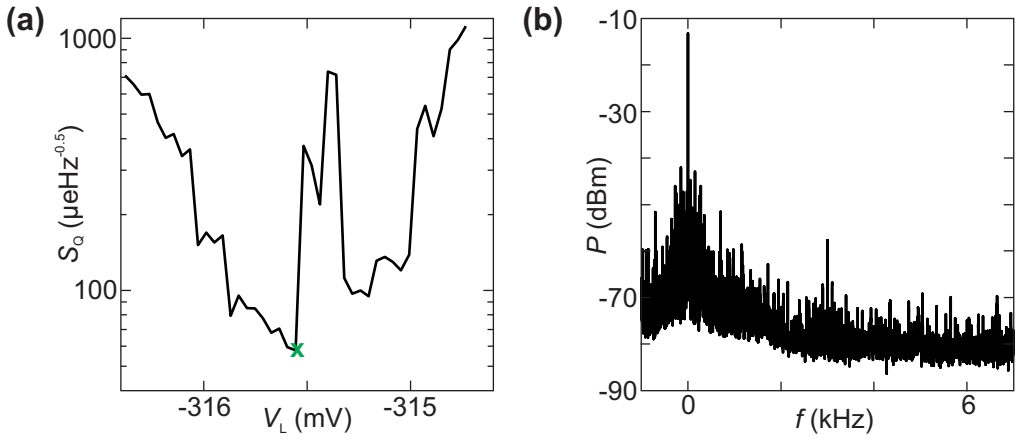

Figure 36: a) Charge sensitivity S_Q as a function of gate voltage V_L measured using $\delta V_L = 15.7\,\mu\mathrm{V_{rms}}$, $f_C = 194.56\,\mathrm{MHz}$, $V_S = 6.1\,\mathrm{V}$, $f_M = 3\,\mathrm{kHz}$ and $P_{IN} = -26\,\mathrm{dBm}$. The best sensitivity $S_Q = 58\,\mu e\mathrm{Hz}^{-0.5}$ is indicated with the green marker. b) Power P at port 2 (after additional room temperature amplification) as a function of frequency in the sideband experiment that leads to the best observed charge sensitivity $S_Q = 58\,\mu e\mathrm{Hz}^{-0.5}$. Parameters: $V_L = -315.556\,\mathrm{mV}$, $\delta V_L = 15.7\,\mu\mathrm{V_{rms}}$, $f_C = 194.56\,\mathrm{MHz}$, $V_S = 6.1\,\mathrm{V}$, $f_M = 3\,\mathrm{kHz}$ and $P_{IN} = -26\,\mathrm{dBm}$.

bias voltage V_B using the optimized charge sensing parameters and the homodyne detection circuit (shown in Fig. 4). For comparison, Fig. 37a shows the differential conductance G calculated from the parallel DC current measurement (numerical derivative), while Fig. 37b shows the demodulated voltage V_D. Both measurements clearly show the characteristic Coulomb diamonds.

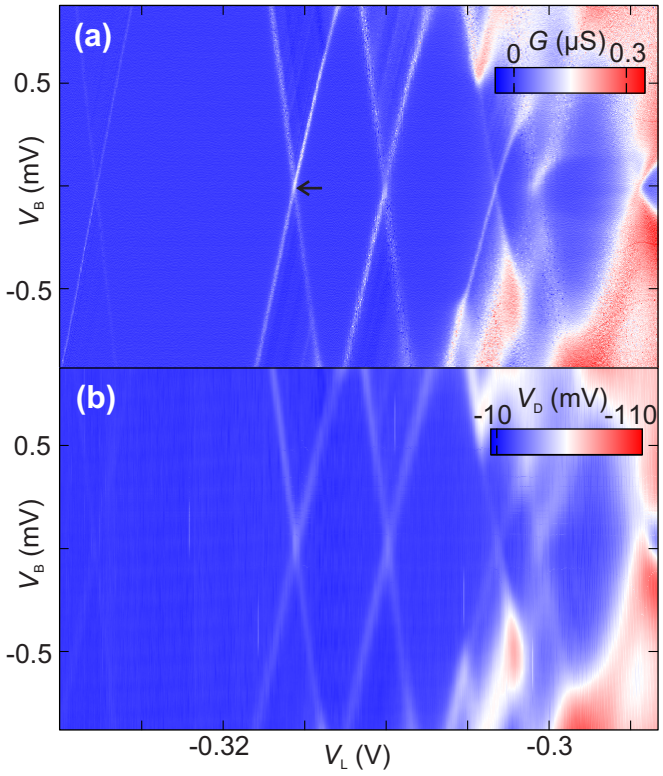

Figure 37: a) Conductance G as a function of gate voltage V_L and bias voltage V_B. The black arrow indicates the Coulomb peak where the charge sensitivity was measured. b) Demodulated voltage V_D from the homodyne detection as a function of gate voltage V_L and bias voltage V_B.

4.3.5 Conclusion

In this section I have presented data from my experiments with a radio frequency SQUID amplifier that can improve the sensitivity of the RF read-out in case the noise in the circuit is dominated by the ampli-

fiers and the input power is limited.

The SQUID amplifier was characterized with respect to offset flux and bias current displaying a behaviour that agrees qualitatively with previous work. The extracted noise temperature of 730 mK is much higher than expected and related to the high input power. For lower input powers the noise temperature improves to 286 mK, but is still away from the best reported value of 47 mK [109]. Nevertheless the addition of the SQUID amplifier leads to a significant improvement compared to the 3.7 K noise temperature from the BJT amplifier that dominated the noise in the previous measurement.

After the SQUID was optimized for low noise, the impedance matching was carried out similar to Sec. 4.2.2. The optimized capacitance sensitivity $S_C = 0.07\,\mathrm{aFHz}^{-0.5}$ has improved by a factor of 26 between the experiment with and without the SQUID amplifier. This is a larger improvement than expected for the difference in noise temperatures, that should contribute a factor of $\sqrt{3.7\,\mathrm{K}/286\,\mathrm{mK}} = 3.6$ according to Ref. [58]. The additional improvement is related to a reduced insertion loss into the tank circuit and reduced losses in the tank circuit at colder temperatures. Rewiring the circuit to accommodate the SQUID amplifier and thereby fixing the broken connector, that caused losses in the previous experiment, is responsible for a large fraction of the improvement.

The performance of the capacitance measurement in terms of $S_C V_0$ was evaluated with respect to the read-out time of a singlet-triplet qubit. While the performance in the experiment without the SQUID amplifier would require a read-out time of 61 µs, the experiment with the SQUID suggests a read-out time of 26 ns. Given a state-of-the-art decay time of 34 µs in a singlet-triplet qubit it should therefore be possible to read-out the qubit state in a single shot with the SQUID amplifier [110].

The best charge sensitivity was found to be $S_Q = 58\,\mu e\mathrm{Hz}^{-0.5}$, which is not a state-of-the-art value, but

corresponds to a factor of 26 improvement with respect to the previous experiment without the SQUID amplifier. This can be explained with the low transparency tunnel barriers in the device: Since charge sensing benefits from a big impedance change as a function of electric field, the ideal sensitivity can be reached at the flanks of the Coulomb peaks. While the optimal Coulomb peak is very conductive with highly transparent tunnel barriers according to Eq. 32, it also needs to be sharp which means that lifetime broadening cannot not be too strong. Since transparent tunnel barriers also lead to lifetime broadening, this results in a trade-off between conductivity and broadening. Ideally the optimal tunnel barrier is found in a device where the tunnel barriers can be tuned independent from the island potential – this is not possible in the measured GaAs quantum dot because one gate does not work. The present tunnel barriers do not allow for a high conductivity such that the GaAs quantum dot cannot be used for charge sensing with a sensitivity close to the theoretical limit.

In the next section I will present an experiment on the silicon nanowire device from Sec. 3.3.1 where Coulomb blockade is dominating the transport. The tunnel barriers in that device are more transparent than in the GaAs quantum dot such that better charge sensitivities should be possible.

4.4 Charge sensing with a silicon nanowire single electron transistor

In the previous two sections I have introduced an impedance matching circuit and a low noise SQUID amplifier to improve the capacitance and charge sensing performance of an RF reflectometry circuit. While impedance matching improves the sensitivity of the circuit independently of device and amplifiers, the SQUID amplifier is only beneficial for low device noise and input power.

In this section I will demonstrate charge sensing using the silicon nanowire from Sec. 3.3.1 (see Fig. 1) which shows a better sensitivity than the previously used GaAs quantum dot. In this device the transport is dominated by Coulomb blockade with more transparent tunnel barriers than in the GaAs quantum dot. Since there is only one gate, however, it is not possible to tune the tunnel barriers independently of the island potential. The transparency of the barriers can therefore not be tuned to the optimal point where transparency is maximized without significant lifetime broadening. Nevertheless I will show charge sensitivities close to the best reported values in a top down fabricated device that could be integrated in a CMOS architecture.

4.4.1 Charge sensitivity

As demonstrated previously in Sec. 4.3.4, the optimal charge sensitivity is achieved when modulation amplitude, modulation frequency, input power, matching frequency and varactor voltage are optimized. The optimal sensitivity can only be reached if the tank circuit can be tuned into matching within the available varactor voltage range. Since the impedance of the tank circuit changes significantly with the more conductive device, it cannot be matched within the tunable range of the varactor when using the

same inductor as in the previous experiments. A different inductor with $L = 140\,\mathrm{nH}$ was therefore used in this experiment and the associated matching frequencies are elevated as a result. This prevents the use of the SQUID amplifier that does not operate at the new frequency range.

As demonstrated in Fig. 38a, where $|S_{21}|$ is shown as a function of f_C for different V_S, the tuning range of the varactor is sufficient to tune the circuit impedance through a point close to perfect matching. In this measurement the best matching is recorded at $V_S = 10.6$ V and $f_C = 330.4\,\mathrm{MHz}$, but the resonance at $V_S = 11.6$ V indicates very similar matching. Since the matching needs to be optimized for charge sensing on the flank of a Coulomb peak, but at this point of the optimization it is not clear which Coulomb peak will produce the best sensitivity, the gate voltage in the measurements from Fig. 38a was chosen at an arbitrary Coulomb peak flank.

Figure 38b shows the charge sensitivity S_Q obtained in a sideband experiment as a function of varactor voltage V_S. As this is the first step of the optimization procedure, the other parameters in the sideband measurement are chosen close to the values from previous experiments. Additionally, since the sensitivity is improving for improved matching, the carrier frequency f_C was adjusted to the best matching for every varactor voltage in Fig. 38b. Note that the gate voltage was changed from $V_G = 649.5\,\mathrm{mV}$ to $V_G = 643.5\,\mathrm{mV}$ between Fig. 38a and b (neighbouring Coulomb peak flank and a small adjustment for gate drift). The best charge sensitivity of $S_Q = 16.4\,\mu\mathrm{eHz}^{-0.5}$ is measured at $V_S = 12.6$ V using $f_C = 333.2\,\mathrm{MHz}$. These matching parameters are slightly different from the best matching found in Fig. 38a. However, the sensitivity in both matching points is very similar given the flat region in Fig. 38b from V_S =10 V to 13.5 V and a sensitivity measurement at the previous gate voltage also yields a comparable sensitivity of $S_Q = 17.5\,\mu\mathrm{eHz}^{-0.5}$. This suggest that small changes in the matching condition do not

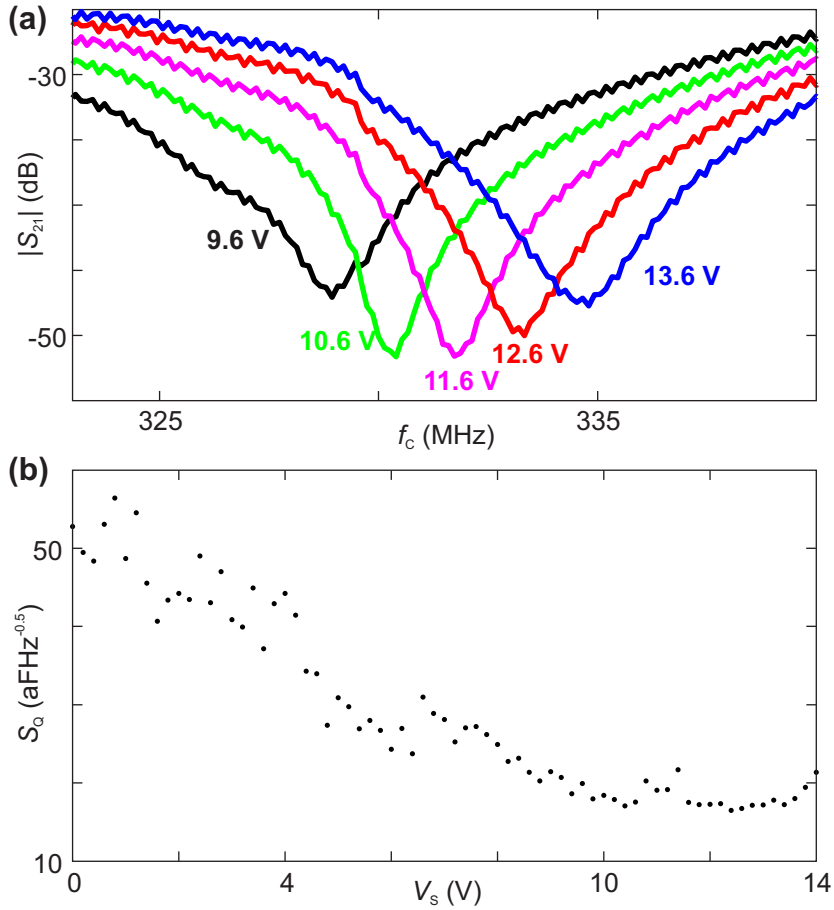

Figure 38: a) Resonances in $|S_{21}|$ as a function of carrier frequency f_C for different values of V_S as indicated. The gate was set to $V_G = 649.5\,\mathrm{mV}$. b) Charge sensitivity S_Q as a function of V_S. For every data point the frequency was adjusted to best matching. The other measurement parameters are $P_{IN} = -35\,\mathrm{dBm}$, $\delta V_G = 99\,\mu\mathrm{V}$, $f_M = 3\,\mathrm{kHz}$ and $V_G = 643.5\,\mathrm{mV}$.

significantly impact the sensitivity and slight changes in conductance between different Coulomb peaks should not require adjustment of V_S and f_C.

The modulation frequency f_M was taken from previous measurements since the filtering in the associated DC line is the same – there is no need to optimize this parameter again. On the other hand, the input power P_{IN} at port 1 as well as the gate voltage modulation amplitude δV_G depend on the measured

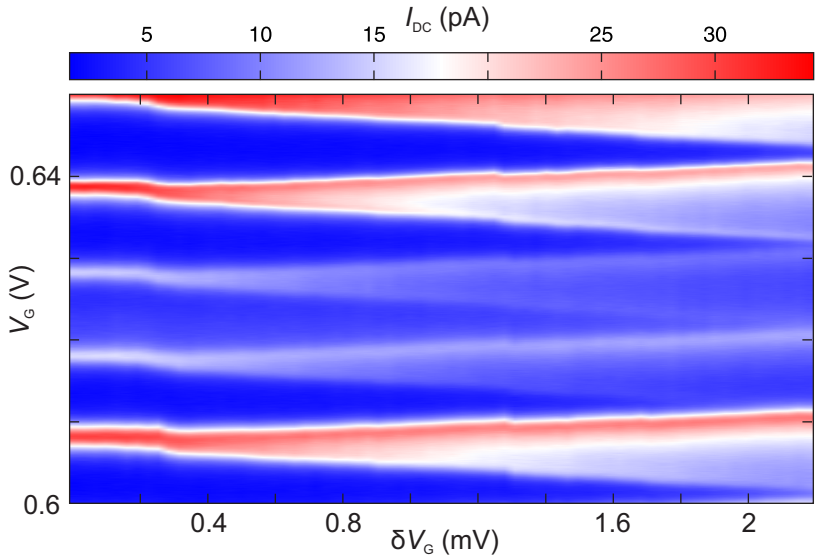

Figure 39: Current I_{DC} close to zero-bias voltage as a function of gate voltage V_G and applied gate voltage modulation δV_G.

device and require optimization. Additionally, given the variations in the Coulomb blockade from e.g. changing tunnel barrier transparency as a function of gate voltage, the sensitivity needs to be optimized with respect to the measured Coulomb peak.

The gate voltage modulation amplitude should be large enough to produce sidebands that are clearly distinguishable from the noise in the measurement, but should not reach the non-linear regime of the Coulomb peak flank to avoid significant additional sidebands – ideally the modulation amplitude is therefore much smaller than the width of a Coulomb peak on the gate voltage axis. Figure 39 shows the current I_{DC} close to zero bias voltage as a function of V_G and δV_G. Note that the broadening of the Coulomb peaks is not significant at $\delta V_G = 99\,\mu V$ which was used in the measurement from Fig. 38b. Nevertheless a slightly reduced amplitude of $\delta V_G = 75\,\mu V$ is chosen in the remaining measurements in this section, since the sidebands remain distinguishable at that modulation amplitude. The broadening of

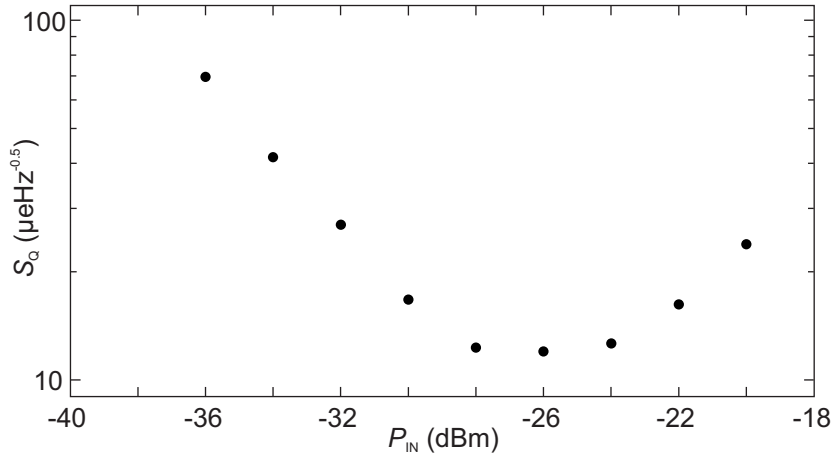

Figure 40: Charge sensitivity S_Q as a function of input power P_{IN} applied to port 1. Other parameters $V_S = 12.6\,\text{dBm}$, $f_C = 333.2\,\text{MHz}$, $\delta V_G = 75\,\mu\text{V}$, $f_M = 3\,\text{kHz}$ and $V_G = 649.5\,\text{mV}$.

the Coulomb peaks in this figure was also used to determine δQ from δV_M as discussed in Sec. 4.3.4.

After the modulation frequency and amplitude as well as the matching frequency and varactor voltage were optimized, S_Q was measured as a function of the applied power to port 1 P_{IN}. The measurement is shown in Fig. 40 with the best recorded charge sensitivity $S_Q = 12\,\mu\text{eHz}^{-0.5}$ at an input power of $P_{IN} = -26\,\text{dBm}$. This corresponds to approximately -109 dBm reflected power from the tank circuit to a possible additional low temperature amplifier, when assuming the absolute of the reflection coefficient that can be inferred from Fig. 38 and +32 dBm gain from the BJT amplifier.

Finally, the charge sensitivity was measured as a function of gate voltage with optimized parameters (Fig. 41a). This measurement can be compared to the DC conductance G and the demodulated voltage V_D, that are shown as a function of gate voltage and bias voltage V_B in Fig. 41b,c. The minima in the charge sensitivity are located at the flanks of the Coulomb peaks and the best charge sensitivity $S_Q = 9 \pm 1\,\mu\text{eHz}^{-0.5}$ was measured at $V_G = 635.5\,\text{mV}$. Note that the demodulated voltage in Fig. 41c

shows particularly strong contrast between Coulomb blockade and conductive region for the Coulomb peaks with the best charge sensitivities. While Fig. 41a shows a relatively small gate voltage region around $V_G = 635.5\,\mathrm{mV}$, the gate voltage range in the measurement was much larger in order to find the most suitable Coulomb peak (see Supplementary Information).

The DC measurement in Fig. 41b shows two lines in the DC measurement close to $\pm 1\,\mathrm{mV}$ in bias voltage, that are artefacts from the data acquisition process and not related to the sample behaviour. Apart from these artefacts, Fig. 41b shows a significant conductance within the Coulomb diamonds that can be attributed to co-tunneling processes [111]. These processes require multiple tunnelling events to happen simultaneously, such that the individual probabilities multiply and the processes become very unlikely for large tunnel barriers with low tunneling probability (low transparency) [111]. The presence of co-tunnelling is indicative of highly transparent tunnel barriers and might also explain the conductivity in the diamonds at lower gate voltage from Fig. 14c. For more details about co-tunneling I want to refer the reader to Ref. [111], since those processes are not covered in the theory of Sec. 7. Note also that the assumptions that were made in Ref. [39] to estimate the ideal charge sensitivity do not include co-tunneling effects.

4.4.2 Conclusion

In this section I have demonstrated charge sensing using the silicon nanowire device from Sec. 3.3.1. First the charge sensitivity was optimized with respect to varactor voltage, carrier frequency and the input power. The best charge sensitivity $S_Q = 9 \pm 1\,\mu\mathrm{eHz}^{-0.5}$ was recorded on the flank of a Coulomb peak in a subsequent measurement as a function of gate voltage.

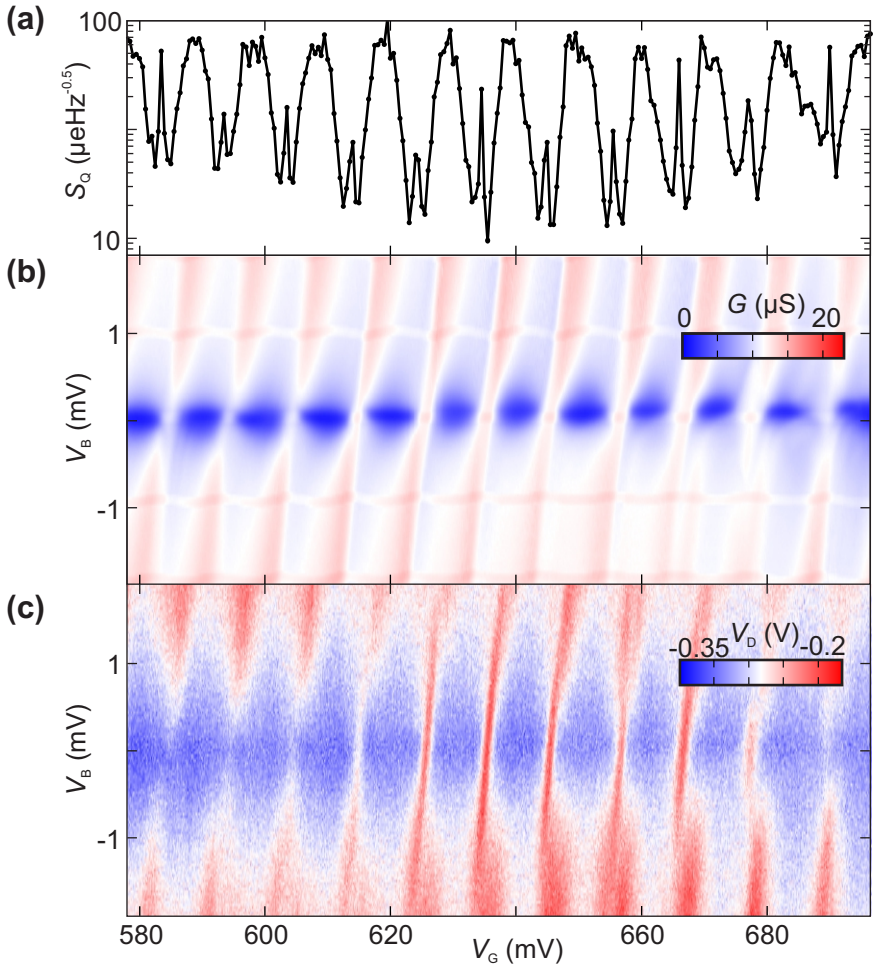

Figure 41: Data from the measurement of the silicon nanowire from Sec. 3.3.1. a) Charge sensitivity S_Q as a function of gate voltage V_G at $V_B = 0$. Other measurement parameters: $P_{IN} = -26\,\mathrm{dBm}$, $V_S = 12.6\,\mathrm{dBm}$, $f_C = 333.2\,\mathrm{MHz}$, $\delta V_G = 75\,\mu\mathrm{V}$ and $f_M = 3\,\mathrm{kHz}$. b) Conductance G as a function of V_G and V_B in the same gate-voltage window as a). c) Demodulated voltage in reflectomentry V_D from a measurement in parallel to b). Other measurement parameters: $P_{IN} = -30\,\mathrm{dBm}$, $V_S = 12.6\,\mathrm{V}$ and $f_C = 333.2\,\mathrm{MHz}$.

To determine whether the charge sensitivity is limited by shot noise or the BJT amplifier, the noise level after reflection can be extracted from the power next to the sideband in any of the sideband experiments by subtracting the amplification in the RF output line. The resulting noise power of $P_N = -178 \pm 1\,\mathrm{dBm}$ at 30 Hz resolution bandwidth corresponds to a noise temperature of $T_N = 3.4 \pm 0.9\,\mathrm{K}$ in agreement with

the specified noise temperature of the BJT amplifier (3.7 K). The sensitivity is therefore limited by the amplifier noise, not the device noise.

Based on the measurements as a function of P_{IN} from Fig. 40, I can estimate whether the charge sensitivity could be improved with the SQUID amplifier assuming it would operate at the increased carrier frequency in this experiment. Considering the estimated threshold for low noise performance of the SQUID amplifier (-127 dBm), the reflected power at $P_{\mathrm{IN}} = -26\,\mathrm{dBm}$ would increase the noise temperature to 6.4 K according to Fig. 29. While this is clearly worse than the noise temperature from the BJT amplifier (3.7 K), there might be a lower input power where the SNR could be improved. This can be calculated by rewriting Eq. 28:

$$S_{\mathrm{Q}} \propto 10^{-\frac{P_{\mathrm{IN}}-|S_{21}|-P_{\mathrm{N}}}{20}} \tag{42}$$

To estimate $P_{\mathrm{N}}(P_{\mathrm{IN}})$, I consider the power law regime of the noise temperature as a function of P_{IN} for $P_{\mathrm{IN}} > -31\,\mathrm{dBm}$ in Fig. 29. An improvement in SNR would then require that $P_{\mathrm{N}}(P_{\mathrm{IN}}) \propto (P_{\mathrm{IN}})^{\xi}$ with $\xi > 1$. Since $T_{\mathrm{N}} \propto P_{\mathrm{N}}$ this corresponds to e.g. one order of magnitude change in T_{N} per 10 dB change in P_{IN} (equivalent to one order of magnitude in P_{IN}). The incline in Fig. 29 is much smaller, such that the sensitivity cannot be improved for lower P_{IN} according to Eq. 42. I therefore conclude that employing the SQUID amplifier would not improve the charge sensitivity at any input power unless the carrier tone can be cancelled, filtering can improve the input power tolerance of the SQUID or the matching can be improved. Another way to improve on the measured charge sensitivity could be an optimized device with tunable tunnel barriers. In such a device it might be possible to find a better trade off between lifetime broadening/co-tunneling and high conductance.

5 Outlook

The results on nanowire transport presented in this thesis contribute to the much bigger effort of developing a generation of transistors that is based on top-down fabricated silicon nanowires. The study of the important transport length scales, e.g. the mean-free path, allowed me to identify the important scattering processes and can be beneficial in future device development. Additionally the work in this thesis stresses the importance of 1D transport, that will have an impact on the device physics of future nanowire transistors if the diameters reach $\sim$ 10 nm.

The presented work also suggests a pathway to top-down fabricated ballistic silicon transistors at cryogenic temperatures. These cryogenic CMOS devices could become crucial for e.g. control electronics in quantum information processing architectures because they could run with very low heat dissipation and be integrated similar to state-of-the-art CMOS devices with a very small footprint. Especially the low temperature measurements on nanowires, that demonstrate transport in the quasi-ballistic limit for the first time in a top-down fabricated silicon nanowire device, suggest that the ballistic regime with minimal energy dissipation could be reached for lower doping densities and/or shorter devices. For large quantum computing architectures this could be a key requirement [20, 19].

Similar silicon nanowires could also be modified as zero dimensional CMOS devices if tunnel barriers can be engineered reproducibly. One possible application would employ reproducible zero dimensional systems as parallel charge pumps that produce a very accurate current when an AC signal is applied [112, 113]. Compared to other charge pumps made from single devices, where the currents are accurate but small, these multi-device charge pumps could increase the output current significantly. Such

a charge pump is highly sought after in the metrology community, where the ampere could be redefined only using the pump frequency and the electron charge. A scalable silicon architecture with many parallel devices could solve the remaining problems because the current could be both accurate and large [37].

The radio-frequency reflectometry experiments presented in this thesis demonstrate charge sensing in a nanowire device with a state-of-the-art charge sensitivity. While the tunnel barriers in this device were not introduced in a reproducible way, other work showed how single-electron transistors can be implemented in similar devices in a more deterministic way using local strain over steps in device height [35]. If this or a similar fabrication technique could be developed for the nanowire devices, it would be possible to build reproducible charge sensing devices that can be integrated in a computing or sensing architecture. Since RF-SET charge sensors are fundamentally limited by shot noise as opposed to the effects from scattering in a diffusive channel that dominate in FETs, it should be possible to outperform FET charge sensors with silicon single electron transistors. In principle, large improvements in charge sensing could also be achieved if reflectometry is carried out on FETs that have reached the ballistic limit [82] – low temperature ballistic nanowire transistors could therefore also be a candidate for charge sensing with superior sensitivity compared to regular FETs.

Applications of RF-reflectometry on a charge sensor include the read-out of qubits after spin-to-charge conversion [49, 114]. To build a quantum information processing architecture from many qubits, it would be beneficial to avoid a dedicated charge sensor and read out the quantum state directly on the qubit via quantum capacitance. In this thesis I have, for the first time, demonstrated sufficient sensitivity for single-shot read-out in this scheme. Crucially the read-out circuit can be attached directly on an already existing contact to the device, such that the read-out electronics have minimal footprint in the qubit layer and the

architecture remains scalable.

While this could have great benefits for the scalability of the qubit layer in a quantum processing architecture, the control and read-out electronics in such a system would have to scale with the qubit number as well. Since it is not realistic to install one refletometry circuit per qubit, the read-out and control of many qubits would require some form of multiplexing using e.g. a 2D array of transistor switches as proposed in Ref. [19, 115]. Since the qubit and control layer of a large quantum processing architecture will most likely be located in a dilution refrigerator, there will only be a very tight thermal budget per qubit for read-out and control electronics. An architecture made from optimized ballistic silicon nanowire transistor switches and the reflectometry read-out circuit could combine the desired sensitive and fast read-out with minimal footprint and heating.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Newsletter*, vol. 20, no. 3, pp. 33–35, 2006.

[2] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI design: A systems perspective*. Addison-Wesley Publishing Co., 1985.

[3] M. M. Waldrop, "The chips are down for Moore's law," *Nature*, vol. 530, pp. 144–147, feb 2016.

[4] M. Pierre, R. Wacquez, X. Jehl, M. Sanquer, M. Vinet, and O. Cueto, "Single-donor ionization energies in a nanoscale CMOS channel.," *Nature nanotechnology*, vol. 5, pp. 133–7, feb 2010.

[5] J. Colless, a. Mahoney, J. Hornibrook, a. Doherty, H. Lu, a. Gossard, and D. Reilly, "Dispersive Readout of a Few-Electron Double Quantum Dot with Fast rf Gate Sensors," *Physical Review Letters*, vol. 110, p. 046805, jan 2013.

[6] D. J. Reilly, C. M. Marcus, M. P. Hanson, and a. C. Gossard, "Fast single-charge sensing with a rf quantum point contact," *Applied Physics Letters*, vol. 91, no. 16, p. 162101, 2007.

[7] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310–316, nov 2011.

[8] Y. M. Niquet, A. Lherbier, N. H. Quang, M. V. Fernández-Serra, X. Blase, and C. Delerue, "Electronic structure of semiconductor nanowires," *Physical Review B - Condensed Matter and Materials Physics*, vol. 73, no. 16, pp. 1–13, 2006.

[9] A. T. Tilke, F. C. Simmel, H. Lorenz, R. H. Blick, and J. P. Kotthaus, "Quantum interference in a one-dimensional silicon nanowire," *Physical Review B*, vol. 68, p. 075311, aug 2003.

[10] P.-Y. Yang, L. Y. Wang, Y.-W. Hsu, and J.-J. Lin, "Universal conductance fluctuations in indium tin oxide nanowires," *Physical Review B*, vol. 85, p. 085423, feb 2012.

[11] J. M. Luttinger, "An Exactly Soluble Model of a Many-Fermion System," *Journal of Mathematical Physics*, vol. 4, no. 9, p. 1154, 1963.

[12] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, "Signatures of Majorana Fermions in Hybrid Superconductor-Semiconductor Nanowire Devices," *Science*, vol. 336, pp. 1003–1007, may 2012.

[13] J. Kammhuber, M. C. Cassidy, H. Zhang, Ö. Gül, F. Pei, M. W. A. de Moor, B. Nijholt, K. Watanabe, T. Taniguchi, D. Car, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, "Conductance Quantization at Zero Magnetic Field in InSb Nanowires," *Nano Letters*, vol. 16, pp. 3482–3486, jun 2016.

[14] G. Barak, H. Steinberg, L. N. Pfeiffer, K. W. West, L. Glazman, F. von Oppen, and A. Yacoby, "Interacting electrons in one dimension beyond the Luttinger-liquid limit," *Nature Physics*, vol. 6, pp. 489–493, jul 2010.

[15] V. P. Georgiev, M. M. Mirza, A.-I. Dochioiu, F.-A. Lema, S. M. Amoroso, E. Towie, C. Riddet, D. A. MacLaren, A. Asenov, and D. J. Paul, "Experimental and simulation study of a high current 1D silicon nanowire transistor using heavily doped channels," in *2016 IEEE Nanotechnology Materials and Devices Conference (NMDC)*, vol. 99, pp. 1–3, IEEE, oct 2016.

[16] M. T. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess, "Donor deactivation in silicon nanostructures.," *Nature nanotechnology*, vol. 4, pp. 103–7, feb 2009.

[17] C. Busche, L. Vilà-Nadal, J. Yan, H. N. Miras, D.-l. Long, V. P. Georgiev, A. Asenov, R. H. Pedersen, N. Gadegaard, M. M. Mirza, D. J. Paul, J. M. Poblet, and L. Cronin, "Design and fabrication of memory devices based on nanoscale polyoxometalate clusters," *Nature*, vol. 515, pp. 545–549, nov 2014.

[18] Y. S. Jung, W. Jung, H. L. Tuller, and C. A. Ross, "Nanowire Conductive Polymer Gas Sensor Patterned Using Self-Assembled Block Copolymer Lithography," *Nano Letters*, vol. 8, pp. 3776–3780, nov 2008.

[19] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak, "Silicon CMOS architecture for a spin-based quantum computer," *Nature Communications*, vol. 8, p. 1766, dec 2017.

[20] H. Bluhm, S. Foletti, I. Neder, M. Rudner, D. Mahalu, V. Umansky, and A. Yacoby, "Dephasing time of GaAs electron-spin qubits coupled to a nuclear bath exceeding 200μs," *Nat Phys*, vol. 7, no. 2, pp. 109–113, 2011.

[21] T. Ihn, *Semiconductor Nanostructures*. Oxford University Press, 2009.

[22] T. A. Fulton and G. J. Dolan, "Observation of single-electron charging effects in small tunnel junctions," *Physical Review Letters*, vol. 59, no. 1, pp. 109–112, 1987.

[23] U. Meirav, M. A. Kastner, and S. J. Wind, "Single-electron charging and periodic conductance resonances in GaAs nanostructures," *Physical Review Letters*, vol. 65, pp. 771–774, aug 1990.

[24] H. Ishikuro and T. Hiramoto, "Quantum mechanical effects in the silicon quantum dot in a single-electron transistor," *Applied Physics Letters*, vol. 71, no. 25, p. 3691, 1997.

[25] C. Stampfer, E. Schurtenberger, F. Molitor, J. Güttinger, T. Ihn, and K. Ensslin, "Tunable Graphene Single Electron Transistor," *Nano Letters*, vol. 8, pp. 2378–2383, aug 2008.

[26] M. Bockrath, "Single-Electron Transport in Ropes of Carbon Nanotubes," *Science*, vol. 275, pp. 1922–1925, mar 1997.

[27] M. Fuechsle, J. a. Miwa, S. Mahapatra, H. Ryu, S. Lee, O. Warschkow, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons, "A single-atom transistor," *Nature Nanotechnology*, vol. 7, pp. 242–246, apr 2012.

[28] S. J. Shin, C. S. Jung, B. J. Park, T. K. Yoon, J. J. Lee, S. J. Kim, J. B. Choi, Y. Takahashi, and D. G. Hasko, "Si-based ultrasmall multiswitching single-electron transistor operating at room-temperature," *Applied Physics Letters*, vol. 97, no. 10, p. 103101, 2010.

[29] R. Lavieville, S. Barraud, A. Corna, X. Jehl, M. Sanquer, and M. Vinet, "350K Operating Silicon Nanowire Single Electron / Hole Transistors Scaled Down to 3.4 nm Diameter and 10 nm Gate Length," *IEEE conference paper*, pp. 9–12, 2015.

[30] P. Puczkarski, P. Gehring, C. S. Lau, J. Liu, A. Ardavan, J. H. Warner, G. A. D. Briggs, and J. A. Mol, "Three-terminal graphene single-electron transistor fabricated using feedback-controlled electroburning," *Applied Physics Letters*, vol. 107, p. 133105, sep 2015.

[31] G. C. Tettamanzi, R. Wacquez, and S. Rogge, "Charge pumping through a single donor atom," *New Journal of Physics*, vol. 16, 2014.

[32] A. K. Geim, T. J. Foster, A. Nogaret, N. Mori, P. J. McDonnell, N. L. Scala, P. C. Main, and L. Eaves, "Resonant tunneling through donor molecules," *Physical Review B*, vol. 50, no. 11, pp. 8074–8077, 1994.

[33] L. E. Calvet, J. P. Snyder, and W. Wernsdorfer, "Excited-state spectroscopy of single Pt atoms in Si," *Physical Review B - Condensed Matter and Materials Physics*, vol. 78, no. 19, pp. 1–7, 2008.

[34] E. Janzén, R. Stedman, G. Grossmann, and H. G. Grimmeiss, "High-resolution studies of sulfur- and selenium-related donor centers in silicon," *Physical Review B*, vol. 29, pp. 1907–1918, feb 1984.

[35] S. J. Shin, J. J. Lee, H. J. Kang, J. B. Choi, S. R. E. Yang, Y. Takahashi, and D. G. Hasko, "Room-temperature charge stability modulated by quantum effects in a nanoscale silicon island," *Nano Letters*, vol. 11, no. 4, pp. 1591–1597, 2011.

[36] G. Yamahata, K. Nishiguchi, and A. Fujiwara, "Gigahertz single-trap electron pumps in silicon," *Nature Communications*, vol. 5, pp. 1–7, 2014.

[37] F. J. Schupp, "Single-electron devices in silicon," *Materials Science and Technology*, vol. 33, pp. 944–962, may 2017.

[38] N. M. Zimmerman and M. W. Keller, "Electrical metrology with single electrons," *Measurement Science and Technology*, vol. 14, pp. 1237–1242, aug 2003.

[39] A. N. Korotkov and M. A. Paalanen, "Charge sensitivity of radio frequency single-electron transistor," *Applied Physics Letters*, vol. 74, pp. 4052–4054, jun 1999.

[40] S. J. Angus, A. J. Ferguson, A. S. Dzurak, and R. G. Clark, "A silicon radio-frequency single electron transistor," *Applied Physics Letters*, vol. 92, no. 11, p. 112103, 2008.

[41] I. Ahmed, J. A. Haigh, S. Schaal, S. Barraud, Y. Zhu, C.-m. Lee, M. Amado, J. W. A. Robinson, A. Rossi, J. J. L. Morton, and M. F. Gonzalez-Zalba, "Radio-frequency capacitive gate-based sensing," *ArXiv*, pp. 1–8, jan 2018.

[42] R. J. Schoelkopf, "The Radio-Frequency Single-Electron Transistor (RF-SET): A Fast and Ultrasensitive Electrometer," *Science*, vol. 280, pp. 1238–1242, may 1998.

[43] M. Jung, M. D. Schroer, K. D. Petersson, and J. R. Petta, "Radio frequency charge sensing in InAs nanowire double quantum dots," *Applied Physics Letters*, vol. 100, p. 253508, jun 2012.

[44] M. F. Gonzalez-Zalba, S. Barraud, a. J. Ferguson, and a. C. Betz, "Probing the limits of gate-based charge sensing," *Nature Communications*, vol. 6, p. 6084, dec 2015.

[45] A. M. Tyryshkin, J. J. L. Morton, S. C. Benjamin, A. Ardavan, G. A. D. Briggs, J. W. Ager, and S. A. Lyon, "Coherence of spin qubits in silicon," *Journal of Physics: Condensed Matter*, vol. 18, pp. S783–S794, may 2006.

[46] M. C. Cassidy, A. S. Dzurak, R. G. Clark, K. D. Petersson, I. Farrer, D. A. Ritchie, and C. G. Smith, "Single shot charge detection using a radio-frequency quantum point contact," *Applied Physics Letters*, vol. 91, no. 22, pp. 6–9, 2007.

[47] K. D. Petersson, C. G. Smith, D. Anderson, P. Atkinson, G. A. C. Jones, and D. A. Ritchie, "Charge and spin state readout of a double quantum dot coupled to a resonator.," *Nano letters*, vol. 10, pp. 2789–93, aug 2010.

[48] R. Mizuta, R. M. Otxoa, A. C. Betz, and M. F. Gonzalez-Zalba, "Quantum and tunneling capacitance in charge and spin qubits," *Physical Review B*, vol. 95, p. 045414, jan 2017.

[49] A. C. Betz, R. Wacquez, M. Vinet, X. Jehl, A. L. Saraiva, M. Sanquer, A. J. Ferguson, and M. F. Gonzalez-Zalba, "Dispersively Detected Pauli Spin-Blockade in a Silicon Nanowire Field-Effect Transistor," *Nano Letters*, p. 150615160818000, 2015.

[50] N. Ares, F. J. Schupp, A. Mavalankar, G. Rogers, J. Griffiths, G. A. C. Jones, I. Farrer, D. A. Ritchie, C. G. Smith, A. Cottet, G. A. D. Briggs, and E. A. Laird, "Sensitive Radio-Frequency Measurements of a Quantum Dot by Tuning to Perfect Impedance Matching," *Physical Review Applied*, vol. 5, p. 034011, mar 2016.

[51] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature*, vol. 430, pp. 61–65, 2004.

[52] M. M. Mirza, F. J. Schupp, J. A. Mol, D. A. MacLaren, G. A. D. Briggs, and D. J. Paul, "One dimensional transport in silicon nanowire junction-less field effect transistors," *Scientific Reports*, vol. 7, p. 3004, dec 2017.

[53] W. Kern, "The Evolution of Silicon Wafer Cleaning Technology," *Journal of The Electrochemical Society*, vol. 137, no. 6, p. 1887, 1990.

[54] M. M. Mirza, *Nanofabrication of Silicon Nanowires and Nanoelectronic Transistors*. PhD thesis, University of Glasgow, 2015.

[55] M. M. Mirza, H. Zhou, P. Velha, X. Li, K. E. Docherty, A. Samarelli, G. Ternent, and D. J. Paul, "Nanofabrication of high aspect ratio (50:1) sub-10 nm silicon nanowires using inductively coupled plasma etching," *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 30, no. 6, p. 06FF02, 2012.

[56] M. M. Mirza, D. a. MacLaren, A. Samarelli, B. M. Holmes, H. Zhou, S. Thoms, D. MacIntyre, and D. J. Paul, "Determining the Electronic Performance Limitations in Top-Down-Fabricated Si Nanowires with Mean Widths Down to 4 nm.," *Nano letters*, vol. 14, pp. 6056–60, nov 2014.

[57] F. Giazotto, T. T. Heikkilä, A. Luukanen, A. M. Savin, and J. P. Pekola, "Opportunities for mesoscopics in thermometry and refrigeration: Physics and applications," *Reviews of Modern Physics*, vol. 78, pp. 217–274, mar 2006.

[58] N. Ares, F. J. Schupp, A. Mavalankar, G. Rogers, J. Griffiths, G. A. C. Jones, I. Farrer, D. A. Ritchie, C. G. Smith, A. Cottet, G. A. D. Briggs, and E. A. Laird, "Sensitive Radio-Frequency Measurements of a Quantum Dot by Tuning to Perfect Impedance Matching: Supplementary Information," in *SpringerReference*, vol. 2, pp. 1–4, Berlin/Heidelberg: Springer-Verlag, 2016.

[59] "`http://www.ez-squid.de/`."

[60] S. M. Goodnick, *Transport in Nanostructures*. Cambridge University Press, 2 ed., 2008.

[61] S. Chuang, Q. Gao, R. Kapadia, A. C. Ford, J. Guo, and A. Javey, "Ballistic InAs nanowire transistors," *Nano Letters*, vol. 13, no. 2, pp. 555–558, 2013.

[62] D. Liang, M. R. Sakr, and X. P. A. Gao, "One-Dimensional Weak Localization of Electrons in a Single InAs Nanowire," *Nano Letters*, vol. 9, pp. 1709–1712, apr 2009.

[63] M. T. Elm, P. Uredat, J. Binder, L. Ostheim, M. Schäfer, P. Hille, J. Müßener, J. Schörmann, M. Eickhoff, and P. J. Klar, "Doping-Induced Universal Conductance Fluctuations in GaN Nanowires," *Nano Letters*, vol. 15, pp. 7822–7828, dec 2015.

[64] A. A. M. Staring, H. van Houten, C. W. J. Beenakker, and C. T. Foxon, "Coulomb-blockade oscillations in disordered quantum wires," *Physical Review B*, vol. 45, pp. 9222–9236, apr 1992.

[65] D. K. Schroder, *Semiconductor Material and Device Characterization*, vol. 44. Hoboken, NJ, USA: John Wiley & Sons, Inc., oct 2005.

[66] B. L. Altshuler, a. G. Aronov, and D. E. Khmelnitsky, "Effects of electron-electron collisions with small energy transfers on quantum localisation," *Journal of Physics C: Solid State Physics*, vol. 15, no. 36, pp. 7367–7386, 2000.

[67] F. J. Rueß, B. Weber, K. E. J. Goh, O. Klochan, A. R. Hamilton, and M. Y. Simmons, "One-dimensional conduction properties of highly phosphorus-doped planar nanowires patterned by scanning probe microscopy," *Physical Review B*, vol. 76, p. 085403, aug 2007.

[68] M. Grundmann, *The Physics of Semiconductors*. Graduate Texts in Physics, Berlin, Heidelberg: Springer Berlin Heidelberg, 2010.

[69] E. Prati, K. Kumagai, M. Hori, and T. Shinada, "Band transport across a chain of dopant sites in silicon over micron distances and high temperatures," *Scientific Reports*, vol. 6, pp. 1–8, 2016.

[70] A. L. Efros and B. I. Shklovskii, "Coulomb gap and low temperature conductivity of disordered systems," *Journal of Physics C: Solid State Physics*, vol. 8, pp. L49–L51, feb 1975.

[71] A. Efros, N. Van Lien, and B. Shklovskii, "Variable range hopping in doped crystalline semiconductors," *Solid State Communications*, vol. 32, pp. 851–854, dec 1979.

[72] J. Voit, "One-dimensional Fermi liquids," *Reports on Progress in Physics*, vol. 58, pp. 977–1116, sep 1995.

[73] P. L. McEuen, M. Bockrath, D. H. Cobden, J. Lu, A. G. Rinzler, R. E. Smalley, and L. Balents, "Luttinger-liquid behavior in carbon nanotubes," *Nature*, vol. 397, pp. 598–601, feb 1999.

[74] L. Venkataraman, Y. S. Hong, and P. Kim, "Electron Transport in a Multichannel One-Dimensional Conductor: Molybdenum Selenide Nanowires," *Physical Review Letters*, vol. 96, p. 076601, feb 2006.

[75] A. Rahman and M. K. Sanyal, "Bias dependent crossover from variable range hopping to power law characteristics in the resistivity of polymer nanowires," *Journal of Physics: Condensed Matter*, vol. 22, p. 175301, may 2010.

[76] C. Mora, R. Egger, and A. Altland, "From Luttinger liquid to Altshuler-Aronov anomaly in multi-channel quantum wires," *Physical Review B*, vol. 75, p. 035310, jan 2007.

[77] E. G. Mishchenko, A. V. Andreev, and L. I. Glazman, "Zero-Bias Anomaly in Disordered Wires," *Physical Review Letters*, vol. 87, p. 246801, nov 2001.

[78] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, *Mesoscopic Electron Transport*. No. 1, Dordrecht: Springer Netherlands, 1 ed., 1997.

[79] H. Van Houten, C. W. J. Beenakker, and A. A. M. Staring, "Coulomb-Blockade Oscillations in Semiconductor Nanostructures," in *Single Charge Tunneling: Coulomb Blockade Phenomena In Nanostructures*, pp. 167–216, Springer, Boston, MA, 1992.

[80] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, "Spins in few-electron quantum dots," *Reviews of Modern Physics*, vol. 79, pp. 1217–1265, oct 2007.

[81] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. L. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson, "Silicon quantum electronics," *Reviews of Modern Physics*, vol. 85, pp. 961–1019, jul 2013.

[82] M. Devoret and R. Schoelkopf, "Amplifying quantum signals with the single-electron transistor," *Nature*, vol. 406, no. 6799, pp. 1039–46, 2000.

[83] J. Knoch, "One-dimensional field-effect transistors," in *One-Dimensional Nanostructures: Principles and Applications*, ch. 24, pp. 503–513, New York: John Wiley and Sons, Incorporated, 1 ed., 2012.

[84] C.-H. Jan, U. Bhattacharya, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *2012 International Electron Devices Meeting*, pp. 3.1.1–3.1.4, IEEE, dec 2012.

[85] D. J. Paul, J. R. A. Cleaver, H. Ahmed, and T. E. Whall, "Coulomb blockade in silicon based structures at temperatures up to 50 K," *Applied Physics Letters*, vol. 63, pp. 631–632, aug 1993.

[86] P. A. Lee and T. V. Ramakrishnan, "Disordered electronic systems," *Reviews of Modern Physics*, vol. 57, pp. 287–337, apr 1985.

[87] F. Liu, M. Bao, K. L. Wang, C. Li, B. Lei, and C. Zhou, "One-dimensional transport of In2O3 nanowires," *Applied Physics Letters*, vol. 86, p. 213101, may 2005.

[88] L. Bartosch and P. Kopietz, "Zero bias anomaly in the density of states of low-dimensional metals," *The European Physical Journal B - Condensed Matter*, vol. 28, pp. 29–36, jul 2002.

[89] S. Kar, C. Soldano, L. Chen, S. Talapatra, R. Vajtai, S. Nayak, and P. M. Ajayan, "Luttinger Liquid to AltshulerAronov Transition in Disordered, Many-Channel Carbon Nanotubes," *ACS Nano*, vol. 3, pp. 207–212, jan 2009.

[90] M. D. Schroer, M. Jung, K. D. Petersson, and J. R. Petta, "Radio Frequency Charge Parity Meter," *Physical Review Letters*, vol. 109, p. 166804, oct 2012.

[91] O. M. Auslaender, "Spin-Charge Separation and Localization in One Dimension," *Science*, vol. 308, pp. 88–92, apr 2005.

[92] D. P. DiVincenzo and IBM, "The Physical Implementation of Quantum Computation," *Progress of Physics*, vol. 48, pp. 771–783, feb 2000.

[93] M. J. Biercuk, N. Mason, J. Martin, A. Yacoby, and C. M. Marcus, "Anomalous Conductance Quantization in Carbon Nanotubes," *Physical Review Letters*, vol. 94, p. 026801, jan 2005.

[94] S. Heedt, W. Prost, J. Schubert, D. Grützmacher, and T. Schäpers, "Ballistic Transport and Exchange Interaction in InAs Nanowire Quantum Point Contacts," *Nano Letters*, vol. 16, pp. 3116–3123, may 2016.

[95] M. Oksanen, A. Uppstu, A. Laitinen, D. J. Cox, M. F. Craciun, S. Russo, A. Harju, and P. Hakonen, "Single-mode and multimode Fabry-Pérot interference in suspended graphene," *Physical Review B*, vol. 89, p. 121414, mar 2014.

[96] F. Vigneau, Z. Zeng, W. Escoffier, P. Caroff, R. Leturcq, Y.-M. Niquet, B. Raquet, and M. Goiran, "Anisotropic transport properties of quasiballistic InAs nanowires under high magnetic field," *Physical Review B*, vol. 97, p. 125308, mar 2018.

[97] D. Pozar, *Microwave Engineering Fourth Edition*. John Wiley and Sons, Incorporated, 2005.

[98] H. K. Olsson and T. Claeson, "Low-noise Josephson parametric amplification and oscillations at 9 GHz," *Journal of Applied Physics*, vol. 64, pp. 5234–5243, nov 1988.

[99] J. Stehlik, Y. Y. Liu, C. M. Quintana, C. Eichler, T. R. Hartke, and J. R. Petta, "Fast charge sensing of a cavity-coupled double quantum dot using a Josephson parametric amplifier," *Physical Review Applied*, vol. 4, no. 1, pp. 1–10, 2015.

[100] C. Macklin, K. O'Brien, D. Hover, M. E. Schwartz, V. Bolkhovsky, X. Zhang, W. D. Oliver, and I. Siddiqi, "A near-quantum-limited Josephson traveling-wave parametric amplifier," *Science*, vol. 350, pp. 307–310, oct 2015.

[101] M. Mück and R. McDermott, "Radio-frequency amplifiers based on dc SQUIDs," *Superconductor Science and Technology*, vol. 23, p. 093001, sep 2010.

[102] V. Vesterinen, O.-p. Saira, I. Räisänen, M. Möttönen, L. Grönberg, J. Pekola, and J. Hassel, "Lumped-element Josephson parametric amplifier at 650 MHz for nano-calorimeter readout," *Superconductor Science and Technology*, vol. 30, p. 085001, aug 2017.

[103] B. D. Josephson, "The Discovery of Tunneling Supercurrents," *Science*, vol. 184, pp. 527–530, may 1974.

[104] B. Josephson, "Possible new effects in superconductive tunnelling," *Physics Letters*, vol. 1, pp. 251–253, jul 1962.

[105] J. Clarke and A. I. Braginski, *The SQUID Handbook*. Weinheim, FRG: Wiley-VCH Verlag GmbH & Co. KGaA, may 2005.

[106] C. D. Tesche and J. Clarke, "dc SQUID: Noise and optimization," *Journal of Low Temperature Physics*, vol. 29, pp. 301–331, nov 1977.

[107] H. Brenning, S. Kafanov, T. Duty, S. Kubatkin, and P. Delsing, "An ultrasensitive radio-frequency single-electron transistor working up to 4.2 K," *Journal of Applied Physics*, vol. 100, no. 11, 2006.

[108] B. Schmidt and M. Mück, "Microstrip direct current superconducting quantum interference device radio frequency amplifier: Noise data," *Applied Physics Letters*, vol. 100, p. 152601, apr 2012.

[109] M. Mück, J. B. Kycia, and J. Clarke, "Superconducting quantum interference device as a near-quantum-limited amplifier at 0.5 GHz," *Applied Physics Letters*, vol. 78, pp. 967–969, feb 2001.

[110] C. Barthel, D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Rapid Single-Shot Measurement of a Singlet-Triplet Qubit," *Physical Review Letters*, vol. 103, p. 160503, oct 2009.

[111] S. De Franceschi, S. Sasaki, J. M. Elzerman, W. G. Van Der Wiel, S. Tarucha, and L. P. Kouwenhoven, "Electron cotunneling in a semiconductor quantum dot," *Physical Review Letters*, vol. 86, no. 5, pp. 878–881, 2001.

[112] X. Jehl, B. Voisin, T. Charron, P. Clapera, S. Ray, B. Roche, M. Sanquer, S. Djordjevic, L. Devoille, R. Wacquez, and M. Vinet, "Hybrid Metal-Semiconductor Electron Pump for Quantum Metrology," *Physical Review X*, vol. 3, p. 021012, may 2013.

[113] B. Kaestner, V. Kashcheyevs, S. Amakawa, M. D. Blumenthal, L. Li, T. J. B. M. Janssen, G. Hein, K. Pierz, T. Weimann, U. Siegner, and H. W. Schumacher, "Single-parameter nonadiabatic quantized charge pumping," *Physical Review B*, vol. 77, p. 153301, apr 2008.

[114] M. Urdampilleta, A. Chatterjee, C. C. Lo, T. Kobayashi, J. Mansir, S. Barraud, A. C. Betz, S. Rogge, M. F. Gonzalez-Zalba, and J. J. L. Morton, "Charge Dynamics and Spin Blockade in a Hybrid Double Quantum Dot in Silicon," *Physical Review X*, vol. 5, p. 031024, aug 2015.

[115] S. Schaal, S. Barraud, J. J. L. Morton, and M. F. Gonzalez-Zalba, "Conditional dispersive readout of a CMOS quantum dot via an integrated transistor circuit," *ArXiv*, aug 2017.

Appendix

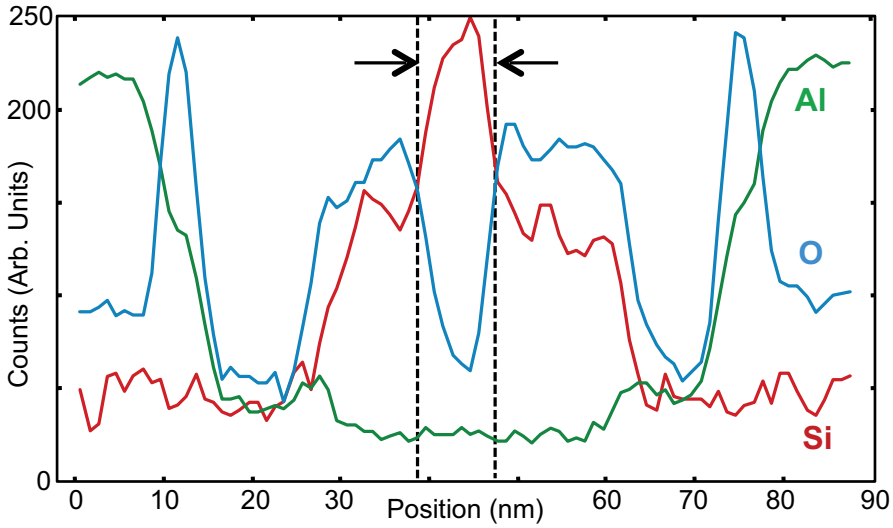

Figure 42: Line cut from the EELS measurement in TEM as indicated by the white frame in the inset of Fig. 8.

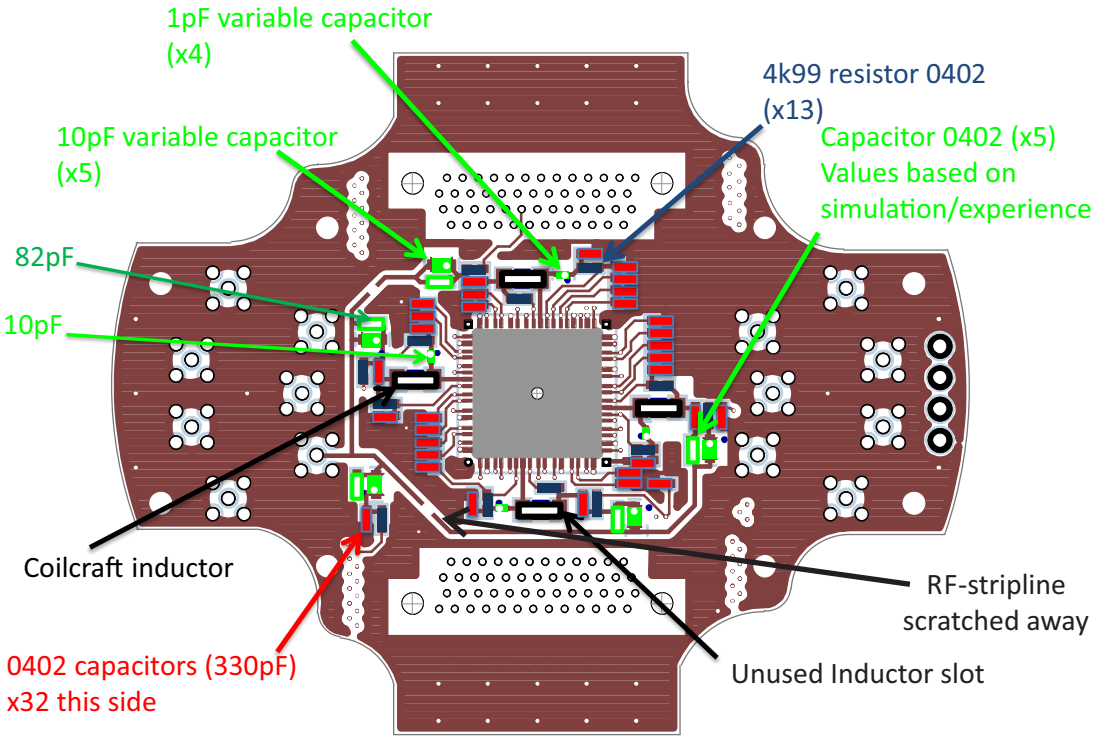

Figure 43: Layout of the sample board (topside). The sample is placed in the grey area in the middle and 3 of the 4 parallel RF circuits in the design have been disconnected by scratching the stripline for the experiments.

Component	Supplier	Part Number
PCB board	Easy circuits	custom design
Nano-D connector	Airborne	NH-2E2-051-325-TH00
SMP launcher	Fairview	SC5335
4-pin header	TE connectivity	826926-4
100 kΩ resistor	Susumu	RR0510P-104-D
4.99 kΩ resistor	Susumu	RR0510P-4991-D
300 pF capacitor	TDK cooperation	CGA2B2C0G1H331J050BA
0.033 µF capacitor	TDK cooperation	CGA4J2C0G1H333J125AD
82 pF capacitor	Vishay	VJ0402A series
10 pF varactor	Macom	MA46H204-1056
1 pF varactor	Macom	MA46H120
Inductors	Coilcraft	1206CS series

Table 2: List of components on the sample board.

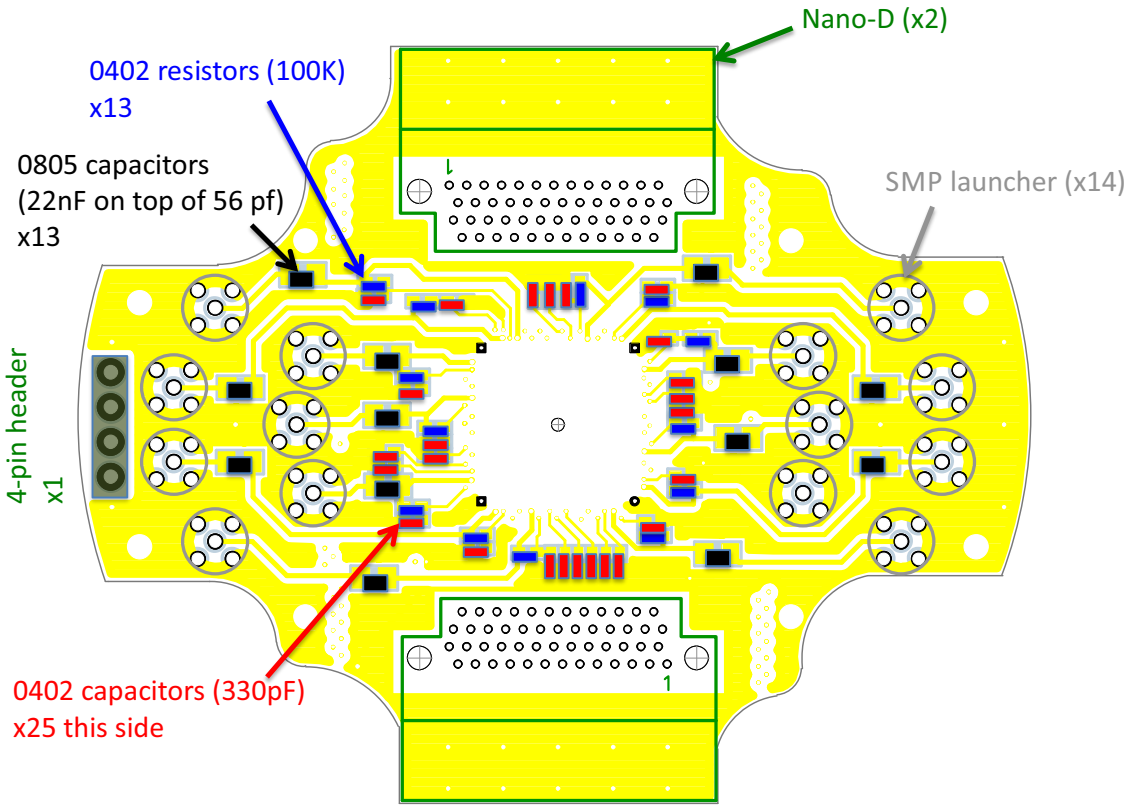

Figure 44: Layout of the sample board (backside).

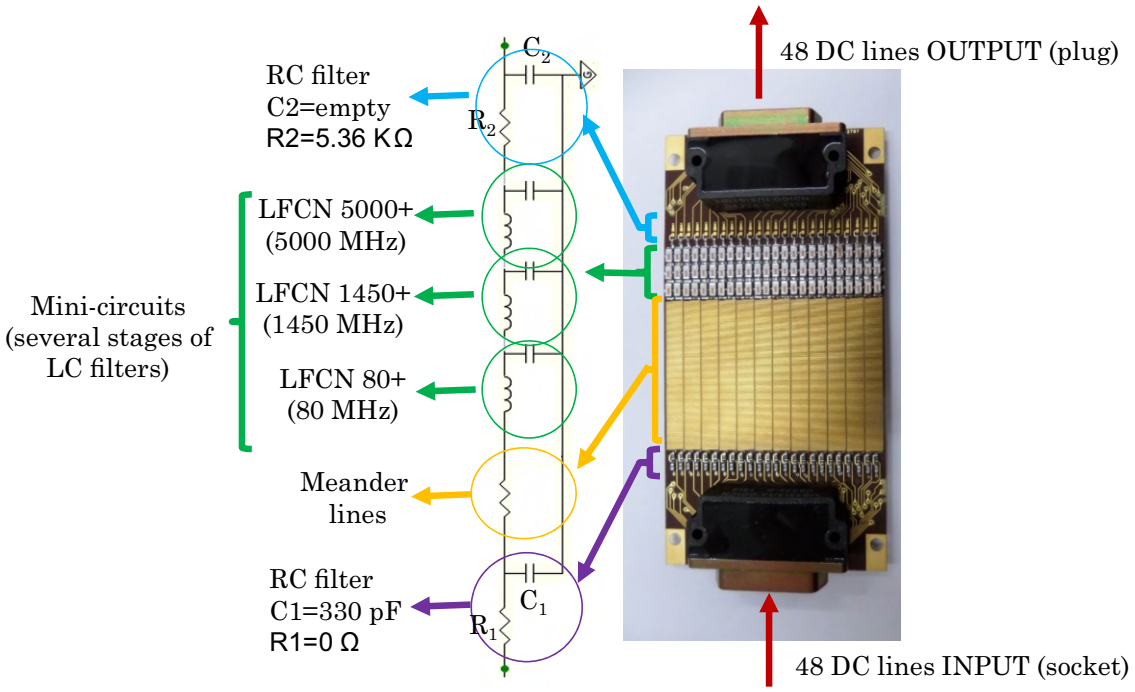

Figure 45: RC-filter for DC wires on the mixing chamber stage of the dilution refrigerator.

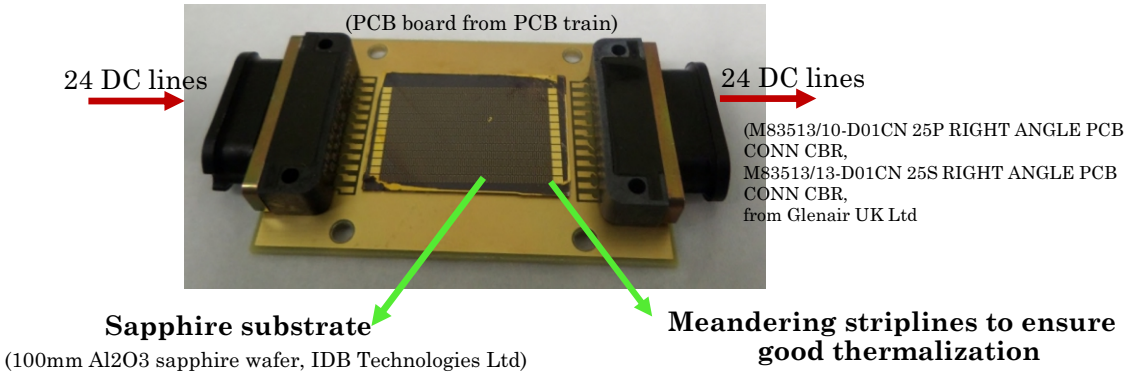

Figure 46: Sapphire heatsink for the DC wires on the mixing chamber stage of the dilution refrigerator. The shown box is closed and screwed to the mixing chamber plate for optimal thermal connection. The sapphire wafer is glued to the box using silver paste.

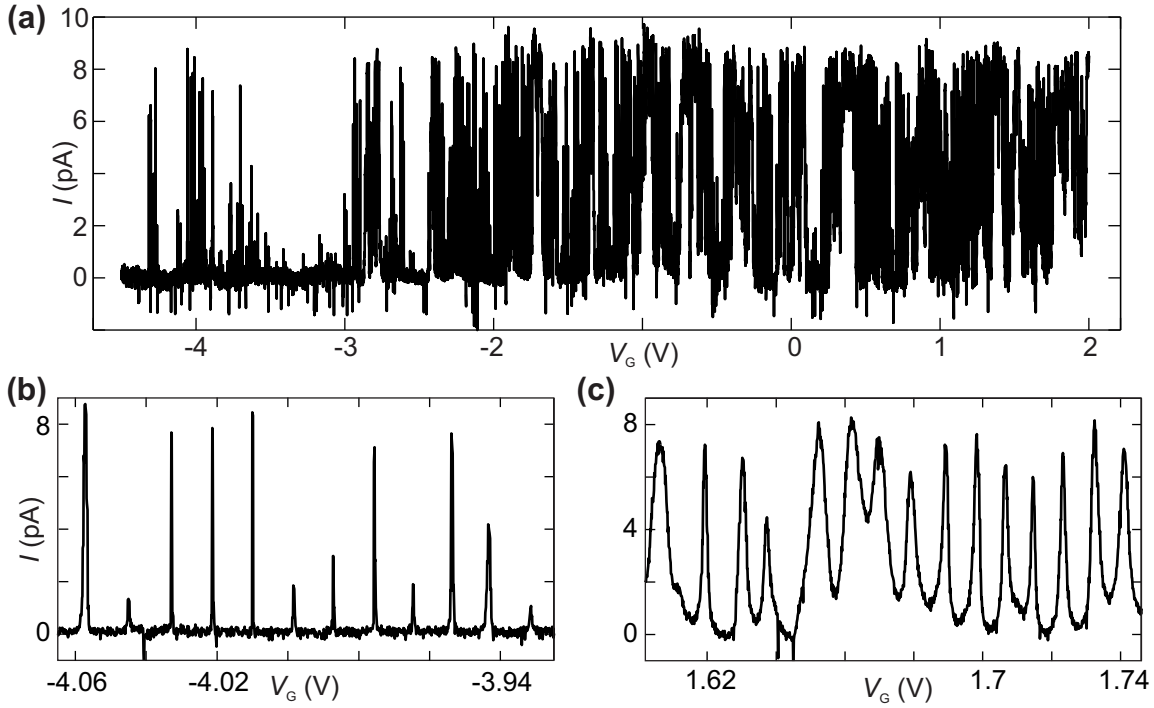

Figure 47: a) Entire measurement of the current I as a function of gate voltage V_G from Sec. 3.3.1. b),c) Zoom into two gate regions.

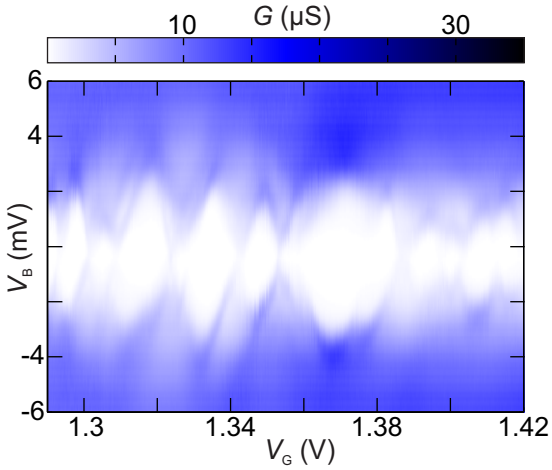

Figure 48: Conductance G as a function of bias voltage V_B and gate voltage V_G in the low gate region from device B in Sec. 3.3.3.

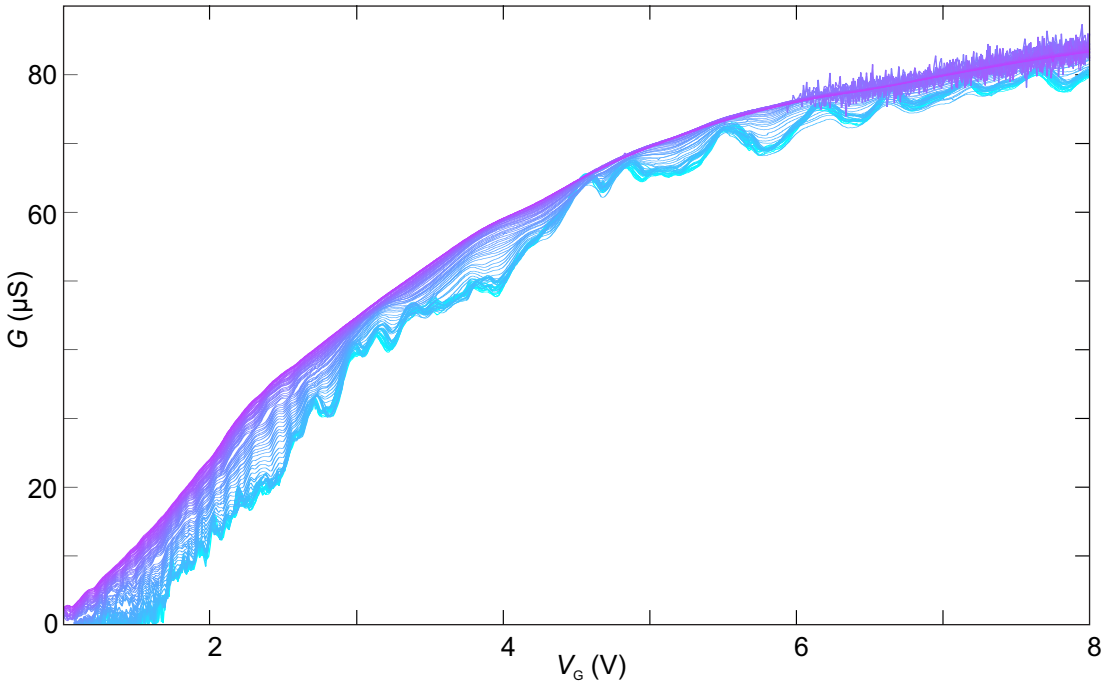

Figure 49: Conductance G as a function of gate voltage V_G at all measured temperatures from 12 mK to 28 K (blue is 12 mK, purple is 28 K). Four traces are shown in Fig. 15. The noise at high temperatures and gate voltages is due to saturation of the amplifier in the measurement and not the device.

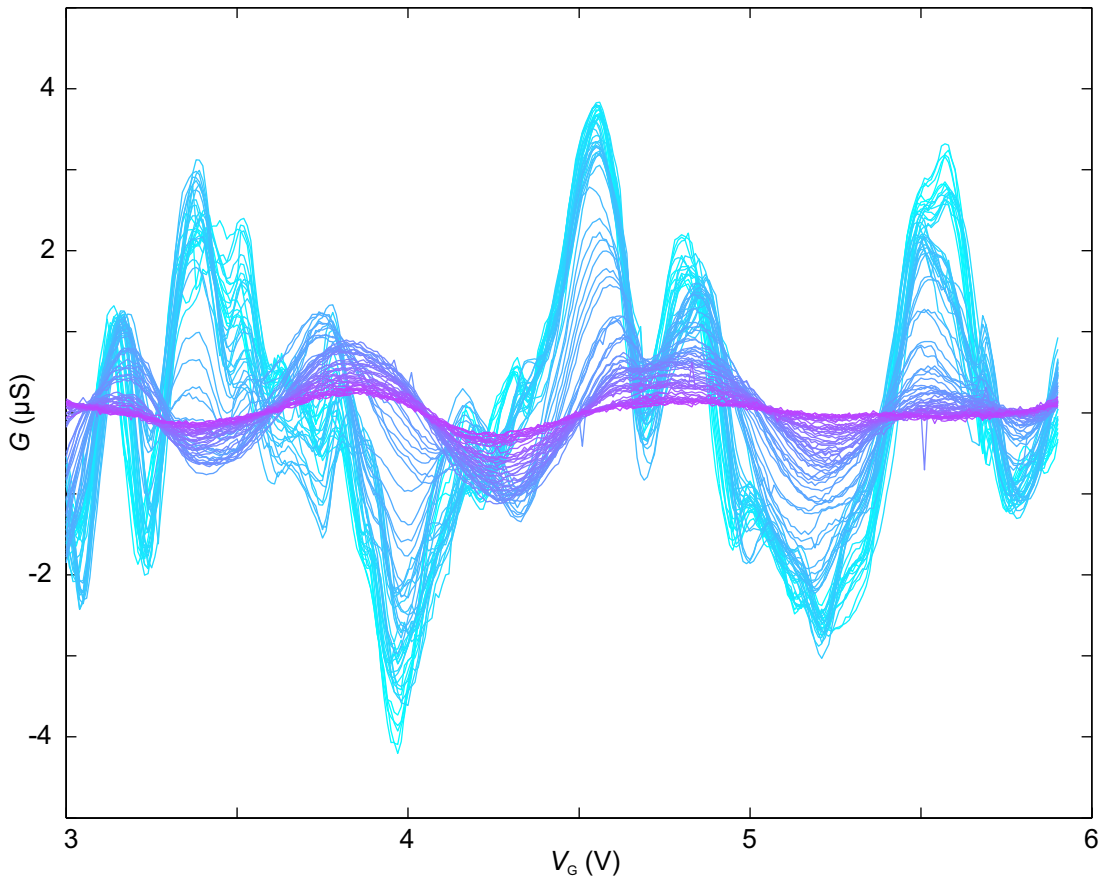

Figure 50: Conductance G as a function of gate voltage V_G at all measured temperatures from 12 mK to 28 K (blue is 12 mK, purple is 28 K) after a 2nd order polynomial fit was subtracted to isolate the conductance fluctuations.

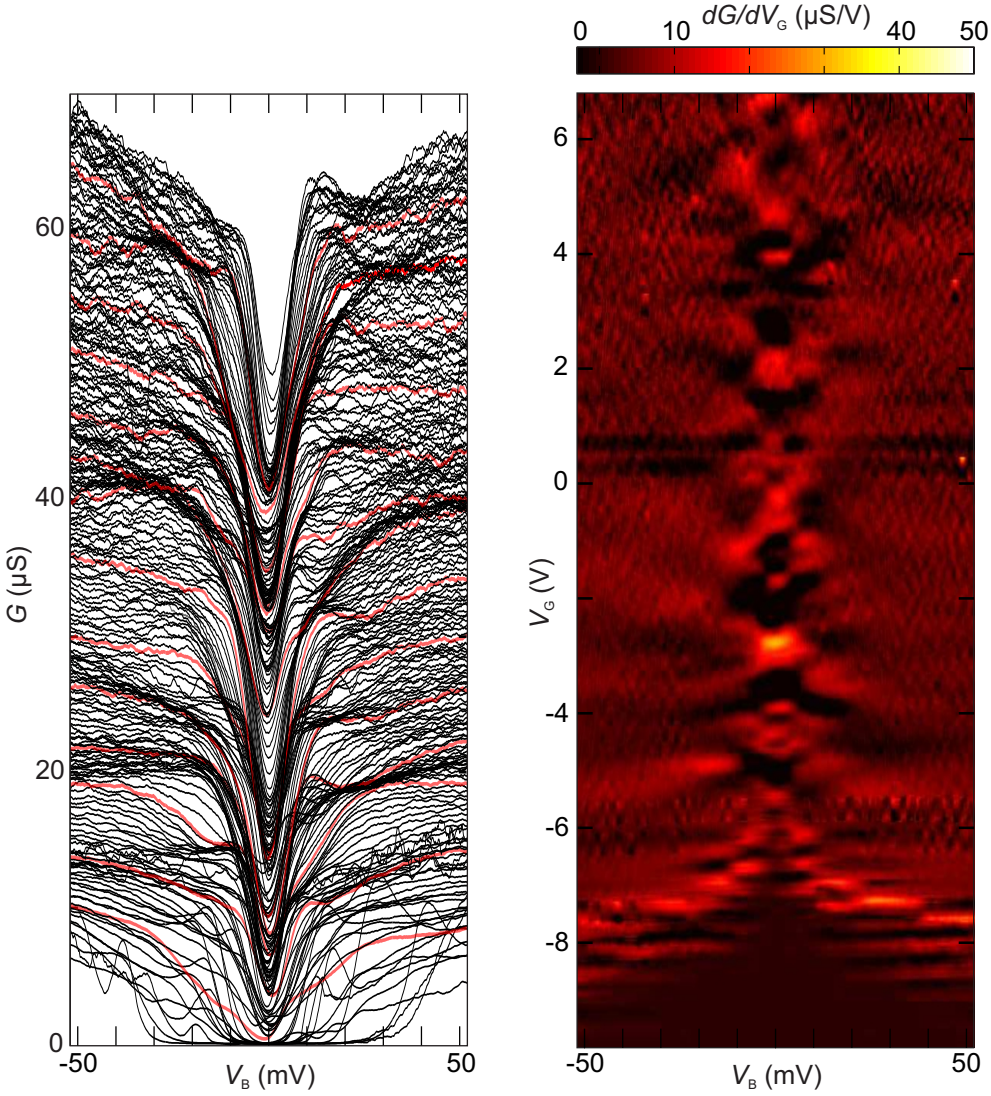

Figure 51: Waterfall and transconductance plot analogous to Fig. 16 for device C (doped Si:P $2 \times 10^{20}\,\mathrm{cm}^{-3}$).

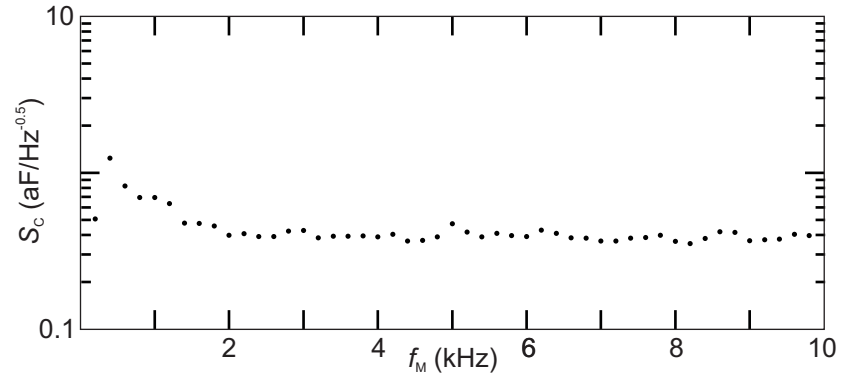

Figure 52: Capacitance sensitivity S_C in the experiment with the SQUID amplifier from Sec. 4.3 as a function of modulation frequency f_M. Other parameters: $P_{IN} = -60\,\mathrm{dBm}$, $V_m = 0.19\,\mathrm{mV_{rms}}$, $V_S = 6.8\,\mathrm{V}$ and $f_C = 196\,\mathrm{MHz}$.

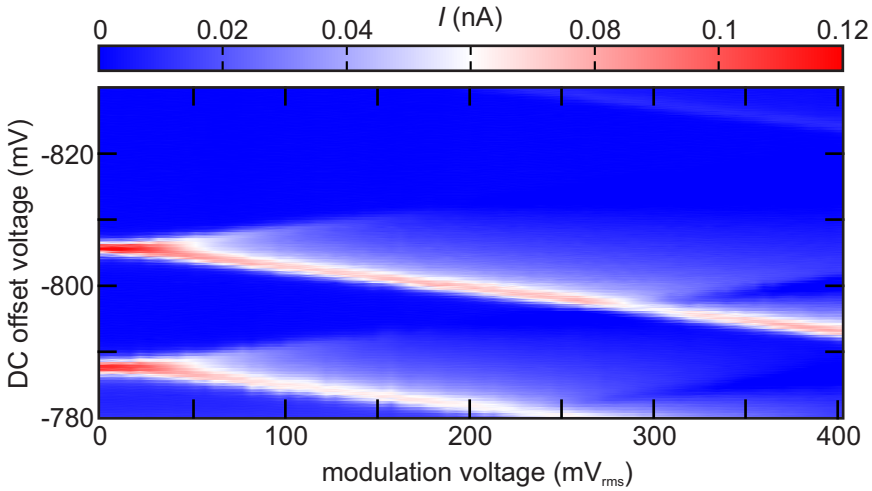

Figure 53: Current through the GaAs quantum dot as a function of gate voltage and applied modulation voltage. Gate voltage and modulation voltage are given in applied voltage to a resistive bias-T.

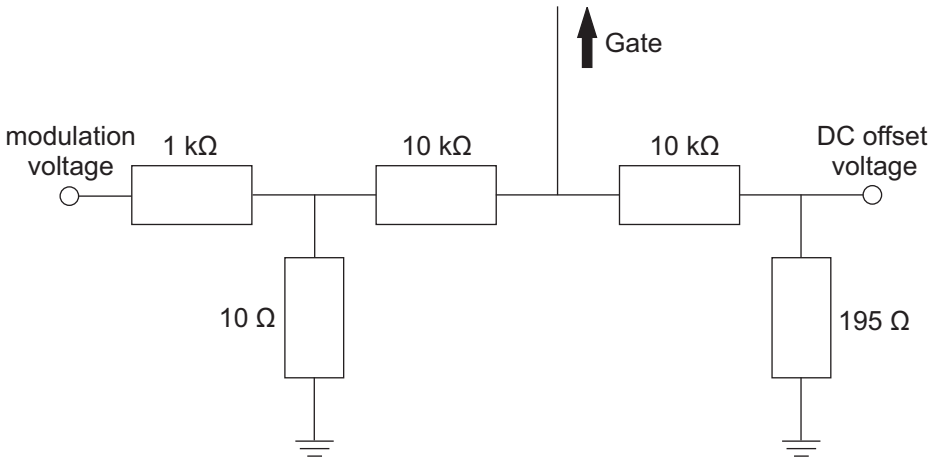

Figure 54: 1/100 divider for the modulation voltage and resistive-T for the application of a DC- and modulation voltage to the gate in charge sensing experiments. The 195 Ω resistor after the offset voltage is made from 19 parallel 3.7 kΩ resistors to carry the current

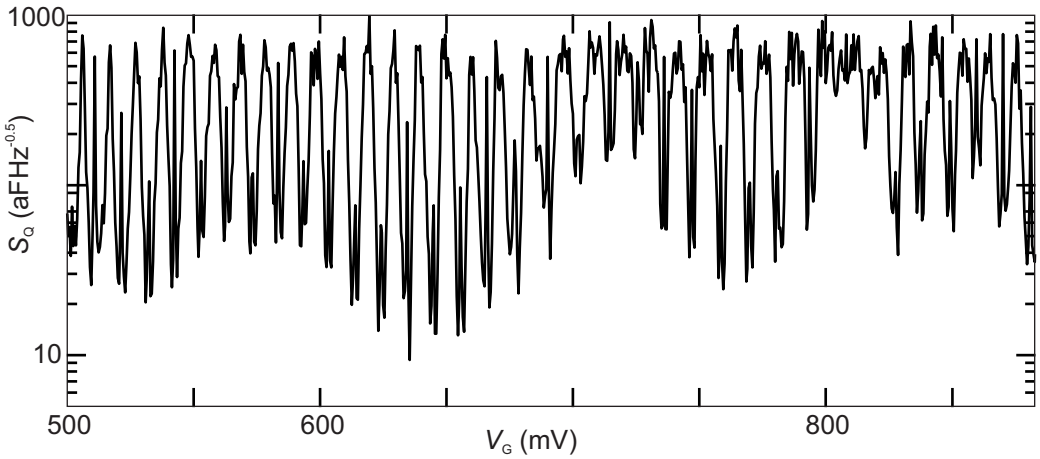

Figure 55: Full gate range in the charge sensitivity measurement from Fig. 41a.

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Declaration

The material within this thesis has not previously been submitted for a degree at the University of Oxford or any other University. The research reported within this thesis has been conducted by the author unless indicated otherwise.

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